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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFBGA
Supplier Device Package	48-BGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg225f32-bga48t

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

## 2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

## 2.1.21 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has one single ended output buffer connected to channel 0. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.22 Operational Amplifier (OPAMP)

The EFM32TG225 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 2.1.23 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE<sup>TM</sup>), is a highly configurable sensor interface with support for up to 12 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

## 2.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

## 2.1.25 General Purpose Input/Output (GPIO)

In the EFM32TG225, there are 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.





Figure 3.2. EM3 current consumption.



Figure 3.3. EM4 current consumption.









### Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = STANDARD





GPIO\_Px\_CTRL DRIVEMODE = HIGH



### Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage



GPIO\_Px\_CTRL DRIVEMODE = STANDARD

![](_page_4_Figure_5.jpeg)

![](_page_5_Picture_0.jpeg)

### Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage

![](_page_5_Figure_3.jpeg)

GPIO\_Px\_CTRL DRIVEMODE = STANDARD

GPIO\_Px\_CTRL DRIVEMODE = HIGH

Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

![](_page_6_Figure_3.jpeg)

Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

![](_page_6_Figure_5.jpeg)

Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

![](_page_6_Figure_7.jpeg)

![](_page_6_Figure_8.jpeg)

#### Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

![](_page_7_Figure_3.jpeg)

![](_page_7_Figure_4.jpeg)

## 3.9.5 AUXHFRCO

### Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		28 MHz frequency band	27.16	28.0	28.84	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
	Oscillation frequen-	14 MHz frequency band	13.58	14.0	14.42	MHz
AUXHFRCO	$T_{AMB}=25^{\circ}C$	11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40 <sup>1</sup>	6.60 <sup>1</sup>	6.80 <sup>1</sup>	MHz
		1 MHz frequency band	1.16 <sup>2</sup>	1.20 <sup>2</sup>	1.24 <sup>2</sup>	MHz
t <sub>AUXHFRCO_settlin</sub>	<sub>g</sub> Settling time after start-up	f <sub>AUXHFRCO</sub> = 14 MHz		0.6		Cycles
TUNESTEP <sub>AU</sub> ) HFRCO	LFrequency step for LSB change in TUNING value			0.3 <sup>3</sup>		%

<sup>1</sup>For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

 $^{2}$ For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

<sup>3</sup>The TUNING field in the CMU\_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

## 3.9.6 ULFRCO

### Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
fulfrco	Oscillation frequen- cy	25°C, 3V	0.70		1.75	kHz
TC <sub>ULFRCO</sub>	Temperature coeffi- cient			0.05		%/°C
VC <sub>ULFRCO</sub>	Supply voltage co- efficient			-18.2		%/V

## 3.10.1 Typical performance

### Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C

![](_page_8_Figure_4.jpeg)

### Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C

![](_page_9_Figure_3.jpeg)

**VDD** Reference

![](_page_10_Figure_2.jpeg)

![](_page_10_Figure_3.jpeg)

**VDD** Reference

![](_page_11_Picture_0.jpeg)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
		OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		16.36		MHz
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		0.81		MHz
CDW	Gain Bandwidth	OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.11		MHz
GBWOPAMP	Product	OPA2 BIASPROG=0xF, HALFBIAS=0x0		2.11		MHz
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.72		MHz
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.09		MHz
		BIASPROG=0xF, HALFBIAS=0x0, C <sub>L</sub> =75 pF		64		o
PM <sub>OPAMP</sub>	Phase Margin	BIASPROG=0x7, HALFBIAS=0x1, C <sub>L</sub> =75 pF		58		o
		BIASPROG=0x0, HALFBIAS=0x1, C <sub>L</sub> =75 pF		58		o
R <sub>INPUT</sub>	Input Resistance			100		Mohm
Rious	Load Resistance	OPA0/OPA1	200			Ohm
∿LOAD		OPA2	2000			Ohm
	Load Current	OPA0/OPA1			11	mA
'LOAD_DC	Load Guilent	OPA2			1.5	mA
V		OPAxHCMDIS=0	V <sub>SS</sub>		V <sub>DD</sub>	V
VINPU1	input voltage	OPAxHCMDIS=1	V <sub>SS</sub>		V <sub>DD</sub> -1.2	V
V <sub>OUTPUT</sub>	Output Voltage		V <sub>SS</sub>		V <sub>DD</sub>	V
Vereer	Input Offset Voltage	Unity Gain, V <sub>SS</sub> <v<sub>in<v<sub>DD, OPAxHCMDIS=0</v<sub></v<sub>		6		mV
VOFFSET	input Onset voltage	Unity Gain, V <sub>SS</sub> <v<sub>in<v<sub>DD-1.2, OPAxHCMDIS=1</v<sub></v<sub>		1		mV
V <sub>OFFSET_DRIFT</sub>	Input Offset Voltage Drift				0.02	mV/°C
		OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		46.11		V/µs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.21		V/µs
SRoows	Slew Rate	OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/µs
UVAMP		OPA2 BIASPROG=0xF, HALFBIAS=0x0		4.43		V/µs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		1.30		V/µs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/µs

![](_page_12_Picture_0.jpeg)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
		OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.52		μs
PU <sub>OPAMP</sub>	Power-up Time	OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		12.74		μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.13		μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.17		μs
	Voltage Noise	V <sub>out</sub> =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=0</f<10>		101		μV <sub>RMS</sub>
		V <sub>out</sub> =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=1</f<10>		141		μV <sub>RMS</sub>
		V <sub>out</sub> =1V, RESSEL=0, 0.1 Hz <f<1 mhz,="" opaxhcmdis="0&lt;/td"><td></td><td>196</td><td></td><td>μV<sub>RMS</sub></td></f<1>		196		μV <sub>RMS</sub>
N <sub>OPAMP</sub>		V <sub>out</sub> =1V, RESSEL=0, 0.1 Hz <f<1 mhz,="" opaxhcmdis="1&lt;/td"><td></td><td>229</td><td></td><td>μV<sub>RMS</sub></td></f<1>		229		μV <sub>RMS</sub>
		RESSEL=7, 0.1 Hz <f<10 khz,<br="">OPAxHCMDIS=0</f<10>		1230		μV <sub>RMS</sub>
		RESSEL=7, 0.1 Hz <f<10 khz,<br="">OPAxHCMDIS=1</f<10>		2130		μV <sub>RMS</sub>
		RESSEL=7, 0.1 Hz <f<1 mhz,<br="">OPAxHCMDIS=0</f<1>		1630		μV <sub>RMS</sub>
		RESSEL=7, 0.1 Hz <f<1 mhz,<br="">OPAxHCMDIS=1</f<1>		2590		μV <sub>RMS</sub>

Figure 3.24. OPAMP Common Mode Rejection Ratio

![](_page_12_Figure_4.jpeg)

# 3.13 Analog Comparator (ACMP)

### Table 3.17. ACMP

Symbol	Parameter	Condition	Min	Тур	Max	Unit
V <sub>ACMPIN</sub>	Input voltage range		0		V <sub>DD</sub>	V
V <sub>ACMPCM</sub>	ACMP Common Mode voltage range		0		V <sub>DD</sub>	V
		BIASPROG=0b0000, FULL- BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	μA
I <sub>ACMP</sub>	Active current	BIASPROG=0b1111, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	μA
		BIASPROG=0b1111, FULL- BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
IACMPREF	Current consump- tion of internal volt-	Internal voltage reference off. Using external voltage refer- ence		0.0	0.5	μA
		Internal voltage reference		2.15	3.00	μA
VACMPOFFSET	Offset voltage	BIASPROG= 0b1010, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
V <sub>ACMPHYST</sub>	ACMP hysteresis	Programmable		17		mV
		CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
P	Capacitive Sense	CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
CSRES	Internal Resistance	CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
t <sub>ACMPSTART</sub>	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 40).  $I_{ACMPREF}$  is zero if an external voltage reference is used.

### Total ACMP Active Current

 $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$ 

(3.1)

![](_page_14_Picture_0.jpeg)

	BGA48 Pin# and Name		Pin Alternate Functi	onality / Description						
Pin #	Pin Name	Analog	Timers	Communication	Other					
A3	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX					
A4	PF5				PRS_CH2 #1					
A5	PF3				PRS_CH0 #1					
A6	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0					
A7	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1					
B1	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0					
B2	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0					
B3	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX					
B4	PF4				PRS_CH1 #1					
B5	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4					
B6	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0					
B7	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0					
C1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0					
C2	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0					
С3	VSS	Ground.								
C4	IOVDD_5	Digital IO power supply 5.								
C5	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1 GPIO_EM4WU3					
C6	PC9	ACMP1_CH1		US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2					
C7	PC10	ACMP1_CH2		US0_RX #2	LES_CH10 #0					
D1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0					
D2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT			LES_CH3 #0					
D3	IOVDD_0	Digital IO power supply 0.		,	,					
D5	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1					
D6	PC8	ACMP1_CH0		US0_CS #2	LES_CH8 #0					
D7	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C <sub>DECOUPLE</sub> is required at this pin.								
E1	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT			LES_CH2 #0					
E2	PC4	ACMP0_CH4 DAC0 P0 /	LETIM0_OUT0 #3		LES_CH4 #0					

![](_page_15_Picture_0.jpeg)

	BGA48 Pin# and Name	Pin Alternate Functionality / Description									
Pin #	Pin Name	Analog	Timers	Communication	Other						
		OPAMP_P0									
E3	PA8										
E4	VDD_DREG	Power supply for on-chip volta	age regulator.								
E5	AVSS_0	Analog ground 0.									
E6	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2						
E7	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2						
F1	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0							
F2	PA9										
F3	RESETn	Reset input, active low. To apply an external reset so ensure that reset is released.	urce to this pin, it is required to o	nly drive this pin low during reset	, and let the internal pull-up						
F4	IOVDD_3	Digital IO power supply 3.									
F5	AVDD_1	Analog power supply 1.			-						
F6	AVDD_0	Analog power supply 0.									
F7	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0							
G1	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0							
G2	PA10										
G3	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LETIM0_OUT0 #1								
G4	AVSS_1	Analog ground 1.	1		I						
G5	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1							
G6	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1							
G7	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0							

## **4.2 Alternate Functionality Pinout**

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 48). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

#### Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCA-TION bitfield. In these cases, the pinout is shown in the column corresponding to LOCA-TION 0.

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Alternate			LOCATION					
Functionality	0	1	2	3	4	5	6	Description
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1					Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14		PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1							Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1		Timer 0 Capture Compare input / output channel 1.

Alternate			L	OCATIO	N			
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC2	PA2	PA2			PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11		PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0					USART1 clock input / output.
US1_CS	PB8		PF1					USART1 chip select input / output.
US1_RX	PC1		PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

# 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32TG225* is shown in Table 4.3 (p. 50). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	PA10	PA9	PA8	-	-	-	-	-	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	-	PC11	PC10	PC9	PC8	-	-	-	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	PD4	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5	PF4	PF3	PF2	PF1	PF0

### Table 4.3. GPIO Pinout

# 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32TG225* is shown in Figure 4.2 (p. 51).

The BGA48 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

![](_page_19_Picture_0.jpeg)

#### Figure 5.3. BGA48 PCB Stencil Design

![](_page_19_Figure_3.jpeg)

 Table 5.3. BGA48 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
а	0.25
b	0.50
d	3.00
e	3.00

- 1. The drawings are not to scale.
- 2. All dimensions are in millimeters.
- 3. All drawings are subject to change without notice.
- 4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
- 5. Stencil thickness 0.125 mm.
- 6. For detailed pin-positioning, see Figure 4.3 (p. 51).

## **5.2 Soldering Information**

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

# A Disclaimer and Trademarks

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