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Details

Product Status	Active
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2286m72f66labhxuma1

2 General Device Information

The XC228xM series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

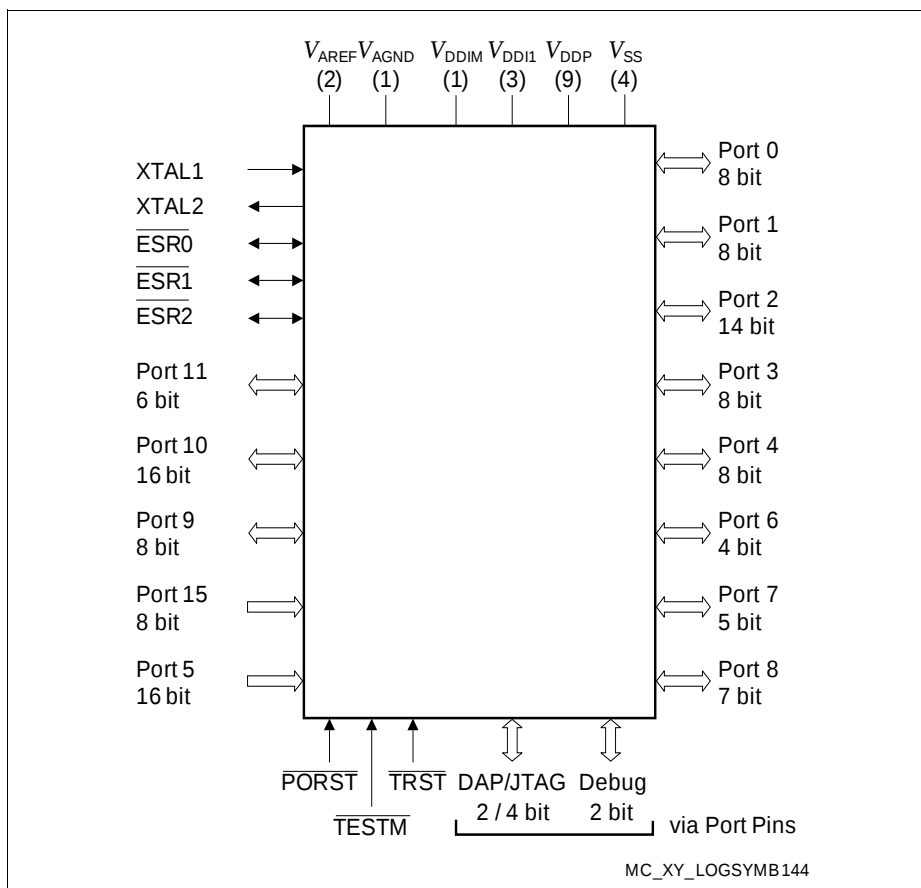


Figure 2 XC228xM Logic Symbol

Key to Pin Definitions

- **Ctrl.:** The output signal for a port pin is selected by bit field PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
- **Type:** Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad - can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	TESTM	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Output
	CCU62_CCP OS0A	I	St/B	CCU62 Position Input 0
	TDI_C	IH	St/B	JTAG Test Data Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
59	P11.3	O0 / I	St/B	Bit 3 of Port 11, General Purpose Input/Output
	CCU61_COU T63	O1	St/B	CCU61 Channel 3 Output
	CCU61_COU T62	O2	St/B	CCU61 Channel 2 Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Input
	CCU61_T13 HRF	I	St/B	External Run Control Input for T13 of CCU61
60	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output
61	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU63_COU T63	O2	St/B	CCU63 Channel 3 Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input
62	P11.2	O0 / I	St/B	Bit 2 of Port 11, General Purpose Input/Output
	CCU61_CC6 1	O1	St/B	CCU61 Channel 1 Output
	U3C1_DOUT	O2	St/B	USIC3 Channel 1 Shift Data Output
	CCU63_CCP OS2A	I	St/B	CCU63 Position Input 2
	CCU61_CC6 1INB	I	St/B	CCU61 Channel 1 Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
75	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3	St/B	CCU61 Channel 0 IOutput
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC60INA	I	St/B	CCU61 Channel 0 Input
	ESR1_11	I	St/B	ESR1 Trigger Input 11
76	P4.5	O0 / I	St/B	Bit 5 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC29	O3 / I	St/B	CAPCOM2 CC29IO Capture Inp./Compare Out.
	CCU61_CCP0S0A	I	St/B	CCU61 Position Input 0
	U3C0_DX0B	I	St/B	USIC3 Channel 0 Shift Data Input
	ESR2_10	I	St/B	ESR2 Trigger Input 10
77	P4.6	O0 / I	St/B	Bit 6 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC30	O3 / I	St/B	CAPCOM2 CC30IO Capture Inp./ Compare Out.
	T4INA	I	St/B	GPT12E Timer T4 Count/Gate Input
	CCU61_CCP0S1A	I	St/B	CCU61 Position Input 1
78	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
	ESR2_8	I	St/B	ESR2 Trigger Input 8
92	P2.13	O0 / I	St/B	Bit 13 of Port 2, General Purpose Input/Output
	U2C1_SELO2	O1	St/B	USIC2 Channel 1 Select/Control 2 Output
	RxDC2D	I	St/B	CAN Node 2 Receive Data Input
93	P3.2	O0 / I	St/B	Bit 2 of Port 3, General Purpose Input/Output
	U2C0_SCLKOUT	O1	St/B	USIC2 Channel 0 Shift Clock Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U2C0_DX1B	I	St/B	USIC2 Channel 0 Shift Clock Input
	HOLD	IH	St/B	External Bus Master Hold Request Input
94	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	A23	OH	St/B	External Bus Interface Address Line 23
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input
	U3C1_DX0A	I	St/B	USIC3 Channel 1 Shift Data Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
120	P1.2	O0 / I	St/B	Bit 2 of Port 1, General Purpose Input/Output
	CCU62_CC62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO6	O2	St/B	USIC1 Channel 0 Select/Control 6 Output
	U2C1_SCLKOUT	O3	St/B	USIC2 Channel 1 Shift Clock Output
	A10	OH	St/B	External Bus Interface Address Line 10
	ESR1_4	I	St/B	ESR1 Trigger Input 4
	CCU61_T12HRB	I	St/B	External Run Control Input for T12 of CCU61
	CCU62_CC62INA	I	St/B	CCU62 Channel 2 Input
	U2C1_DX0D	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1C	I	St/B	USIC2 Channel 1 Shift Clock Input
121	P10.12	O0 / I	St/B	Bit 12 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	TDO_B	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	AD12	OH / IH	St/B	External Bus Interface Address/Data Line 12
	U1C0_DX0C	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1E	I	St/B	USIC1 Channel 0 Shift Clock Input
122	P9.3	O0 / I	St/B	Bit 3 of Port 9, General Purpose Input/Output
	CCU63_COUT60	O1	St/B	CCU63 Channel 0 Output
	BRKOUT	O2	St/B	OCDS Break Signal Output

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
123	P10.13	O0 / I	St/B	Bit 13 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U1C0_SELO 3	O3	St/B	USIC1 Channel 0 Select/Control 3 Output
	WR/WRL	OH	St/B	External Bus Interface Write Strobe Output Active for each external write access, when <u>WR</u> , active for ext. writes to the low byte, when <u>WRL</u> .
	U1C0_DX0D	I	St/B	USIC1 Channel 0 Shift Data Input
124	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output
	CCU62_COU T63	O1	St/B	CCU62 Channel 3 Output
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output
	A11	OH	St/B	External Bus Interface Address Line 11
	ESR2_4	I	St/B	ESR2 Trigger Input 4
	CCU62_T12 HRB	I	St/B	External Run Control Input for T12 of CCU62
125	P9.4	O0 / I	St/B	Bit 4 of Port 9, General Purpose Input/Output
	CCU63_COU T61	O1	St/B	CCU63 Channel 1 Output
	U2C0_DOUT	O2	St/B	USIC2 Channel 0 Shift Data Output
	CCU62_COU T63	O3	St/B	CCU62 Channel 3 Output

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
130	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input
131	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output
	CCU62_COUT60	O1	St/B	CCU62 Channel 0 Output
	U1C1_SELO3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output
	BRKOUT	O3	St/B	OCDS Break Signal Output
	A13	OH	St/B	External Bus Interface Address Line 13
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input
132	P9.6	O0 / I	St/B	Bit 6 of Port 9, General Purpose Input/Output
	CCU63_COUT63	O1	St/B	CCU63 Channel 3 Output
	CCU63_COUT62	O2	St/B	CCU63 Channel 2 Output
	CCU62_COUT61	O3	St/B	CCU62 Channel 1 Output
	CCU63_CTRAPA	I	St/B	CCU63 Emergency Trap Input
	CCU60_CCP0S1B	I	St/B	CCU60 Position Input 1

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.</i>
1, 37, 73, 109	V_{SS}	-	PS/--	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane. <i>Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.</i> <i>For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</i>

- 1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

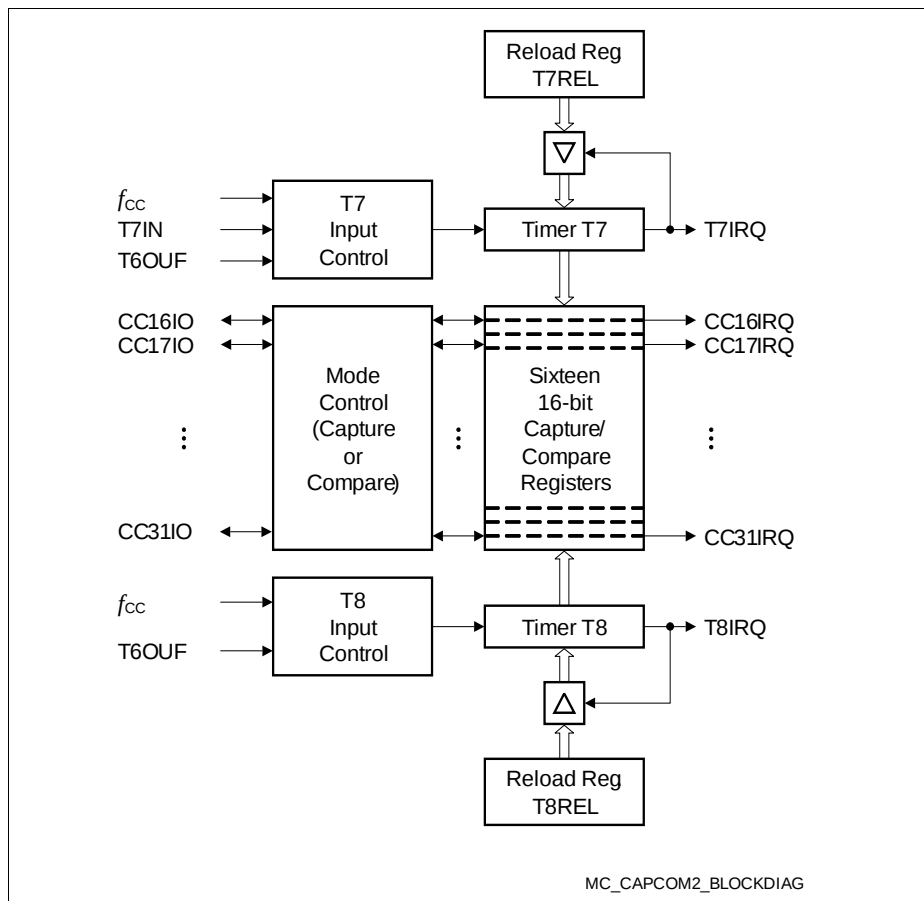


Figure 6 CAPCOM2 Unit Block Diagram

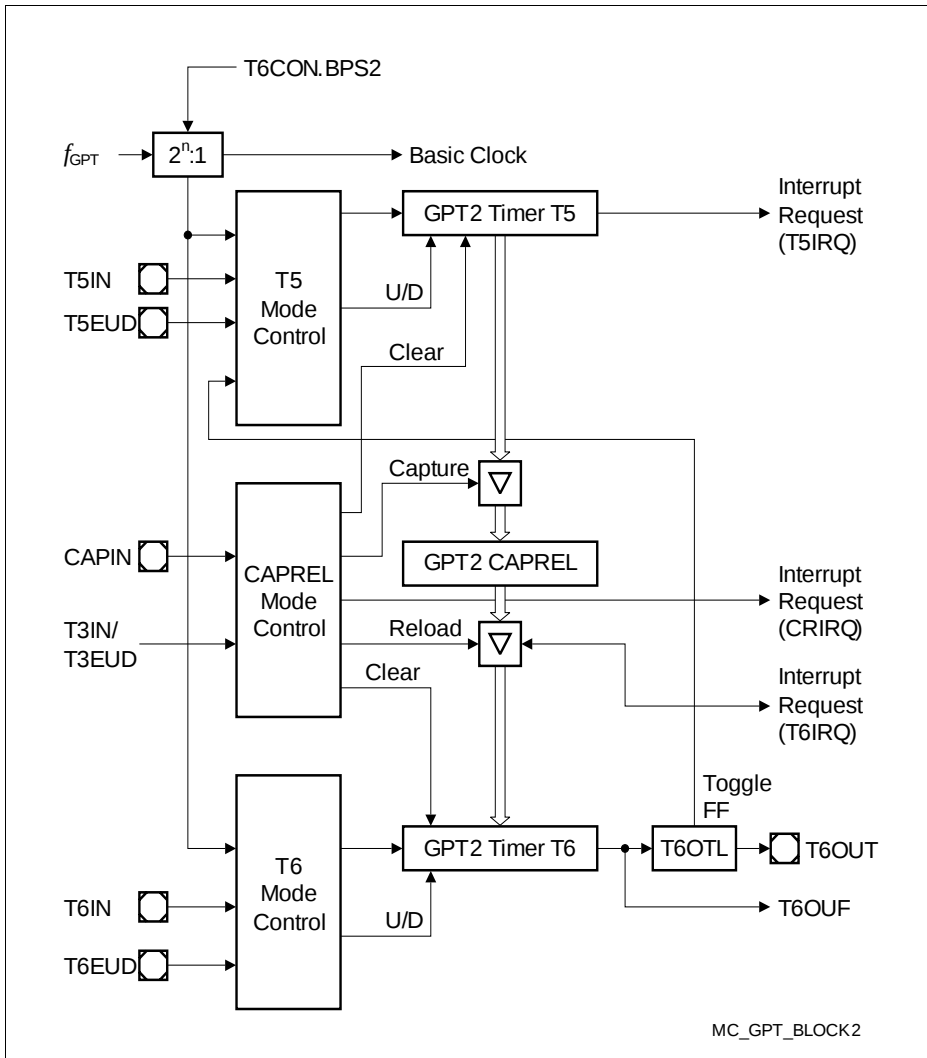


Figure 9 Block Diagram of GPT2

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.20 Instruction Set Summary

Table 11 lists the instructions of the XC228xM.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 11 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4.3 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 18 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	4	5	pF	not subject to production test ¹⁾
Total capacitance at an analog input	C_{AINT} CC	–	10	12	pF	not subject to production test ¹⁾
Switched capacitance at the reference input	C_{AREFSW} CC	–	7	9	pF	not subject to production test ¹⁾
Total capacitance at the reference input	C_{AREFT} CC	–	13	15	pF	not subject to production test ¹⁾
Differential Non-Linearity Error	$ EA_{DNL} $ CC	–	0.8	1.0	LSB	not subject to production test
Gain Error	$ EA_{GAIN} $ CC	–	0.4	0.8	LSB	not subject to production test
Integral Non-Linearity	$ EA_{INL} $ CC	–	0.8	1.2	LSB	not subject to production test
Offset Error	$ EA_{OFF} $ CC	–	0.5	0.8	LSB	not subject to production test
Analog clock frequency	f_{ADCI} SR	0.5	–	20	MHz	Upper voltage range
		0.5	–	16.5	MHz	Lower voltage range
Input resistance of the selected analog channel	R_{AIN} CC	–	–	2	kOhm	not subject to production test ¹⁾
Input resistance of the reference input	R_{AREF} CC	–	–	2	kOhm	not subject to production test ¹⁾

Coding of bit fields LEVxV in SWD and PVC Configuration Registers

Table 21 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes ¹⁾
0000 _B	2.9 V	
0001 _B	3.0 V	LEV1V: reset request
0010 _B	3.1 V	
0011 _B	3.2 V	
0100 _B	3.3 V	
0101 _B	3.4 V	
0110 _B	3.6 V	
0111 _B	4.0 V	
1000 _B	4.2 V	
1001 _B	4.5 V	LEV2V: no request
1010 _B	4.6 V	
1011 _B	4.7 V	
1100 _B	4.8 V	
1101 _B	4.9 V	
1110 _B	5.0 V	
1111 _B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B	0.95 V	
001 _B	1.05 V	
010 _B	1.15 V	
011 _B	1.25 V	
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B	1.55 V	
111 _B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

4.5 Flash Memory Parameters

The XC228xM is delivered with all Flash sectors erased and with no protection installed. The data retention time of the XC228xM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 23 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	4 ¹⁾		$N_{FL_RD} \leq 1$, $f_{SYS} \leq 80$ MHz
		–	–	1 ²⁾		$N_{FL_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq 20$ years
Flash wait states ³⁾	N_{WSFLAS} H SR	1	–	–		$f_{SYS} \leq 8$ MHz
		2	–	–		$f_{SYS} \leq 13$ MHz
		3	–	–		$f_{SYS} \leq 17$ MHz
		4	–	–		$f_{SYS} > 17$ MHz
Erase time per sector/page	t_{ER} CC	–	7 ⁴⁾	8.0	ms	
Programming time per page	t_{PR} CC	–	3 ⁴⁾	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{Er} \leq 1\,000$ cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC228xM. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2
- By supplying an **external clock signal**
 - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain)

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH} . If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters ($t_1 \dots t_4$) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 25 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input = clock signal
		4	–	16	MHz	Input = crystal or ceramic resonator
XTAL1 input current absolute value	$ I_{IL} $ CC	–	–	20	μA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	–	8	ns	
Input clock fall time	t_4 SR	–	–	8	ns	
Input voltage amplitude on XTAL1 ¹⁾	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	4 to 16 MHz
		0.4 x V_{DDIM}	–	–	V	16 to 25 MHz
		0.5 x V_{DDIM}	–	–	V	25 to 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	²⁾

Electrical Parameters

Table 26 is valid under the following conditions:

$V_{DDP} \geq 4.5 \text{ V}$; $V_{DDPtyp} = 5 \text{ V}$; $V_{DDP} \leq 5.5 \text{ V}$; $C_L \geq 20 \text{ pF}$; $C_L \leq 100 \text{ pF}$;

Table 26 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	—	—	10	mA	Strong driver
		—	—	4.0	mA	Medium driver
		—	—	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	—	—	2.5	mA	Strong driver
		—	—	1.0	mA	Medium driver
		—	—	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	$4.2 + 0.14 \times C_L$	ns	Strong driver; Sharp edge
		—	—	$11.6 + 0.22 \times C_L$	ns	Strong driver; Medium edge
		—	—	$20.6 + 0.22 \times C_L$	ns	Strong driver; Slow edge
		—	—	$23 + 0.6 \times C_L$	ns	Medium driver
		—	—	$212 + 1.9 \times C_L$	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 50 mA.

4.6.5.2 External Bus Arbitration

If the arbitration signals are enabled, the XC228xM makes its external resources available in response to an arbitration request.

Note: Operating Conditions apply.

Table 32 Bus Arbitration Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input setup time HOLD input	t_{40} SR	23		–	ns	
Output delay rising edge HLDA, BREQ	t_{41} CC	-1		13	ns	
Output delay falling edge HLDA	t_{42} CC	-2		14	ns	

Table 33 Bus Arbitration Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input setup time HOLD input	t_{40} SR	28		–	ns	
Output delay rising edge HLDA, BREQ	t_{41} CC	-1		19	ns	
Output delay falling edge HLDA	t_{42} CC	-2		21	ns	

Electrical Parameters

Table 35 USIC SSC Master Mode Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	—	—	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 36 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	7	—	—	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	7	—	—	ns	
Receive data input setup time to shift clock receive edge ¹⁾	t_{12} SR	7	—	—	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	5	—	—	ns	
Data output DOUT valid time	t_{14} CC	7	—	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).