Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2287m104f80laakxuma1

Edition 2011-07

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC228xM Special Device Types

Derivative[1)]	Flash Memory[2)]	PSRAM DSRAM[3)]	Capt./Comp. Modules	ADC[4)] Chan.	Interfaces[4)]
XC2287M-56FxxL	448 Kbytes	16/8 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	6 CAN Nodes, 8 Serial Chan.
XC2286M-104FxxL	832 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	3 CAN Nodes, 8 Serial Chan.
XC2286M-72FxxL	576 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	3 CAN Nodes, 8 Serial Chan.
XC2286M-56FxxL	448 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	3 CAN Nodes, 8 Serial Chan.
XC2285M-104FxxL	832 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XC2285M-72FxxL	576 Kbytes	32/16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XC2285M-56FxxL	448 Kbytes	16/8 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).
2) Specific information about the on-chip Flash memory in **Table 3**.
3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.3 Definition of Feature Variants

The XC228xM types are offered with several Flash memory sizes. **Table 3** describes the location of the available memory areas for each Flash memory size.

Table 3 Flash Memory Allocation

Total Flash Size	Flash Area A[1]	Flash Area B	Flash Area C
832 Kbytes	C0’0000$_H$ … C0’EFFF$_H$	C1’0000$_H$ … CC’FFFF$_H$	n.a.
576 Kbytes	C0’0000$_H$ … C0’EFFF$_H$	C1’0000$_H$ … C7’FFFF$_H$	CC’0000$_H$ … CC’FFFF$_H$
448 Kbytes	C0’0000$_H$ … C0’EFFF$_H$	C1’0000$_H$ … C5’FFFF$_H$	CC’0000$_H$ … CC’FFFF$_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0’F000$_H$ to C0’FFFF$_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1]	Flash 1	Flash 2	Flash 3
832 Kbytes	256	256	256	64
576 Kbytes	256	256	---	64
448 Kbytes	256	128	---	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0’F000$_H$ to C0’FFFF$_H$).

The XC228xM types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 … CH15
8 ADC0 channels	CH0 … CH7
8 ADC1 channels	CH0 … CH7 (overlay: CH8 … CH11)
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 256 message objects
3 CAN nodes	CAN0, CAN1, CAN2 64 message objects
2 CAN nodes	CAN0, CAN1 64 message objects

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
104	P3.6	O0 / I	St/B	**Bit 6 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	U0C0_SELO6	O3	St/B	**USIC0 Channel 0 Select/Control 6 Output**
	U2C1_DX0A	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1B	I	St/B	**USIC2 Channel 1 Shift Clock Input**
105	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / IH	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCPOS0A	I	St/B	**CCU60 Position Input 0**
	RxDC4C	I	St/B	**CAN Node 4 Receive Data Input**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
106	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_SELO3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	TxDC3	O3	St/B	**CAN Node 3 Transmit Data Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_CTRAPB	I	St/B	**CCU61 Emergency Trap Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
107	P3.7	O0 / I	St/B	**Bit 7 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	U2C0_SELO3	O2	St/B	**USIC2 Channel 0 Select/Control 3 Output**
	U0C0_SELO7	O3	St/B	**USIC0 Channel 0 Select/Control 7 Output**
	U2C1_DX0B	I	St/B	**USIC2 Channel 1 Shift Data Input**
111	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_MCLKOUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_SELO4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	CCU62_CTRAPB	I	St/B	**CCU62 Emergency Trap Input**
	T6INB	I	St/B	**GPT12E Timer T6 Count/Gate Input**
112	P9.0	O0 / I	St/B	**Bit 0 of Port 9, General Purpose Input/Output**
	CCU63_CC60	O1	St/B	**CCU63 Channel 0 Output**
	CCU63_CC60INA	I	St/B	**CCU63 Channel 0 Input**
	T6EUDB	I	St/B	**GPT12E Timer T6 External Up/Down Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
126	P9.5	O0 / I	St/B	**Bit 5 of Port 9, General Purpose Input/Output**
	CCU63_COUT62	O1	St/B	**CCU63 Channel 2 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**
	CCU62_COUT62	O3	St/B	**CCU62 Channel 2 Output**
	U2C0_DX0E	I	St/B	**USIC2 Channel 0 Shift Data Input**
	CCU60_CCPOS2B	I	St/B	**CCU60 Position Input 2**
128	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_SELO1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U3C0_SCLKOUT	O3	St/B	**USIC3 Channel 0 Shift Clock Output**
	$\overline{RD}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC3C	I	St/B	**CAN Node 3 Receive Data Input**
	U3C0_DX1A	I	St/B	**USIC3 Channel 0 Shift Clock Input**
129	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	CCU62_COUT61	O1	St/B	**CCU62 Channel 1 Output**
	U1C1_SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
	RxDC5A	I	St/B	**CAN Node 5 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
137	XTAL1	I	Sp/M	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.
	ESR2_9	I	St/B	**ESR2 Trigger Input 9**
138	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC228xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
139	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**

3.1 Memory Subsystem and Organization

The memory space of the XC228xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC228xM Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	With Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for Flash	$CD'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 3	$CC'0000_H$	$CC'FFFF_H$	64 Kbytes	–
Program Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	[3)]
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[4)]	$21'0000_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
Reserved	$20'BC00_H$	$20'FFFF_H$	17 Kbytes	–
USIC alternate regs.	$20'B000_H$	$20'BFFF_H$	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	$20'8000_H$	$20'AFFF_H$	12 Kbytes	Accessed via EBC
Reserved	$20'6000_H$	$20'7FFF_H$	8 Kbytes	–
USIC registers	$20'4000_H$	$20'5FFF_H$	8 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–

Table 8 XC228xM Memory Map (cont'd)[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Data SRAM	$00'A000_H$	$00'DFFF_H$	16 Kbytes	–
Reserved for DSRAM	$00'8000_H$	$00'9FFF_H$	8 Kbytes	–
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated. See column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1)]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{\text{CS}}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

A $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ protocol is available for bus arbitration; this allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software, after which pins P3.0 … P3.2 ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{\text{HLDA}}$ pin is an output. In Slave Mode pin $\overline{\text{HLDA}}$ is switched to be an input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

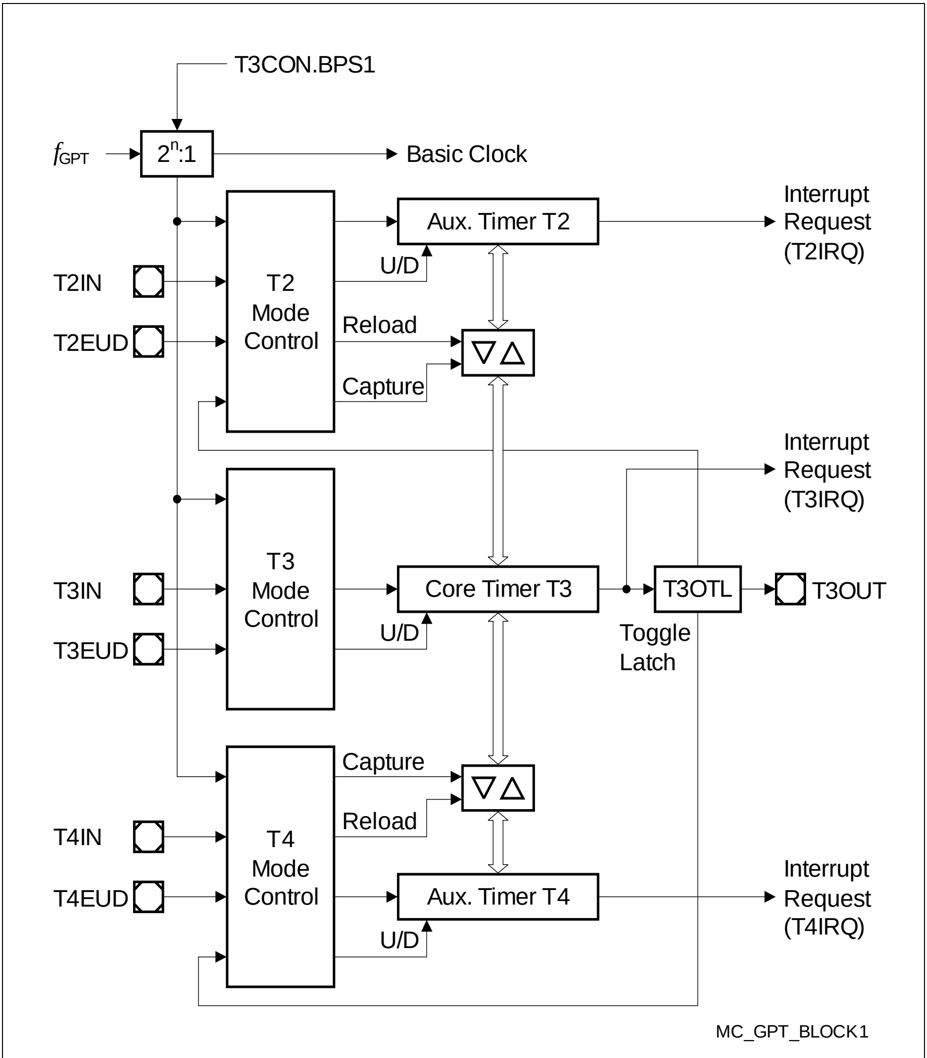

Figure 8 Block Diagram of GPT1

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  – Can be assigned to one of the CAN nodes
  – Configurable as transmit or receive objects, or as message buffer FIFO
  – Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  – Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

4 Electrical Parameters

The operating range for the XC228xM is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	–	–	mA	
Output current on a pin when low value is driven	I_{OL} SR	–	–	30	mA	
Overload current	I_{OV} SR	-10	–	10	mA	1)
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	100	mA	1)
Junction Temperature	T_J SR	-40	–	150	°C	
Storage Temperature	T_{ST} SR	-65	–	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDPA}, V_{DDPB} SR	-0.5	–	6.0	V	
Voltage on any pin with respect to ground (Vss)	V_{IN} SR	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

4.2.3 Power Consumption

The power consumed by the XC228xM depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.
- **Standby mode**:
  Voltage domain DMP_1 switched off completely, power supply control switched off.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} and V_{DDI1} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Note: Operating Conditions apply.

Table 16 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	10 + 0.6 x f_{SYS}[1]	10 + 1.0 x f_{SYS}[1]	mA	[2][3]
Power supply current in standby mode[4]	I_{SSB} CC	–	100	250	µA	Upper voltage range
		–	70	150	µA	Lower voltage range
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	0.7	2.0	mA	

1) f_{SYS} in MHz.

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x f_{SYS}.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) These values are valid if the voltage validation circuits for V_{DDPB} (SWD) and V_{DDIM} (PVC_M) are off. Leaving SWD and PVC_M active adds another 90 µA.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC228xM's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 0.6×f_{SYS}) mA.

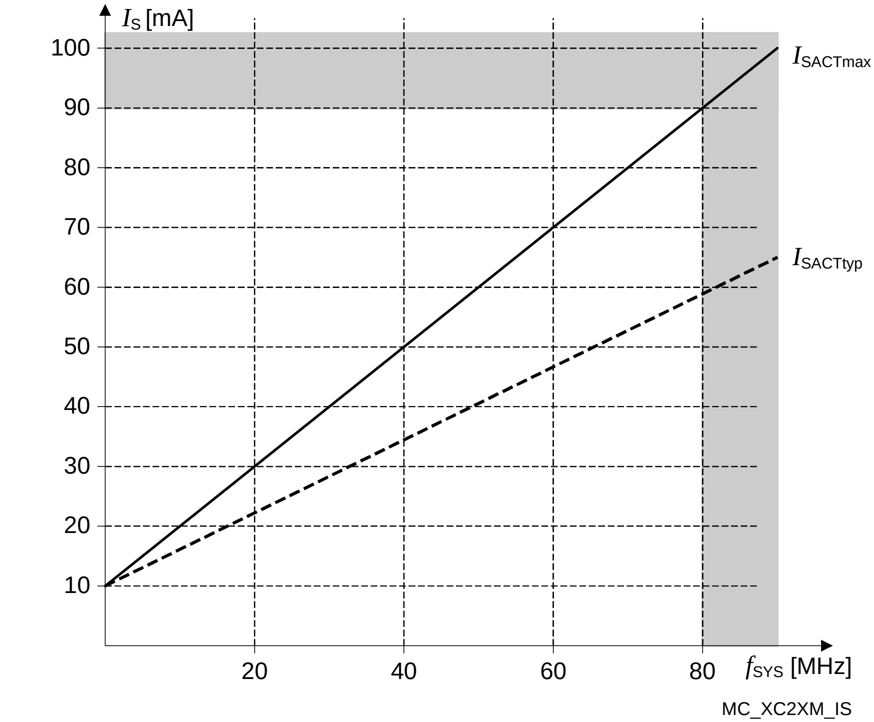

Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 23 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{Er} SR	–	–	15 000	cycles	t_{RET} Ó 5 years; Valid for up to 64 user-selected sectors (data storage)
		–	–	1 000	cycles	t_{RET} Ó 20 years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.

3) Value of IMB_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC228xM Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.6.5.2 External Bus Arbitration

If the arbitration signals are enabled, the XC228xM makes its external resources available in response to an arbitration request.

Note: Operating Conditions apply.

Table 32 Bus Arbitration Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input setup time $\overline{\text{HOLD}}$ input	t_{40} SR	23		–	ns	
Output delay rising edge $\overline{\text{HLDA}}$, $\overline{\text{BREQ}}$	t_{41} CC	-1		13	ns	
Output delay falling edge $\overline{\text{HLDA}}$	t_{42} CC	-2		14	ns	

Table 33 Bus Arbitration Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input setup time $\overline{\text{HOLD}}$ input	t_{40} SR	28		–	ns	
Output delay rising edge $\overline{\text{HLDA}}$, $\overline{\text{BREQ}}$	t_{41} CC	-1		19	ns	
Output delay falling edge $\overline{\text{HLDA}}$	t_{42} CC	-2		21	ns	

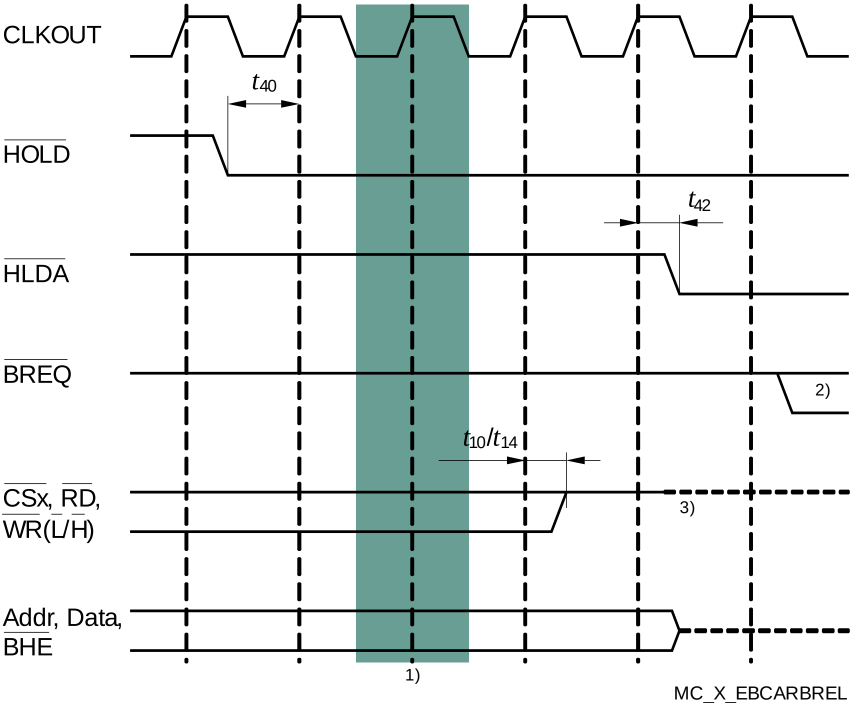

Figure 26 External Bus Arbitration, Releasing the Bus

Notes

1. *The XC228xM completes the currently running bus cycle before granting bus access.*
2. *This is the first possibility for $\overline{\text{BREQ}}$ to get active.*
3. *The control outputs will be resistive high (pull-up) after being driven inactive (ALE will be low).*