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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2287m104f80lrabkxuma1

1.3 Definition of Feature Variants

The XC228xM types are offered with several Flash memory sizes. **Table 3** describes the location of the available memory areas for each Flash memory size.

Table 3 Flash Memory Allocation

Total Flash Size	Flash Area A[1]	Flash Area B	Flash Area C
832 Kbytes	C0'0000$_H$ … C0'EFFF$_H$	C1'0000$_H$ … CC'FFFF$_H$	n.a.
576 Kbytes	C0'0000$_H$ … C0'EFFF$_H$	C1'0000$_H$ … C7'FFFF$_H$	CC'0000$_H$ … CC'FFFF$_H$
448 Kbytes	C0'0000$_H$ … C0'EFFF$_H$	C1'0000$_H$ … C5'FFFF$_H$	CC'0000$_H$ … CC'FFFF$_H$

[1] The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000$_H$ to C0'FFFF$_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1]	Flash 1	Flash 2	Flash 3
832 Kbytes	256	256	256	64
576 Kbytes	256	256	---	64
448 Kbytes	256	128	---	64

[1] The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000$_H$ to C0'FFFF$_H$).

The XC228xM types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 … CH15
8 ADC0 channels	CH0 … CH7
8 ADC1 channels	CH0 … CH7 (overlay: CH8 … CH11)
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 256 message objects
3 CAN nodes	CAN0, CAN1, CAN2 64 message objects
2 CAN nodes	CAN0, CAN1 64 message objects

2.1 Pin Configuration and Definition

The pins of the XC228xM are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

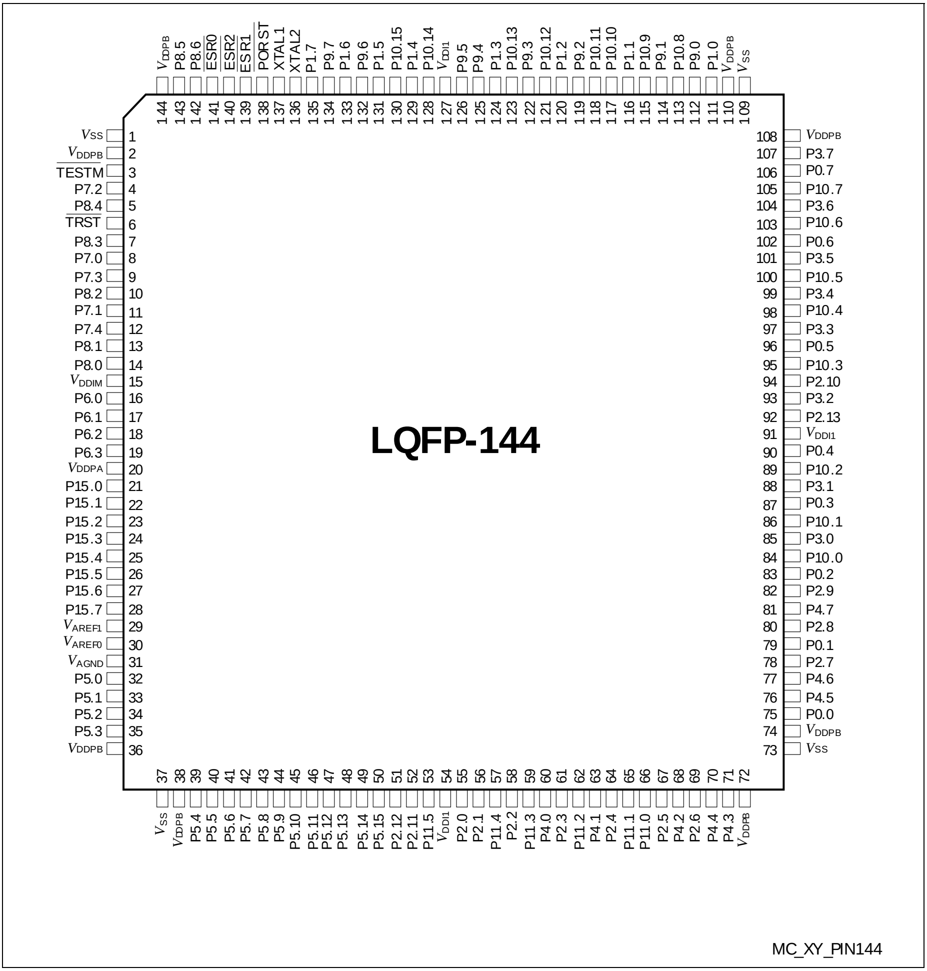

Figure 3 XC228xM Pin Configuration (top view)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P8.4	O0 / I	St/B	**Bit 4 of Port 8, General Purpose Input/Output**
	CCU60_COUT61	O1	St/B	**CCU60 Channel 1 Output**
	CCU62_CC61	O2	St/B	**CCU62 Channel 1 Output**
	TMS_D	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC61INB	I	St/B	**CCU62 Channel 1 Input**
6	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC228xM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	**Bit 3 of Port 8, General Purpose Input/Output**
	CCU60_COUT60	O1	St/B	**CCU60 Channel 0 Output**
	CCU62_CC60	O2	St/B	**CCU62 Channel 0 Output**
	TDI_D	IH	St/B	**JTAG Test Data Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC60INB	I	St/B	**CCU62 Channel 0 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU62_CCPOS2A	I	St/B	**CCU62 Position Input 2**
	TCK_C	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
13	P8.1	O0 / I	St/B	**Bit 1 of Port 8, General Purpose Input/Output**
	CCU60_CC61	O1	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INB	I	St/B	**CCU60 Channel 1 Input**
	RxDC1F	I	St/B	**CAN Node 1 Receive Data Input**
14	P8.0	O0 / I	St/B	**Bit 0 of Port 8, General Purpose Input/Output**
	CCU60_CC60	O1	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INB	I	St/B	**CCU60 Channel 0 Input**
16	P6.0	O0 / I	DA/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	DA/A	**External Analog MUX Control Output 0 (ADC0)**
	TxDC2	O2	DA/A	**CAN Node 2 Transmit Data Output**
	$\overline{\text{BRKOUT}}$	O3	DA/A	**OCDS Break Signal Output**
	ADCx_REQGTyG	I	DA/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	DA/A	**USIC1 Channel 1 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P2.1	O0 / I	St/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	St/B	**CAN Node 0 Transmit Data Output**
	CCU63_CC61	O2	St/B	**CCU63 Channel 1 Output**
	AD14	OH / IH	St/B	**External Bus Interface Address/Data Line 14**
	RxDC5C	I	St/B	**CAN Node 5 Receive Data Input**
	CCU63_CC61INB	I	St/B	**CCU63 Channel 1 Input**
	T5EUDB	I	St/B	**GPT12E Timer T5 External Up/Down Control Input**
	ESR1_5	I	St/B	**ESR1 Trigger Input 5**
57	P11.4	O0 / I	St/B	**Bit 4 of Port 11, General Purpose Input/Output**
	CCU61_CC62	O1	St/B	**CCU61 Channel 2 Output**
	U3C1_DOUT	O2	St/B	**USIC3 Channel 1 Shift Data Output**
	RxDC5B	I	St/B	**CAN Node 5 Receive Data Input**
	CCU61_CC62INB	I	St/B	**CCU61 Channel 2 Input**
	U3C1_DX0B	I	St/B	**USIC3 Channel 1 Shift Data Input**
58	P2.2	O0 / I	St/B	**Bit 2 of Port 2, General Purpose Input/Output**
	TxDC1	O1	St/B	**CAN Node 1 Transmit Data Output**
	CCU63_CC62	O2	St/B	**CCU63 Channel 2 Output**
	AD15	OH / IH	St/B	**External Bus Interface Address/Data Line 15**
	CCU63_CC62INB	I	St/B	**CCU63 Channel 2 Input**
	ESR2_5	I	St/B	**ESR2 Trigger Input 5**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
104	P3.6	O0 / I	St/B	**Bit 6 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	U0C0_SELO6	O3	St/B	**USIC0 Channel 0 Select/Control 6 Output**
	U2C1_DX0A	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1B	I	St/B	**USIC2 Channel 1 Shift Clock Input**
105	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / IH	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCPOS0A	I	St/B	**CCU60 Position Input 0**
	RxDC4C	I	St/B	**CAN Node 4 Receive Data Input**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
106	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_SELO3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	TxDC3	O3	St/B	**CAN Node 3 Transmit Data Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_CTRAPB	I	St/B	**CCU61 Emergency Trap Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
113	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	AD8	OH / IH	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN}}$_B	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
114	P9.1	O0 / I	St/B	**Bit 1 of Port 9, General Purpose Input/Output**
	CCU63_CC61	O1	St/B	**CCU63 Channel 1 Output**
	CCU63_CC61INA	I	St/B	**CCU63 Channel 1 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent $V_{\mathrm{DDP}}/V_{\mathrm{SS}}$ pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage* V_{DDPB}.
1, 37, 73, 109	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to* V_{SS}. *To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.* *For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

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1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{\text{CS}}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

A $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ protocol is available for bus arbitration; this allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software, after which pins P3.0 … P3.2 ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{\text{HLDA}}$ pin is an output. In Slave Mode pin $\overline{\text{HLDA}}$ is switched to be an input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

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1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

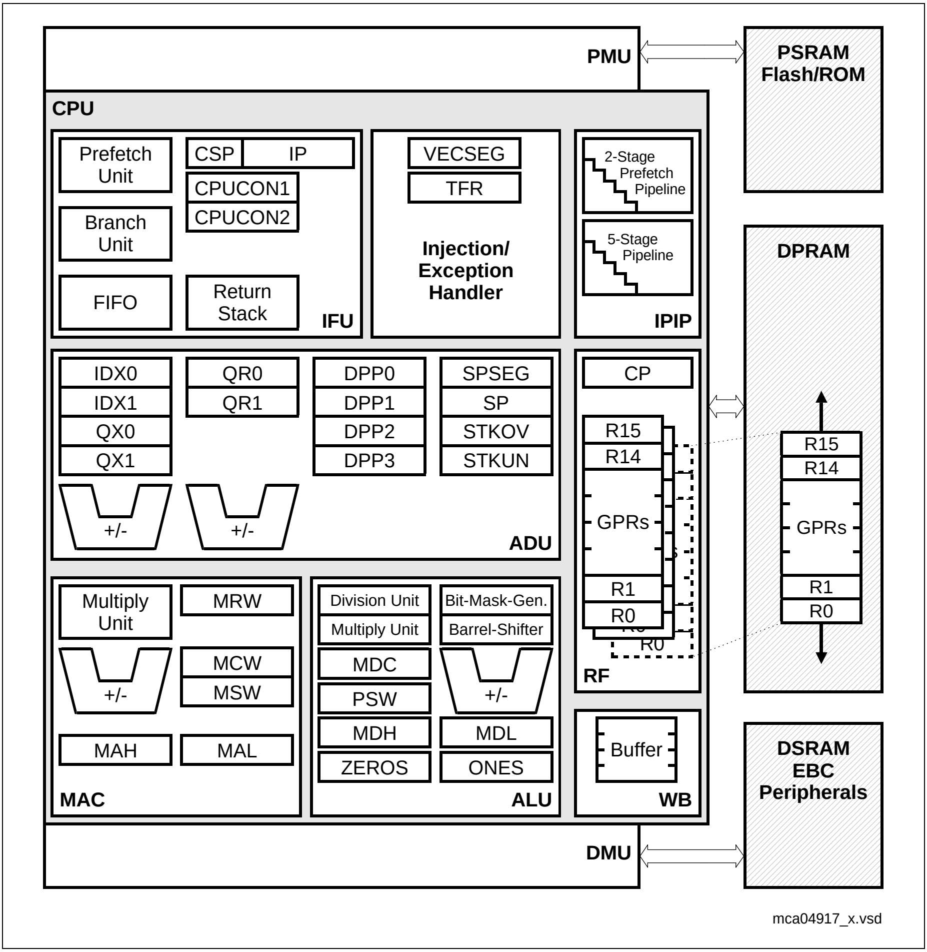

Figure 5 CPU Block Diagram

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

Table 11 Instruction Set Summary (cont'd)

Mnemonic	**Description**	**Bytes**
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction1)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Table 15 DC Characteristics for Lower Voltage Range (cont'd)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Output Low Voltage[8]	V_{OL} CC	–	–	1.0	V	$I_{OL} \leq I_{OLmax}$
		–	–	0.4	V	$I_{OL} \leq I_{OLnom}$[10]

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} <= V_{IL}$ for a pullup; $V_{PIN} >= V_{IH}$ for a pulldown.

6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} >= V_{IH}$ for a pullup; $V_{PIN} <= V_{IL}$ for a pulldown.

8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

9) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.

10) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

Table 16 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	10 + 0.6 x f_{SYS}[1]	10 + 1.0 x f_{SYS}[1]	mA	[2][3]
Power supply current in standby mode[4]	I_{SSB} CC	–	100	250	µA	Upper voltage range
		–	70	150	µA	Lower voltage range
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	0.7	2.0	mA	

1) f_{SYS} in MHz.

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x f_{SYS}.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) These values are valid if the voltage validation circuits for V_{DDPB} (SWD) and V_{DDIM} (PVC_M) are off. Leaving SWD and PVC_M active adds another 90 µA.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC228xM's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 0.6×f_{SYS}) mA.

Sample time and conversion time of the XC228xM's A/D converters are programmable. The timing above can be calculated using **Table 19**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 19 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	$f_{SYS} / 2$	01_H	$t_{ADCI} \times 3$
000010_B	$f_{SYS} / 3$	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	$f_{SYS} / 63$	FE_H	$t_{ADCI} \times 256$
111111_B	$f_{SYS} / 64$	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions:	f_{SYS}	= 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock	f_{ADCI}	= f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time	t_S	= $t_{ADCI} \times 2$ = 100 ns

Conversion 10-bit:

$$t_{C10} = 13 \times t_{ADCI} + 2 \times t_{SYS} = 13 \times 50\ \text{ns} + 2 \times 12.5\ \text{ns} = 0.675\ \mu\text{s}$$

Conversion 8-bit:

$$t_{C8} = 11 \times t_{ADCI} + 2 \times t_{SYS} = 11 \times 50\ \text{ns} + 2 \times 12.5\ \text{ns} = 0.575\ \mu\text{s}$$

Converter Timing Example B:

Assumptions:	f_{SYS}	= 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock	f_{ADCI}	= f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time	t_S	= $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

$$t_{C10} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 75\ \text{ns} + 2 \times 25\ \text{ns} = 1.25\ \mu\text{s}$$

Conversion 8-bit:

$$t_{C8} = 14 \times t_{ADCI} + 2 \times t_{SYS} = 14 \times 75\ \text{ns} + 2 \times 25\ \text{ns} = 1.10\ \mu\text{s}$$

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization

3) f_{WU} in MHz

4) This value includes a hysteresis of approximately 50 mV for rising voltage.

5) V_{LV} = selected SWD voltage level

6) The limit V_{LV} - 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} - 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO}. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XC228xM is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSB} Timing Measurement

The time required for the transition from **Standby** to **Base** mode is called t_{SSB}. It is measured under the following conditions:

Precondition: The **Standby** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO}. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

Coding of bit fields LEVxV in SWD and PVC Configuration Registers

Table 21 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1]
000_B	0.95 V	
001_B	1.05 V	
010_B	1.15 V	
011_B	1.25 V	
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2]
110_B	1.55 V	
111_B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

Table 23 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{Er} SR	–	–	15 000	cycles	$t_{\mathrm{RET}} \geq 5$ years; Valid for up to 64 user-selected sectors (data storage)
		–	–	1 000	cycles	$t_{\mathrm{RET}} \geq 20$ years

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1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.

3) Value of IMB_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC228xM Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.6.5 External Bus Timing

The following parameters specify the behavior of the XC228xM bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Bus Interface Performance Limits

The output frequency at the bus interface pins is limited by the performance of the output drivers. The fast clock driver (used for CLKOUT) can drive 80-MHz signals, the standard drivers can drive 40-MHz signals

Therefore, the speed of the EBC must be limited, either by limiting the system frequency to $f_{SYS} \leq 80$ MHz or by adding waitstates so that signal transitions have a minimum distance of 12.5 ns.

For a description of the bus protocol and the programming of its variable timing parameters, please refer to the User's Manual.

Table 28 EBC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKOUT Cycle Time[1]	t_5 CC	–	$1 / f_{SYS}$	–	ns	
CLKOUT high time	t_6 CC	2	–	–		
CLKOUT low time	t_7 CC	2	–	–		
CLKOUT rise time	t_8 CC	–	–	3	ns	
CLKOUT fall time	t_9 CC	–	–	3		

[1] The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

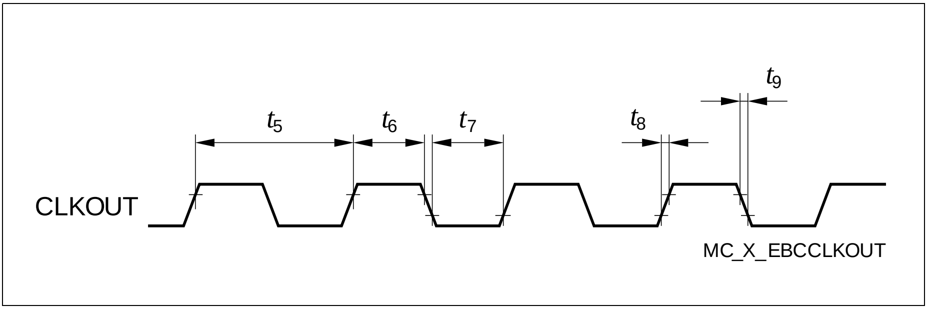

Figure 22 CLKOUT Signal Timing