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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

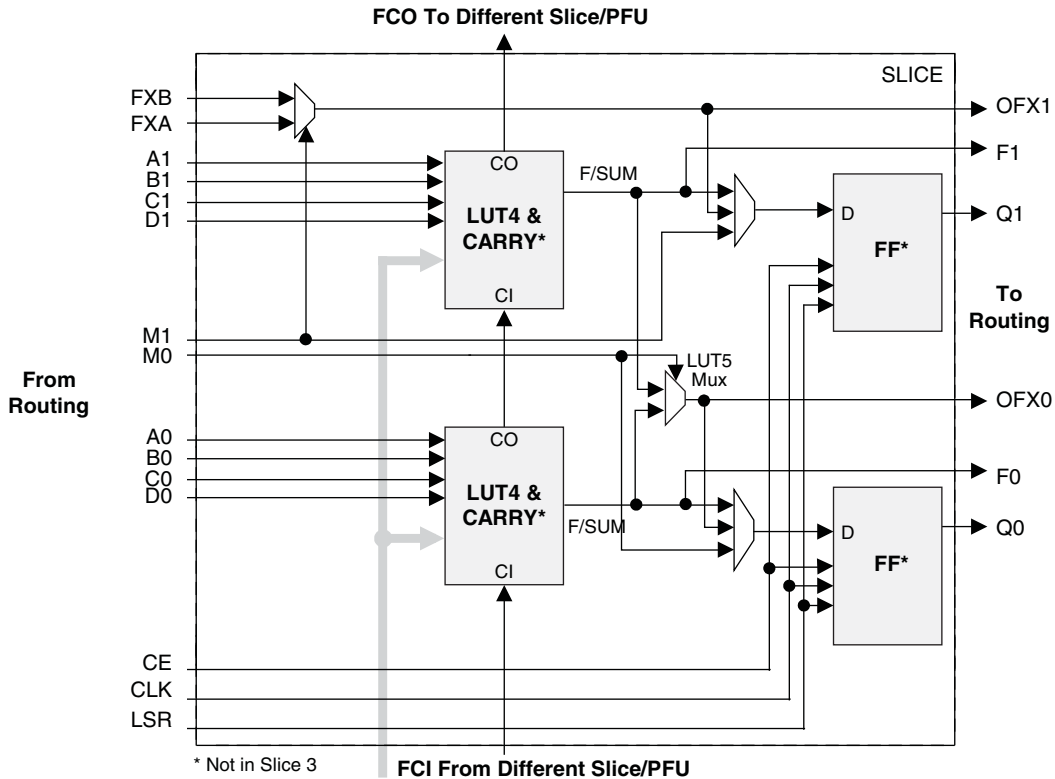
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn1156c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn1156c</a>

Figure 2-3. Slice Diagram



\* Not in Slice 3

For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:  
WCK is CLK  
WRE is from LSR  
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2  
WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in <sup>1</sup>
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output <sup>1</sup>

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

**Table 2-5. DLL Signals**

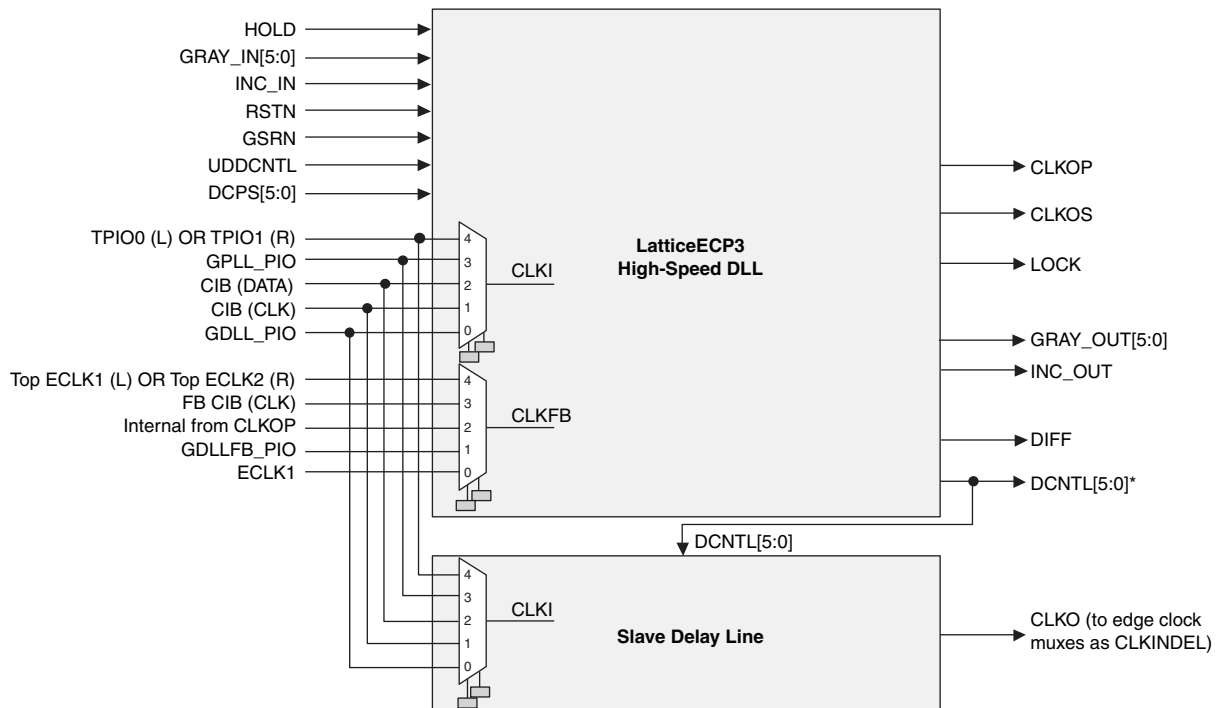
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#).

**Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line**



\* This signal is not user accessible. It can only be used to feed the slave delay line.

## Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

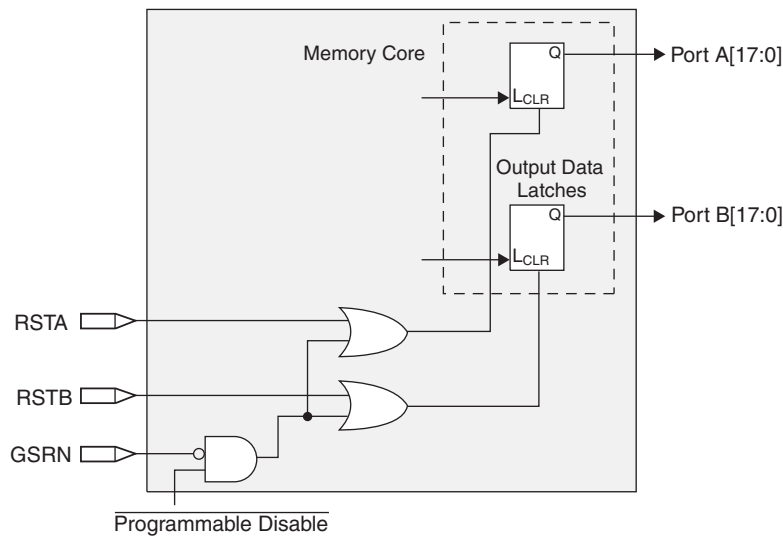
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

**Figure 2-22. Memory Core Reset**



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

## sysDSP™ Slice

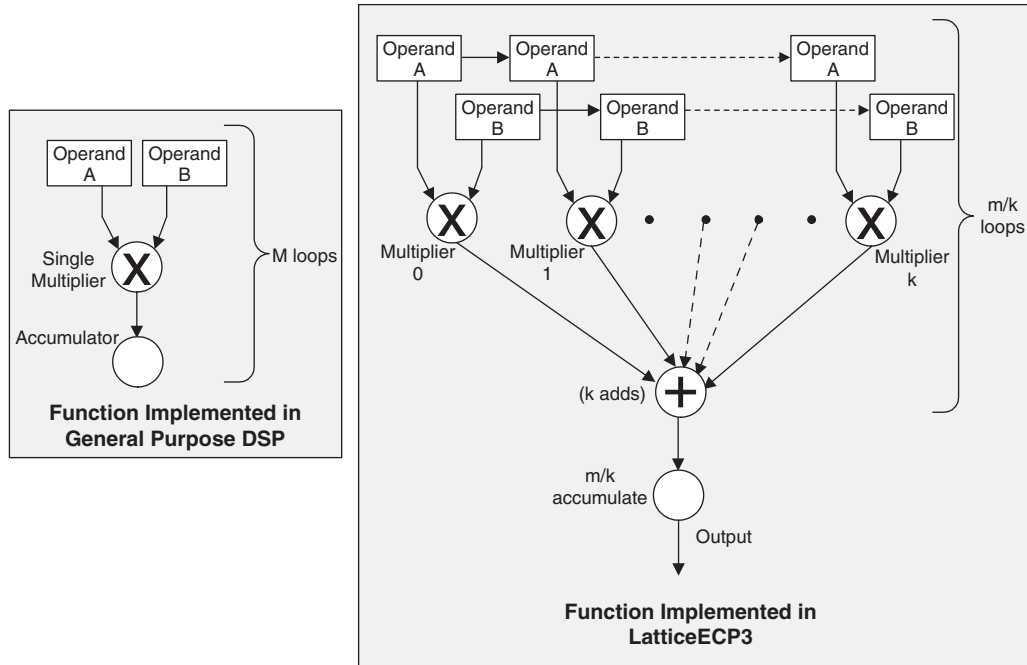
The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

**Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches**



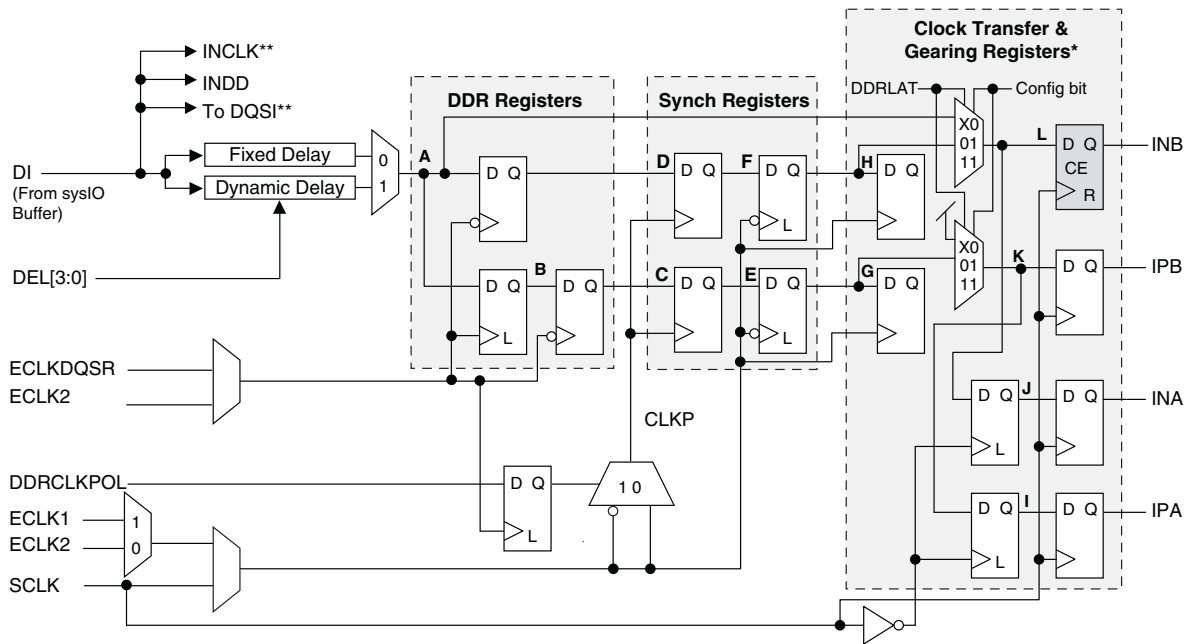
## LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multipliers per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multipliers feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

Figure 2-33. Input Register Block for Left, Right and Top Edges



\* Only on the left and right sides.  
 \*\* Selected PIO.  
 Note: Simplified diagram does not show CE/SET/REST details.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sys/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDR2 gearing of output logic. ODDR2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

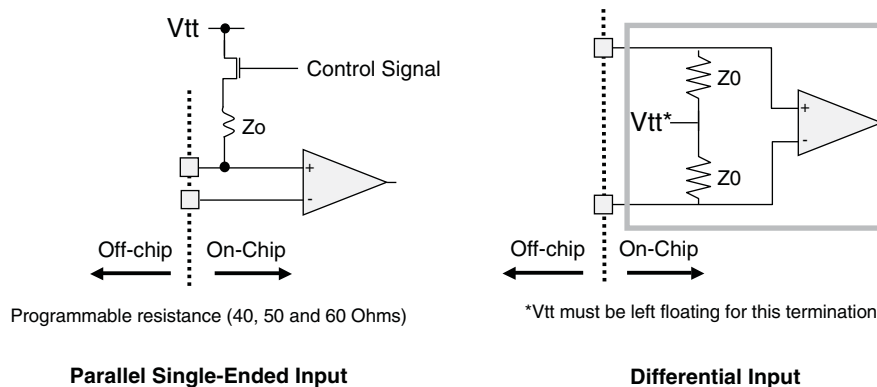
Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

## On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

**Figure 2-39. On-Chip Termination**



See Table 2-12 for termination options for input modes.

**Table 2-12. On-Chip Termination Options for Input Modes**

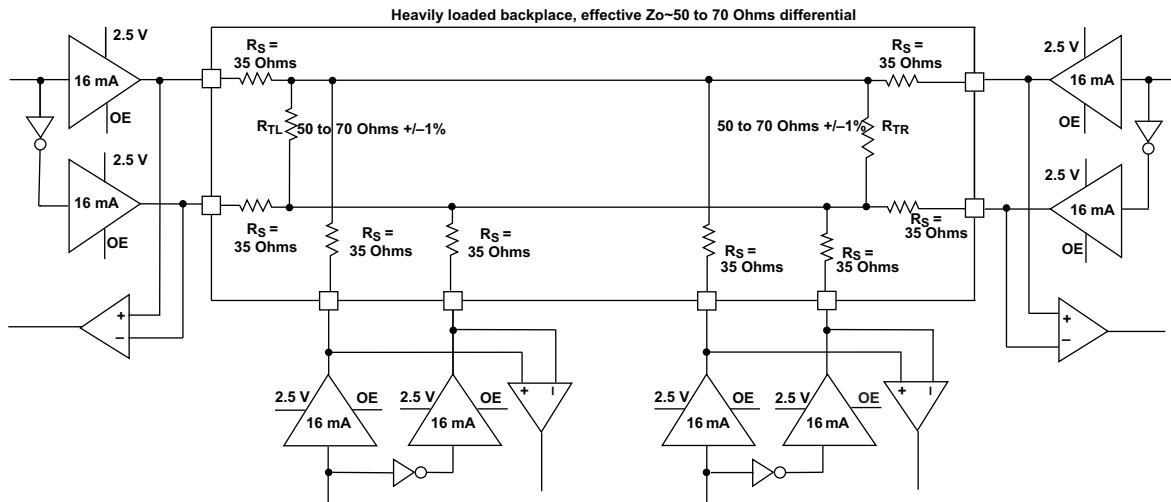
IO_TYPE	TERMINATE to VTT <sup>1,2</sup>	DIFFERENTIAL TERMINATION RESISTOR <sup>1</sup>
LVDS25	␣	80, 100, 120
BLVDS25	␣	80, 100, 120
MLVDS	␣	80, 100, 120
HSTL18_I	40, 50, 60	␣
HSTL18_II	40, 50, 60	␣
HSTL18D_I	40, 50, 60	␣
HSTL18D_II	40, 50, 60	␣
HSTL15_I	40, 50, 60	␣
HSTL15D_I	40, 50, 60	␣
SSTL25_I	40, 50, 60	␣
SSTL25_II	40, 50, 60	␣
SSTL25D_I	40, 50, 60	␣
SSTL25D_II	40, 50, 60	␣
SSTL18_I	40, 50, 60	␣
SSTL18_II	40, 50, 60	␣
SSTL18D_I	40, 50, 60	␣
SSTL18D_II	40, 50, 60	␣
SSTL15	40, 50, 60	␣
SSTL15D	40, 50, 60	␣

1. TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.  
Use of TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.  
On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.

### MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

**Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)**



**Table 3-5. MLVDS25 DC Conditions<sup>1</sup>**

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R <sub>TR</sub>	Receiver Termination (+/-1%)	50.00	70.00	Ω
V <sub>OH</sub>	Output High Voltage	1.52	1.60	V
V <sub>OL</sub>	Output Low Voltage	0.98	0.90	V
V <sub>OD</sub>	Output Differential Voltage	0.54	0.70	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.



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**Register-to-Register Performance<sup>1, 2, 3</sup>**

Function	-8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
3. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

**Derating Timing Tables**

Logic timing provided in the following sections of this data sheet and the Diamond and ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond and ispLEVER design tools can provide logic timing numbers at a particular temperature and voltage.

## LatticeECP3 Internal Switching Characteristics<sup>1, 2, 5</sup> (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory	0.141	—	0.145	—	0.149	—	ns
t <sub>SUCE_EBR</sub>	Clock Enable Setup Time to EBR Output Register	0.087	—	0.096	—	0.104	—	ns
t <sub>HCE_EBR</sub>	Clock Enable Hold Time to EBR Output Register	-0.066	—	-0.080	—	-0.094	—	ns
t <sub>SUBE_EBR</sub>	Byte Enable Set-Up Time to EBR Output Register	-0.071	—	-0.070	—	-0.068	—	ns
t <sub>HBE_EBR</sub>	Byte Enable Hold Time to EBR Output Register	0.118	—	0.098	—	0.077	—	ns
<b>DSP Block Timing<sup>3</sup></b>								
t <sub>SUI_DSP</sub>	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t <sub>HI_DSP</sub>	Input Register Hold Time	-0.17	—	-0.19	—	-0.21	—	ns
t <sub>SUP_DSP</sub>	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t <sub>HP_DSP</sub>	Pipeline Register Hold Time	-1.02	—	-1.09	—	-1.15	—	ns
t <sub>SUO_DSP</sub>	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t <sub>HO_DSP</sub>	Output Register Hold Time	-1.67	—	-1.76	—	-1.84	—	ns
t <sub>COI_DSP</sub>	Input Register Clock to Output Time	—	3.05	—	3.35	—	3.73	ns
t <sub>COP_DSP</sub>	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t <sub>COO_DSP</sub>	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t <sub>SUOPT_DSP</sub>	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t <sub>HOPT_DSP</sub>	Opcode Register Hold Time	-0.20	—	-0.24	—	-0.27	—	ns
t <sub>SUDATA_DSP</sub>	Cascade_data through ALU to Output Register Setup Time	1.69	—	1.94	—	2.14	—	ns
t <sub>HPDATA_DSP</sub>	Cascade_data through ALU to Output Register Hold Time	-0.58	—	-0.80	—	-0.97	—	ns

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

**LatticeECP3 Family Timing Adders<sup>1, 2, 3, 4, 5, 7</sup> (Continued)**
**Over Recommended Commercial Operating Conditions**

Buffer Type	Description	-8	-7	-6	Units
LVC MOS15_4mA	LVC MOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVC MOS15_8mA	LVC MOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVC MOS12_2mA	LVC MOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVC MOS12_6mA	LVC MOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVC MOS33_4mA	LVC MOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVC MOS33_8mA	LVC MOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVC MOS33_12mA	LVC MOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVC MOS33_16mA	LVC MOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVC MOS33_20mA	LVC MOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVC MOS25_4mA	LVC MOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVC MOS25_8mA	LVC MOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVC MOS25_12mA	LVC MOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVC MOS25_16mA	LVC MOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVC MOS25_20mA	LVC MOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVC MOS18_4mA	LVC MOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVC MOS18_8mA	LVC MOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVC MOS18_12mA	LVC MOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVC MOS18_16mA	LVC MOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVC MOS15_4mA	LVC MOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVC MOS15_8mA	LVC MOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVC MOS12_2mA	LVC MOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVC MOS12_6mA	LVC MOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	-0.12	-0.13	-0.14	ns

1. Timing adders are characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.
5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
6. This data does not apply to the LatticeECP3-17EA device.
7. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units	
f <sub>IN</sub>	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz	
			Primary clock <sup>4</sup>	2	—	420	MHz	
f <sub>OUT</sub>	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz	
			Primary clock <sup>4</sup>	4	—	420	MHz	
f <sub>OUT1</sub>	K-Divider output frequency	CLKOK		0.03125	—	250	MHz	
f <sub>OUT2</sub>	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz	
f <sub>VCO</sub>	PLL VCO frequency			500	—	1000	MHz	
f <sub>PDF</sub> <sup>3</sup>	Phase detector input frequency		Edge clock	2	—	500	MHz	
			Primary clock <sup>4</sup>	2	—	420	MHz	
<b>AC Characteristics</b>								
t <sub>PA</sub>	Programmable delay unit			65	130	260	ps	
t <sub>DT</sub>	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%	
			f <sub>OUT</sub> ≤ 250 MHz	Primary clock	45	50	55	%
			f <sub>OUT</sub> > 250 MHz	Primary clock	30	50	70	%
t <sub>CFA</sub>	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period	
t <sub>OPW</sub>	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns	
t <sub>OPJIT</sub> <sup>1</sup>	Output clock period jitter	f <sub>OUT</sub> ≥ 420 MHz		—	—	200	ps	
		420 MHz > f <sub>OUT</sub> ≥ 100 MHz		—	—	250	ps	
		f <sub>OUT</sub> < 100 MHz		—	—	0.025	UIPP	
t <sub>SK</sub>	Input clock to output clock skew when N/M = integer			—	—	500	ps	
t <sub>LOCK</sub> <sup>2</sup>	Lock time	2 to 25 MHz		—	—	200	us	
		25 to 500 MHz		—	—	50	us	
t <sub>UNLOCK</sub>	Reset to PLL unlock time to ensure fast reset			—	—	50	ns	
t <sub>HI</sub>	Input clock high time	90% to 90%		0.5	—	—	ns	
t <sub>LO</sub>	Input clock low time	10% to 10%		0.5	—	—	ns	
t <sub>IPJIT</sub>	Input clock period jitter			—	—	400	ps	
t <sub>RST</sub>	Reset signal pulse width high, RSTK			10	—	—	ns	
	Reset signal pulse width high, RST			500	—	—	ns	

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t<sub>LOCK</sub> for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for f<sub>PDF</sub> > 4 MHz. For f<sub>PDF</sub> < 4 MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for f<sub>PDF</sub> < 4 MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

## SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units	
RX-CID <sub>S</sub>	Stream of nontransitions <sup>1</sup> (CID = Consecutive Identical Digits) @ 10 <sup>-12</sup> BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
V <sub>RX-DIFF-S</sub>	Differential input sensitivity	150	—	1760	mV, p-p	
V <sub>RX-IN</sub>	Input levels	0	—	V <sub>CCA</sub> +0.5 <sup>4</sup>	V	
V <sub>RX-CM-DC</sub>	Input common mode range (DC coupled)	0.6	—	V <sub>CCA</sub>	V	
V <sub>RX-CM-AC</sub>	Input common mode range (AC coupled) <sup>3</sup>	0.1	—	V <sub>CCA</sub> +0.2	V	
T <sub>RX-RELOCK</sub>	SCDR re-lock time <sup>2</sup>	—	1000	—	Bits	
Z <sub>RX-TERM</sub>	Input termination 50/75 Ohm/High Z	-20%	50/75/HiZ	+20%	Ohms	
RL <sub>RX-RL</sub>	Return loss (without package)	10	—	—	dB	

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

### Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-14. Jitter Transfer – 3.125 Gbps

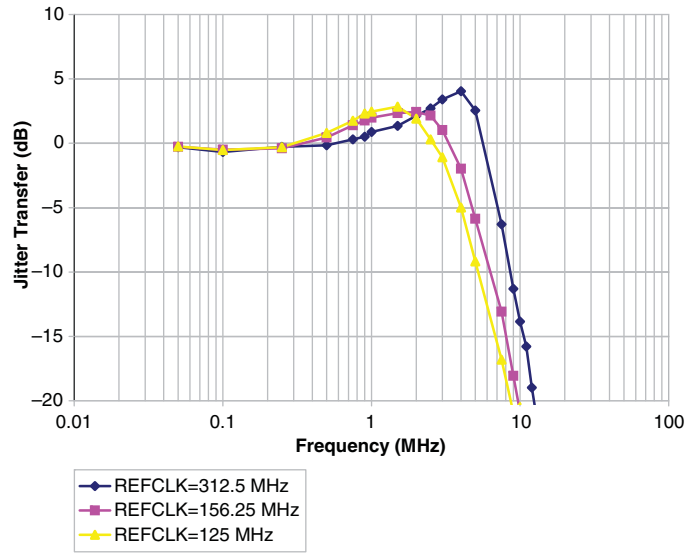
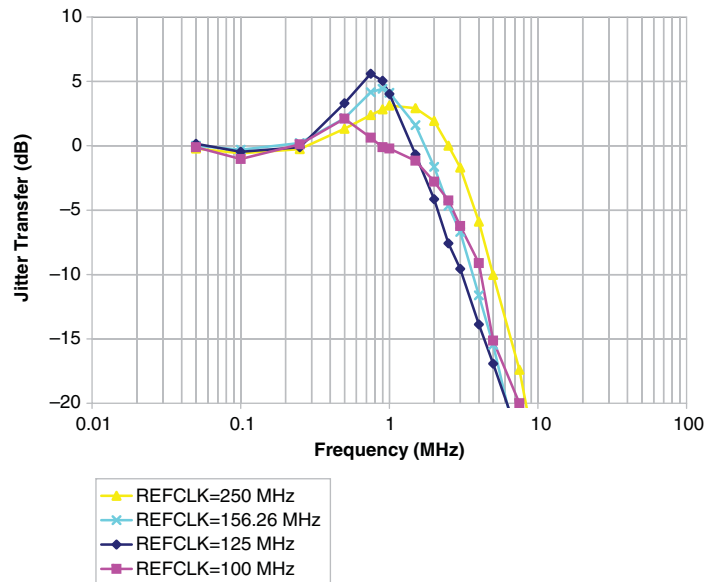


Figure 3-15. Jitter Transfer – 2.5 Gbps



## Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

### AC and DC Characteristics

**Table 3-17. Transmit**

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$T_{RF}$	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
$J_{TX\_DDJ}^{3,4,5}$	Output data deterministic jitter		—	—	0.10	UI
$J_{TX\_TJ}^{2,3,4,5}$	Total output data jitter		—	—	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pF load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

**Table 3-18. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$RL_{RX\_DIFF}$	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
$RL_{RX\_CM}$	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
$Z_{RX\_DIFF}$	Differential termination resistance		80	100	120	Ohms
$J_{RX\_DJ}^{1,2,3,4,5}$	Deterministic jitter tolerance (peak-to-peak)		—	—	0.34	UI
$J_{RX\_RJ}^{1,2,3,4,5}$	Random jitter tolerance (peak-to-peak)		—	—	0.26	UI
$J_{RX\_SJ}^{1,2,3,4,5}$	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.11	UI
$J_{RX\_TJ}^{1,2,3,4,5}$	Total jitter tolerance (peak-to-peak)		—	—	0.71	UI
$T_{RX\_EYE}$	Receiver eye opening		0.29	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

## LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

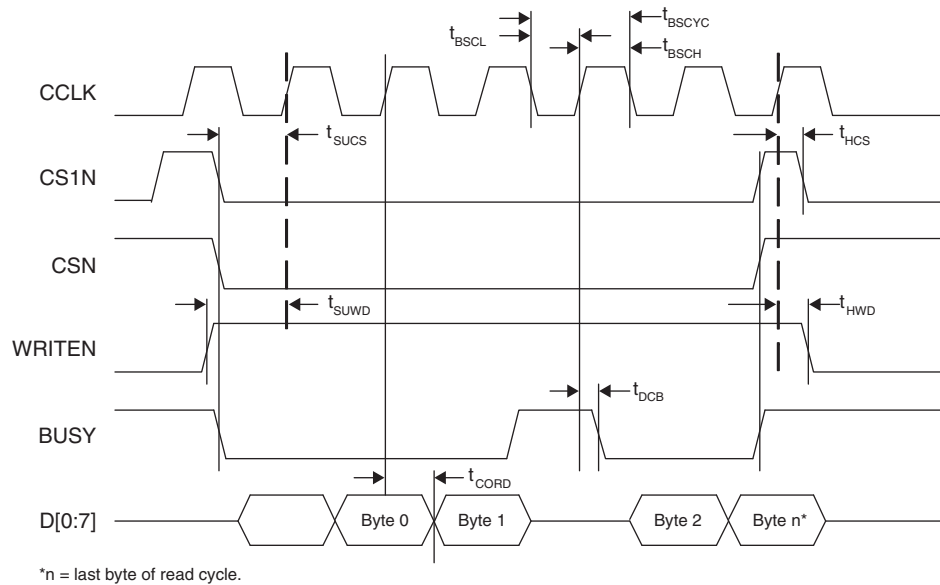
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$t_{SSCL}$	CCLK Minimum Low Pulse	5	—	ns
$t_{HLCH}$	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
$t_{CHHH}$	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
<b>Master and Slave SPI (Continued)</b>				
$t_{CHHL}$	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
$t_{HHCH}$	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
$t_{HLQZ}$	HOLDN to Output High-Z	—	9	ns
$t_{HHQX}$	HOLDN to Output Low-Z	—	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle





Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at [www.latticesemi.com](http://www.latticesemi.com).

- TN1169, [LatticeECP3 sysCONFIG Usage Guide](#)
- TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#)
- TN1177, [LatticeECP3 sysIO Usage Guide](#)
- TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#)
- TN1179, [LatticeECP3 Memory Usage Guide](#)
- TN1180, [LatticeECP3 High-Speed I/O Interface](#)
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- TN1182, [LatticeECP3 sysDSP Usage Guide](#)
- TN1184, [LatticeECP3 Soft Error Detection \(SED\) Usage Guide](#)
- TN1189, [LatticeECP3 Hardware Checklist](#)
- TN1215, [LatticeECP2MS and LatticeECP2S Devices](#)
- TN1216, [LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3](#)
- TN1222, [LatticeECP3 Slave SPI Port User's Guide](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): [www.jedec.org](http://www.jedec.org)
- PCI: [www.pcisig.com](http://www.pcisig.com)

Date	Version	Section	Change Summary
			<p>LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.</p> <p>Updated SERDES External Reference Clock Waveforms.</p> <p>Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break-down table.</p>
		Pinout Information	<p>“Logic Signal Connections” section heading renamed “Package Pinout Information”. Software menu selections within this section have been updated.</p> <p>Signal Descriptions table – Updated description for V<sub>CCA</sub> signal.</p>
April 2012	02.2EA	Architecture	<p>Updated first paragraph of Output Register Block section.</p> <p>Updated the information about sysIO buffer pairs below Figure 2-38.</p> <p>Updated the information relating to migration between devices in the Density Shifting section.</p>
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for t <sub>RST</sub> .
		Ordering Information	Updated topside marks with new logos in the Ordering Information section.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	<p>Updated LatticeECP3 Supply Current table power numbers.</p> <p>Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.</p>
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	<p>Added information for LatticeECP3-17EA, 328-ball csBGA package.</p> <p>Added ordering information for low power devices and -9 speed grade devices.</p>
July 2011	01.9EA	DC and Switching Characteristics	<p>Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.</p> <p>sysCLOCK PLL Timing table, added footnote 4.</p> <p>External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.</p>
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP3-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	<p>Added data for 150 Mbps to SERDES Power Supply Requirements table.</p> <p>Updated Frequencies in Table 3-6 Serial Output Timing and Levels</p> <p>Added Data for 150 Mbps to Table 3-7 Channel Output Jitter</p> <p>Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, t<sub>JIT</sub>.</p> <p>Corrected Internal Switching Characteristics table, Description for EBR Timing, t<sub>SUWREN_EBR</sub> and t<sub>HWREN_EBR</sub>.</p> <p>Added footnote 1 to sysConfig Port Timing Specifications table.</p> <p>Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications</p>

Date	Version	Section	Change Summary
			Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification
December 2010	01.7EA	Multiple	Data sheet made final. Removed “preliminary” headings.
			Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices.
			Updated for Lattice Diamond design software.
		Introduction	Corrected number of user I/Os
		Architecture	Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices.
			Updated description of General Purpose PLL
			Added additional information in the Flexible Quad SERDES Architecture section.
			Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal).
			Updated Figure 2-16, Per Region Secondary Clock Selection.
			Updated description for On-Chip Programmable Termination.
			Added information about number of rows of DSP slices.
			Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes.
			Updated information for sysIO buffer pairs.
			Corrected minimum number of General Purpose PLLs (was 4, now 2).
			DC and Switching Characteristics
		Added $t_{V}$ (clock pulse width) in External Switching Characteristics table.	
		Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table.	
		Added Jitter Transfer figures in SERDES External Reference Clock section.	
		Corrected capacitance information in the DC Electrical Characteristics table.	
		Corrected data in the Register-to-Register Performance table.	
		Corrected GDDR Parameter name HOGDDR.	
		Corrected RSDS25 -7 data in Family Timing Adders table.	
		Added footnotes 10-12 to DDR data information in the External Switching Characteristics table.	
		Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDR2 Parameters).	
		Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differential Signaling)) and 3-6 (Generic DDRX1/DDR2 (With Clock and Data Edges Aligned)).	
		Updated Supply Current table.	
		Added GDDR interface information to the External Switching and Characteristics table.	
		Added footnote to sysIO Recommended Operating Conditions table.	
		Added footnote to LVDS25 table.	
		Corrected DDR section footnotes and references.	
		Corrected Hot Socketing support from “top and bottom banks” to “top and bottom I/O pins”.	
		Pinout Information	Updated description for VTTx.

Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
		Updated Device Configuration text section.	
		Corrected software default value of MCCLK to be 2.5 MHz.	
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
		Corrected footnote 2 in sysIO Recommended Operating Conditions table.	
		Added added footnote 7 for $t_{\text{SKEW\_PRIB}}$ to External Switching Characteristics table.	
		Added 2-to-1 Gearing text section and table.	
		Updated External Reference Clock Specification (refclkp/refclkn) table.	
		LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{\text{DINIT}}$ information.	
		Added sysCONFIG Port Timing waveform.	
		Serial Input Data Specifications table, delete Typ data for $V_{\text{RX-DIFF-S}}$ .	
		Added footnote 4 to sysCLOCK PLL Timing table for $t_{\text{PFD}}$ .	
		Added SERDES/PCS Block Latency Breakdown table.	
		External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.	
		Added SERDES External Reference Clock Waveforms.	
		Updated Serial Output Timing and Levels table.	
		Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".	
		Updated timing information	
		Updated SERDES minimum frequency.	
		Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.	
Updated Serial Input Data Specifications table.			
Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.			
Pinout Information	Updated Signal Description tables.		
Updated Pin Information Summary tables and added footnote 1.			
February 2009	01.0	—	Initial release.