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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Obsolete
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn1156ctw">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn1156ctw</a>

## PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

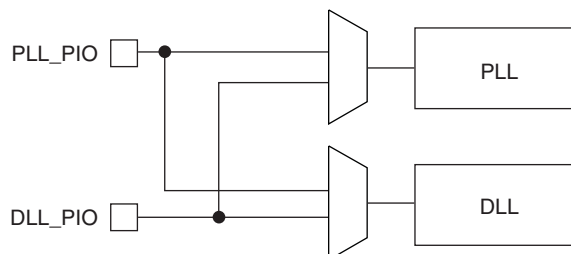
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

## PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

**Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices**



Note: Not every PLL has an associated DLL.

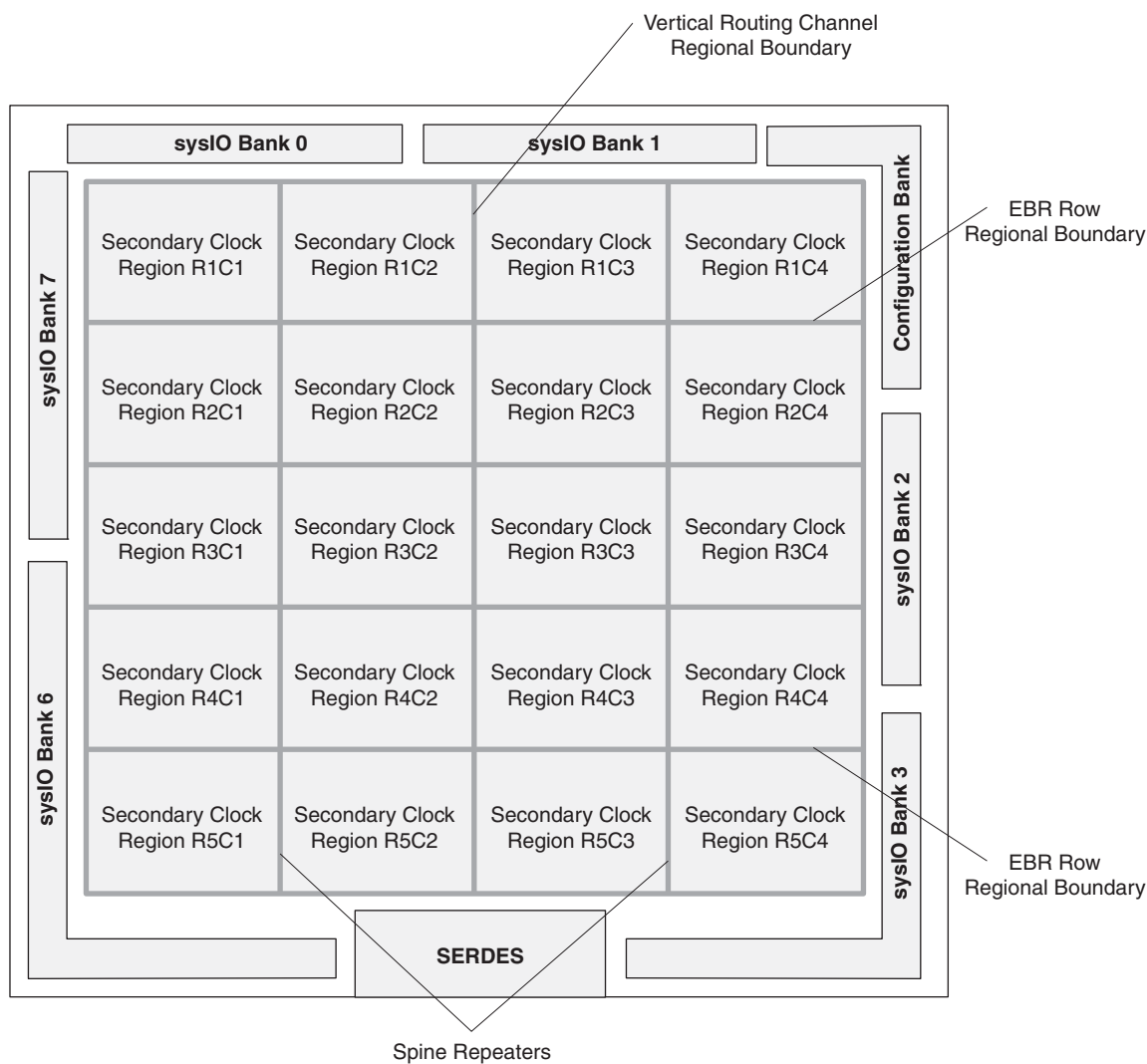
## Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a  $\div 2$ ,  $\div 4$  or  $\div 8$  mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#). Figure 2-8 shows the clock divider connections.

**Table 2-6. Secondary Clock Regions**

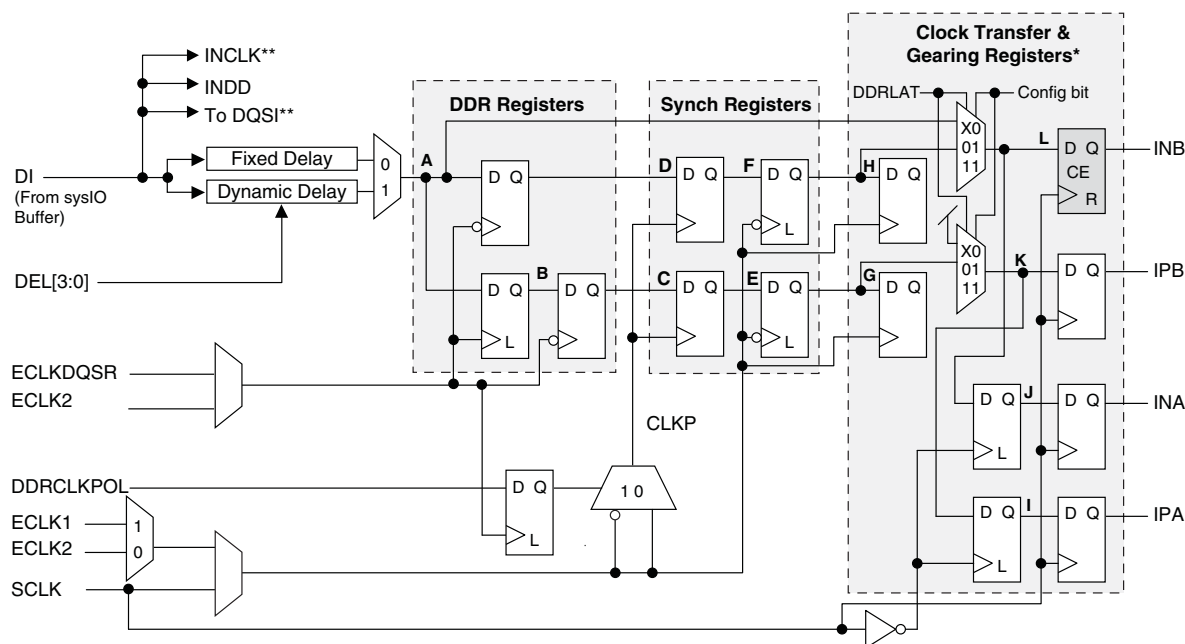
Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

**Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions**





**Figure 2-33. Input Register Block for Left, Right and Top Edges**



\* Only on the left and right sides.  
\*\* Selected PIO.  
Note: Simplified diagram does not show CE/SET/REST details.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDR2 gearing of output logic. ODDR2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

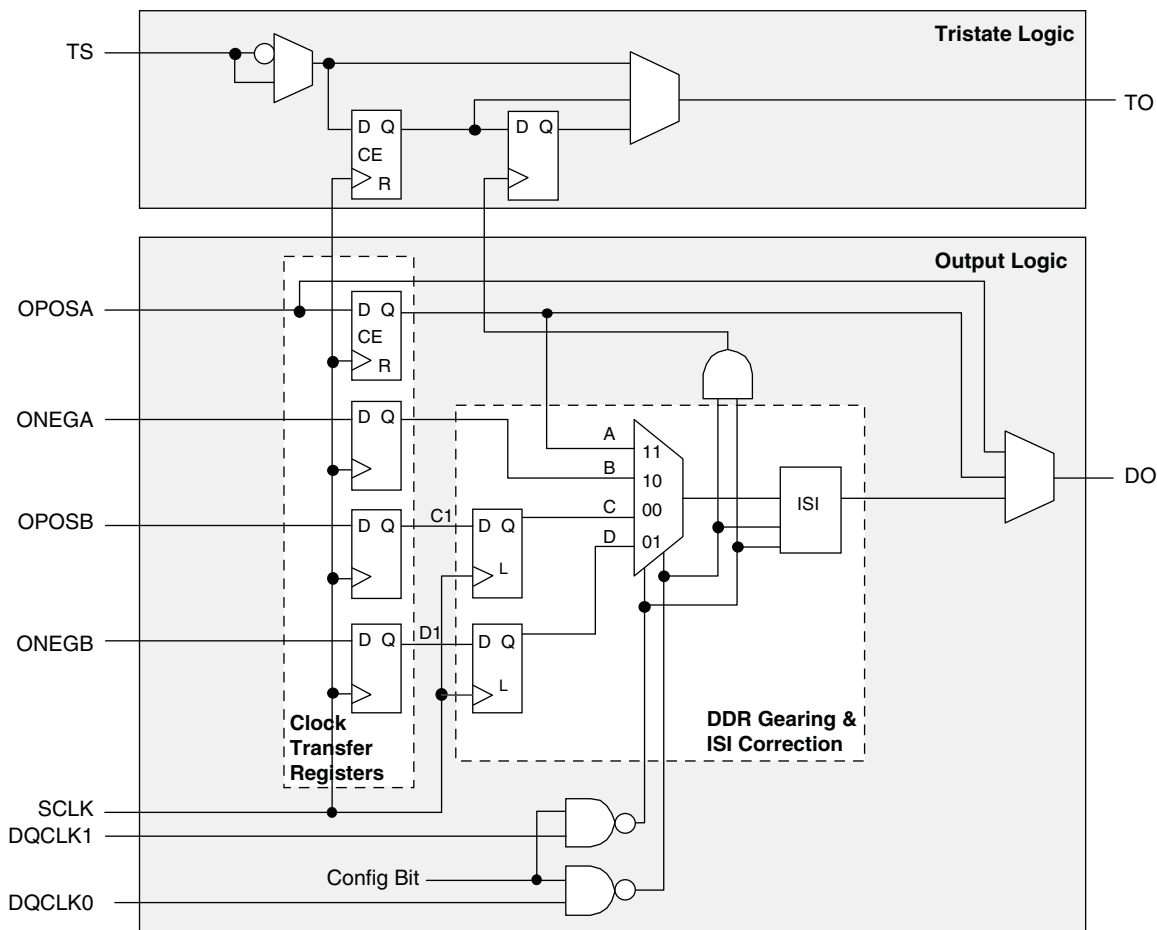
A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

**Figure 2-34. Output and Tristate Block for Left and Right Edges**



## Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

## ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

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**2. Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

**3. Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**

The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

**Typical sysI/O I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO8}$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The  $V_{CC}$  and  $V_{CCAUX}$  supply the power to the FPGA core fabric, whereas the  $V_{CCIO}$  supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric.  $V_{CCIO}$  supplies should be powered-up before or together with the  $V_{CC}$  and  $V_{CCAUX}$  supplies.

**Supported sysI/O Standards**

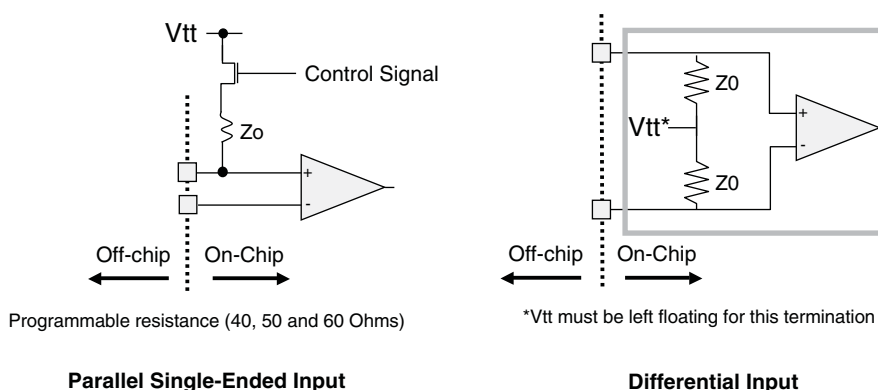
The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, [LatticeECP3 sysIO Usage Guide](#).

## On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

**Figure 2-39. On-Chip Termination**



See Table 2-12 for termination options for input modes.

**Table 2-12. On-Chip Termination Options for Input Modes**

IO_TYPE	TERMINATE to VTT <sup>1,2</sup>	DIFFERENTIAL TERMINATION RESISTOR <sup>1</sup>
LVDS25	p	80, 100, 120
BLVDS25	p	80, 100, 120
MLVDS	p	80, 100, 120
HSTL18_I	40, 50, 60	p
HSTL18_II	40, 50, 60	p
HSTL18D_I	40, 50, 60	p
HSTL18D_II	40, 50, 60	p
HSTL15_I	40, 50, 60	p
HSTL15D_I	40, 50, 60	p
SSTL25_I	40, 50, 60	p
SSTL25_II	40, 50, 60	p
SSTL25D_I	40, 50, 60	p
SSTL25D_II	40, 50, 60	p
SSTL18_I	40, 50, 60	p
SSTL18_II	40, 50, 60	p
SSTL18D_I	40, 50, 60	p
SSTL18D_II	40, 50, 60	p
SSTL15	40, 50, 60	p
SSTL15D	40, 50, 60	p

1. TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.  
Use of TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.  
On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.



**Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)**

MCCLK (MHz)	MCCLK (MHz)
	10
2.5 <sup>1</sup>	13
4.3	15 <sup>2</sup>
5.4	20
6.9	26
8.1	33 <sup>3</sup>
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

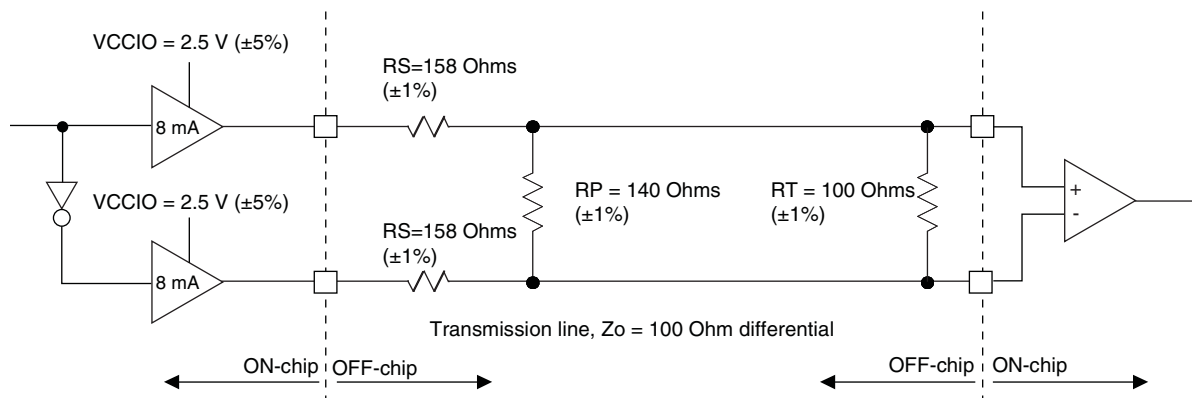
## Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the [LatticeECP3 Pin Migration Tables](#) and Diamond software for specific restrictions and limitations.

### LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

**Figure 3-1. LVDS25E Output Termination Example**



**Table 3-1. LVDS25E DC Conditions**

Parameter	Description	Typical	Units
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	V
Z <sub>OUT</sub>	Driver Impedance	20	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	158	Ω
R <sub>P</sub>	Driver Parallel Resistor (+/-1%)	140	Ω
R <sub>T</sub>	Receiver Termination (+/-1%)	100	Ω
V <sub>OH</sub>	Output High Voltage	1.43	V
V <sub>OL</sub>	Output Low Voltage	1.07	V
V <sub>OD</sub>	Output Differential Voltage	0.35	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	V
Z <sub>BACK</sub>	Back Impedance	100.5	Ω
I <sub>DC</sub>	DC Output Current	6.03	mA

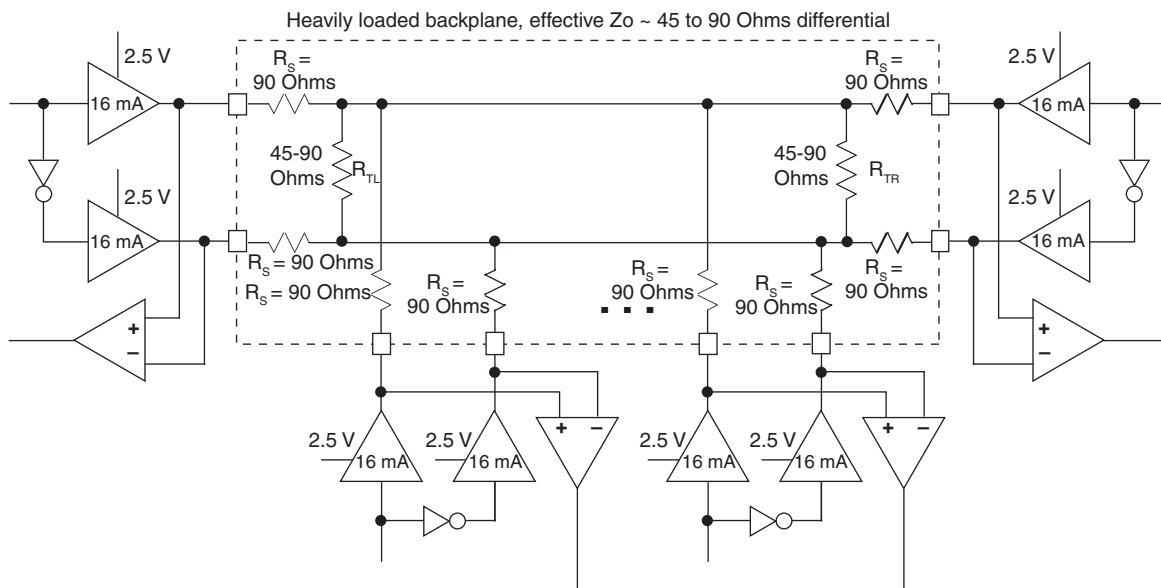
### LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V<sub>CCIO</sub>. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

### BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

**Figure 3-2. BLVDS25 Multi-point Output Example**



**Table 3-2. BLVDS25 DC Conditions<sup>1</sup>**

#### Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V <sub>CCIO</sub>	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R <sub>TR</sub>	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V <sub>OH</sub>	Output High Voltage	1.38	1.48	V
V <sub>OL</sub>	Output Low Voltage	1.12	1.02	V
V <sub>OD</sub>	Output Differential Voltage	0.25	0.46	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

# LatticeECP3 External Switching Characteristics (Continued)<sup>1, 2, 3, 13</sup>

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDR2_RX.ECLK.Aligned) (No CLKDIV)									
Left and Right Sides Using DLLCLKPIN for Clock Input									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR2_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left and Right Sides									
t <sub>SUGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDR2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDR1_TX.SCLK.Centered) <sup>10</sup>									
t <sub>DVBGDDR</sub>	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t <sub>DVAGDDR</sub>	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f <sub>MAX_GDDR</sub>	DDR1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t <sub>DVBGDDR</sub>	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
t <sub>DVAGDDR</sub>	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

**LatticeECP3 Family Timing Adders<sup>1, 2, 3, 4, 5, 7</sup> (Continued)**
**Over Recommended Commercial Operating Conditions**

Buffer Type	Description	–8	–7	–6	Units
LVC MOS15_4mA	LVC MOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVC MOS15_8mA	LVC MOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVC MOS12_2mA	LVC MOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVC MOS12_6mA	LVC MOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVC MOS33_4mA	LVC MOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVC MOS33_8mA	LVC MOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVC MOS33_12mA	LVC MOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVC MOS33_16mA	LVC MOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVC MOS33_20mA	LVC MOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVC MOS25_4mA	LVC MOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVC MOS25_8mA	LVC MOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVC MOS25_12mA	LVC MOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVC MOS25_16mA	LVC MOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVC MOS25_20mA	LVC MOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVC MOS18_4mA	LVC MOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVC MOS18_8mA	LVC MOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVC MOS18_12mA	LVC MOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVC MOS18_16mA	LVC MOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVC MOS15_4mA	LVC MOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVC MOS15_8mA	LVC MOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVC MOS12_2mA	LVC MOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVC MOS12_6mA	LVC MOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	–0.12	–0.13	–0.14	ns

1. Timing adders are characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.
5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
6. This data does not apply to the LatticeECP3-17EA device.
7. For details on –9 speed grade devices, please contact your Lattice Sales Representative.

### sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f <sub>IN</sub>	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock <sup>4</sup>	2	—	420	MHz
f <sub>OUT</sub>	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock <sup>4</sup>	4	—	420	MHz
f <sub>OUT1</sub>	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f <sub>OUT2</sub>	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f <sub>VCO</sub>	PLL VCO frequency			500	—	1000	MHz
f <sub>PFD</sub> <sup>3</sup>	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock <sup>4</sup>	2	—	420	MHz
AC Characteristics							
t <sub>PA</sub>	Programmable delay unit			65	130	260	ps
t <sub>DT</sub>	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		f <sub>OUT</sub> ≤ 250 MHz	Primary clock	45	50	55	%
		f <sub>OUT</sub> > 250 MHz	Primary clock	30	50	70	%
t <sub>CPA</sub>	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t <sub>OPW</sub>	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t <sub>OPJIT</sub> <sup>1</sup>	Output clock period jitter	f <sub>OUT</sub> ≥ 420 MHz		—	—	200	ps
		420 MHz > f <sub>OUT</sub> ≥ 100 MHz		—	—	250	ps
		f <sub>OUT</sub> < 100 MHz		—	—	0.025	UIPP
t <sub>SK</sub>	Input clock to output clock skew when N/M = integer			—	—	500	ps
t <sub>LOCK</sub> <sup>2</sup>	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t <sub>UNLOCK</sub>	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t <sub>HI</sub>	Input clock high time	90% to 90%		0.5	—	—	ns
t <sub>LO</sub>	Input clock low time	10% to 10%		0.5	—	—	ns
t <sub>IPJIT</sub>	Input clock period jitter			—	—	400	ps
t <sub>RST</sub>	Reset signal pulse width high, RSTK			10	—	—	ns
	Reset signal pulse width high, RST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 4$  MHz. For  $f_{PFD} < 4$  MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for  $f_{PFD} < 4$  MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

## SERDES High-Speed Data Transmitter<sup>1</sup>

**Table 3-6. Serial Output Timing and Levels**

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64 V setting) <sup>1,2</sup>	0.15 to 3.125 Gbps	480	640	800	mV, p-p
$V_{OCM}$	Output common mode voltage	—	$V_{CCOB} - 0.75$	$V_{CCOB} - 0.60$	$V_{CCOB} - 0.45$	V
$T_{TX-R}$	Rise time (20% to 80%)	—	145	185	265	ps
$T_{TX-F}$	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/Hi Z	+20%	Ohms
$R_{LTX-RL}$	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}^3$	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 Ohm impedance.

2. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for actual binary settings and the min-max range.

3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

## Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

### AC and DC Characteristics

**Table 3-17. Transmit**

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$T_{RF}$	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
$J_{TX\_DDJ}^{3,4,5}$	Output data deterministic jitter		—	—	0.10	UI
$J_{TX\_TJ}^{2,3,4,5}$	Total output data jitter		—	—	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pF load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

**Table 3-18. Receive and Jitter Tolerance**

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$RL_{RX\_DIFF}$	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
$RL_{RX\_CM}$	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
$Z_{RX\_DIFF}$	Differential termination resistance		80	100	120	Ohms
$J_{RX\_DJ}^{1,2,3,4,5}$	Deterministic jitter tolerance (peak-to-peak)		—	—	0.34	UI
$J_{RX\_RJ}^{1,2,3,4,5}$	Random jitter tolerance (peak-to-peak)		—	—	0.26	UI
$J_{RX\_SJ}^{1,2,3,4,5}$	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.11	UI
$J_{RX\_TJ}^{1,2,3,4,5}$	Total jitter tolerance (peak-to-peak)		—	—	0.71	UI
$T_{RX\_EYE}$	Receiver eye opening		0.29	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.



## LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

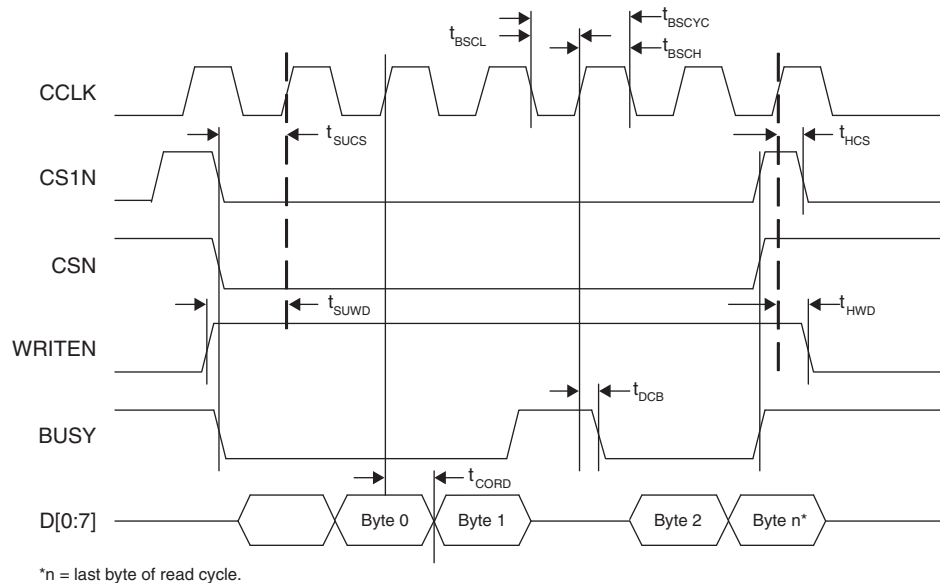
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$t_{SSCL}$	CCLK Minimum Low Pulse	5	—	ns
$t_{HLCH}$	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
$t_{CHHH}$	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
<b>Master and Slave SPI (Continued)</b>				
$t_{CHHL}$	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
$t_{HHCH}$	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
$t_{HLQZ}$	HOLDN to Output High-Z	—	9	ns
$t_{HHQX}$	HOLDN to Output Low-Z	—	9	ns

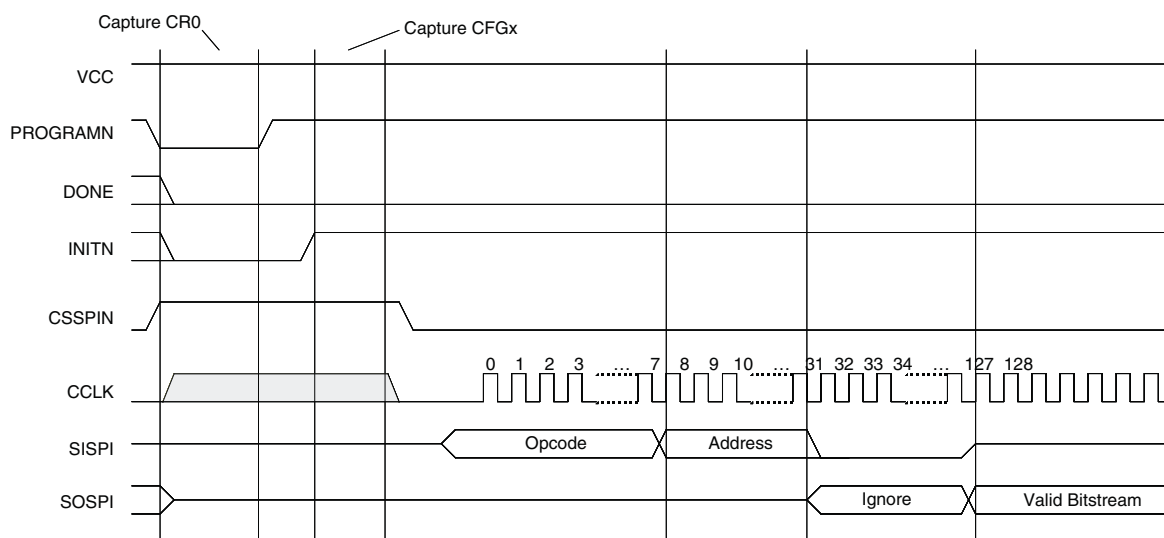
1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

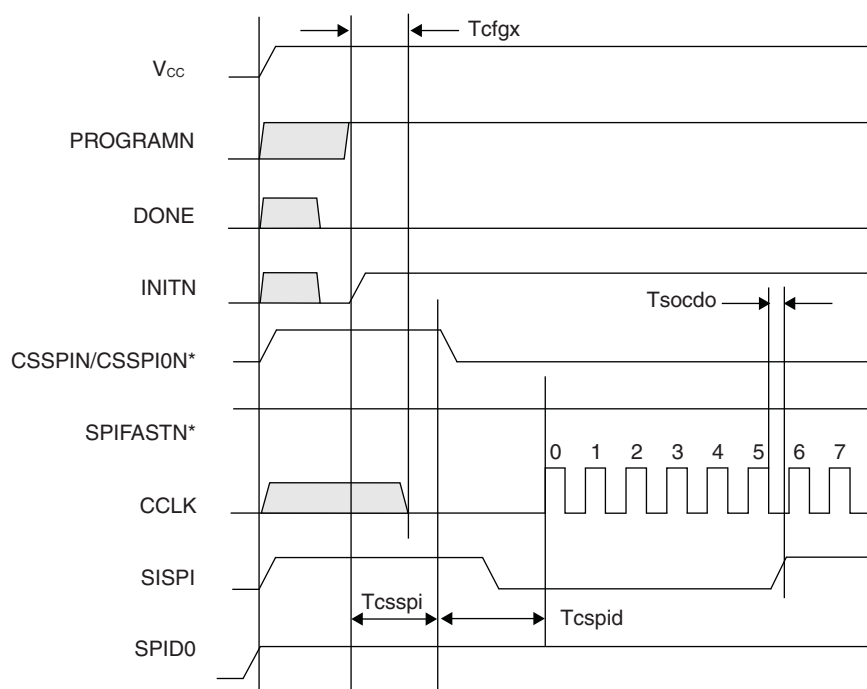
**Figure 3-20. sysCONFIG Parallel Port Read Cycle**



**Figure 3-28. Master SPI Configuration Waveforms**



**Figure 3-29. Master SPI POR Waveforms**

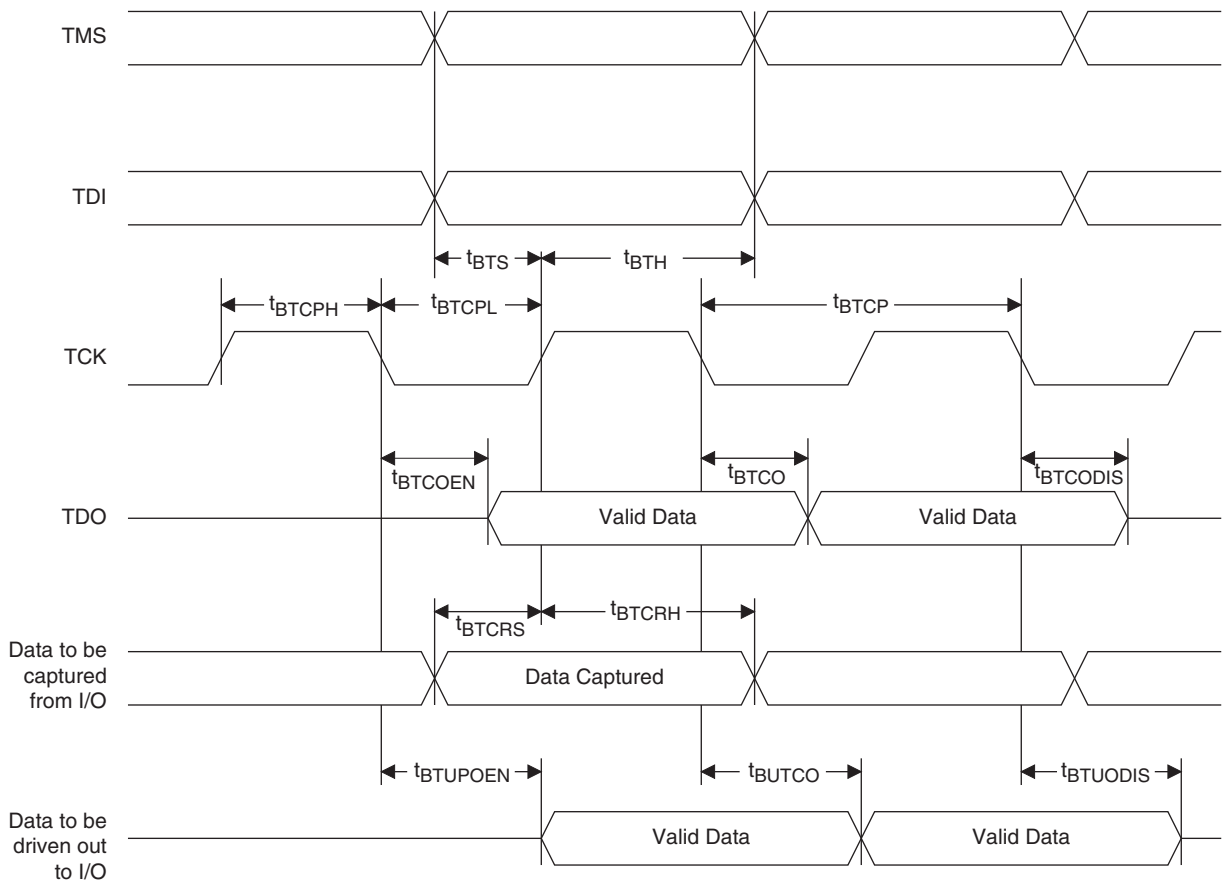


## JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$f_{\text{MAX}}$	TCK clock frequency	—	25	MHz
$t_{\text{BTCP}}$	TCK [BSCAN] clock pulse width	40	—	ns
$t_{\text{BTCPH}}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{\text{BTCPL}}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{\text{BTS}}$	TCK [BSCAN] setup time	10	—	ns
$t_{\text{BTH}}$	TCK [BSCAN] hold time	8	—	ns
$t_{\text{BTRF}}$	TCK [BSCAN] rise/fall time	50	—	mV/ns
$t_{\text{BTCO}}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{\text{BTCODIS}}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{\text{BTCOEN}}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{\text{BTCRS}}$	BSCAN test capture register setup time	8	—	ns
$t_{\text{BTCRH}}$	BSCAN test capture register hold time	25	—	ns
$t_{\text{BUTCO}}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{\text{BTUODIS}}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{\text{BTUPOEN}}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-32. JTAG Port Timing Waveforms



## Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank <sup>2</sup>	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.

2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

### For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at [www.latticesemi.com](http://www.latticesemi.com).

- TN1169, [LatticeECP3 sysCONFIG Usage Guide](#)
- TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#)
- TN1177, [LatticeECP3 sysIO Usage Guide](#)
- TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#)
- TN1179, [LatticeECP3 Memory Usage Guide](#)
- TN1180, [LatticeECP3 High-Speed I/O Interface](#)
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- TN1182, [LatticeECP3 sysDSP Usage Guide](#)
- TN1184, [LatticeECP3 Soft Error Detection \(SED\) Usage Guide](#)
- TN1189, [LatticeECP3 Hardware Checklist](#)
- TN1215, [LatticeECP2MS and LatticeECP2S Devices](#)
- TN1216, [LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3](#)
- TN1222, [LatticeECP3 Slave SPI Port User's Guide](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): [www.jedec.org](http://www.jedec.org)
- PCI: [www.pcisig.com](http://www.pcisig.com)