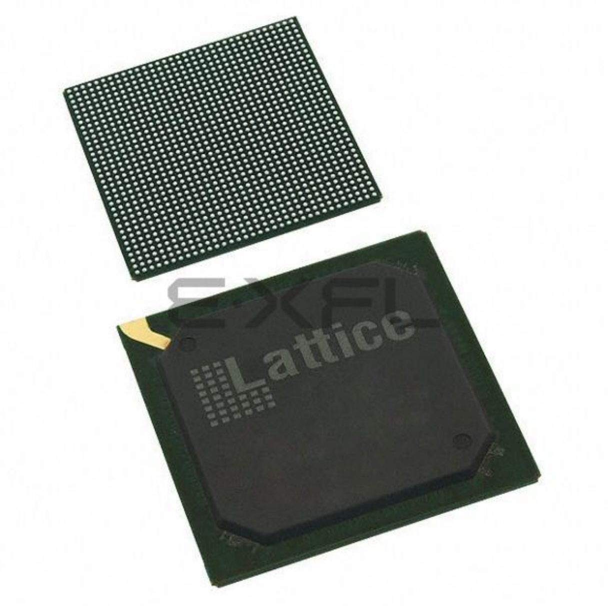
# Lattice Semiconductor Corporation - LFE3-150EA-6FN1156ITW Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 18625 |
| Number of Logic Elements/Cells | 149000 |
| Total RAM Bits | 7014400 |
| Number of I/O | 586 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1156-BBGA |
| Supplier Device Package | 1156-FPBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn1156itw |

# LatticeECP3 Family Data Sheet
# Architecture

**June 2013** **Data Sheet DS1021**

## Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

***Table 2-3. Number of Slices Required to Implement Distributed RAM***

| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

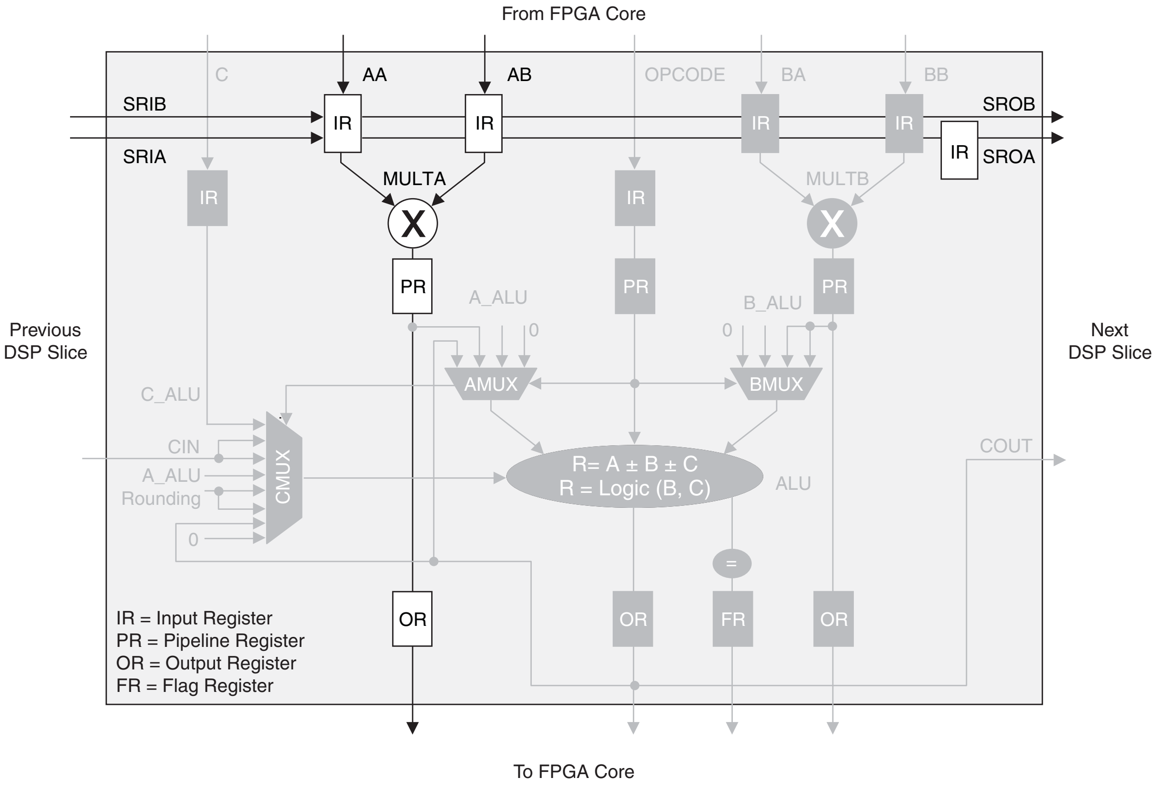
Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

## MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

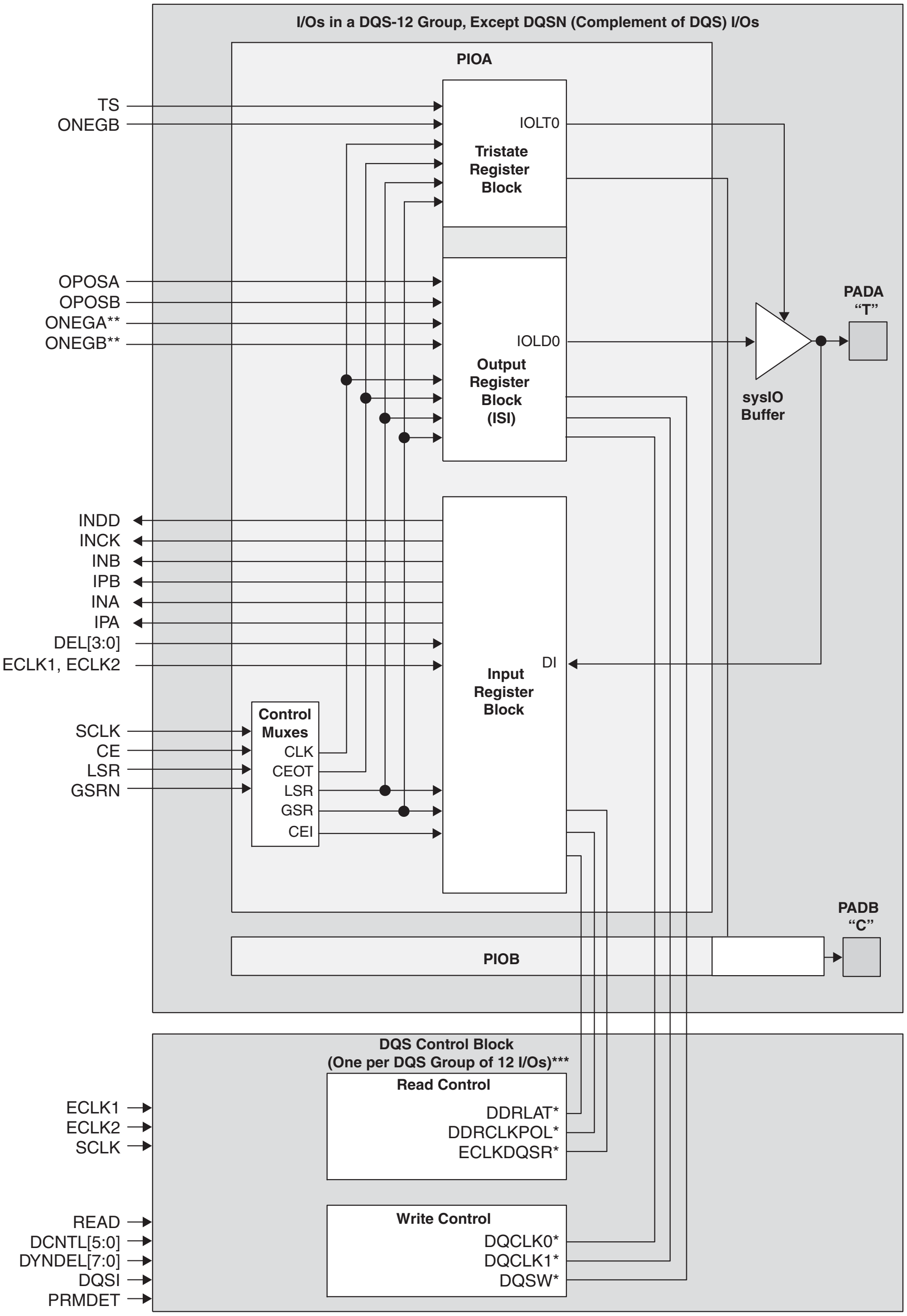
*Figure 2-26. MULT sysDSP Element*



## Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

***Figure 2-32. PIC Diagram***



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-30 provides further information on the use of the gearbox function.

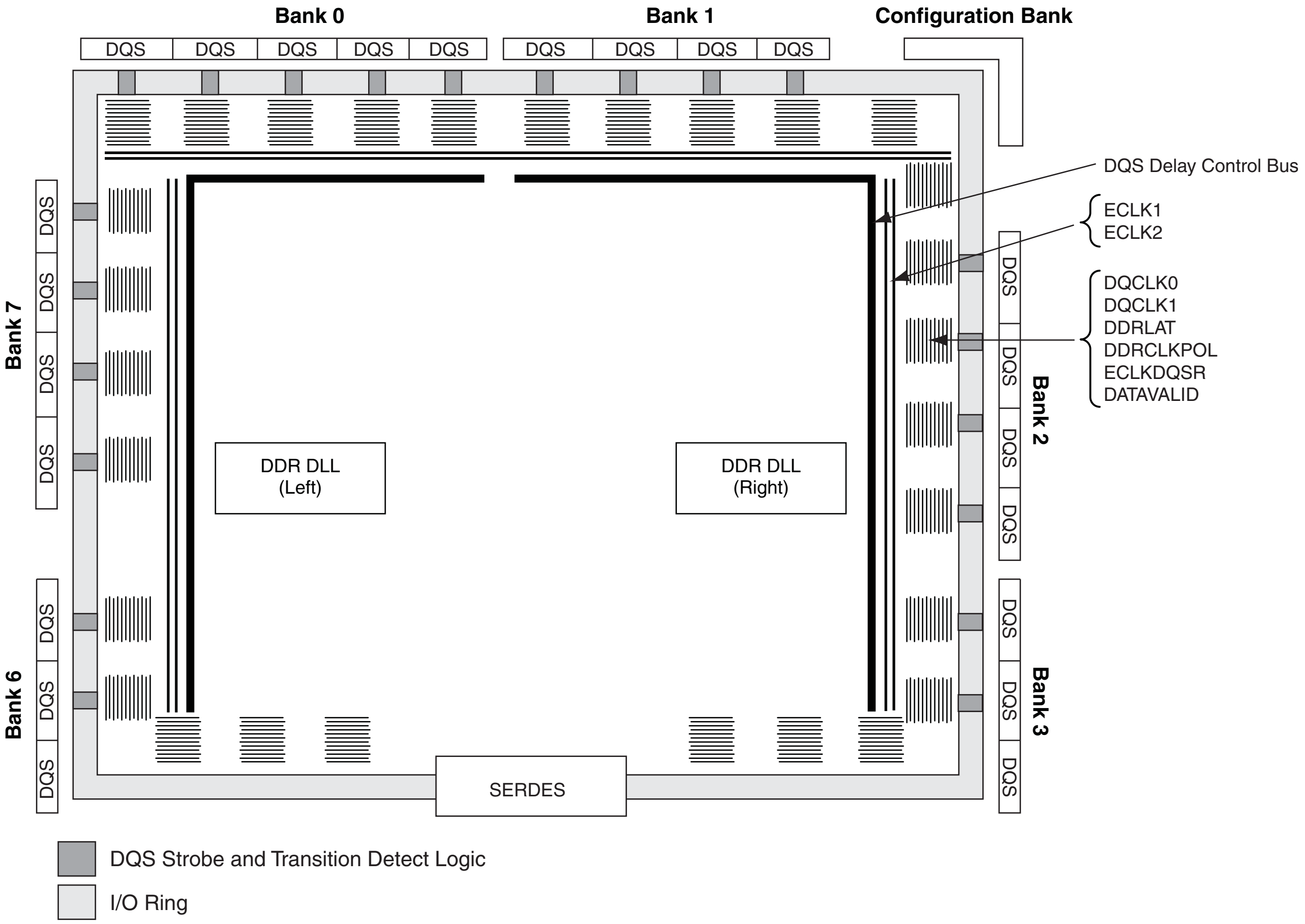
The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-37 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

*Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution*



*Includes shared configuration I/Os and dedicated configuration I/Os.

Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

### Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

### Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

## SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel ÷1, ÷2 and ÷11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.

# LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical | | Units |
|---|---|---|---|---|---|
| | | | **–6L, –7L, –8L** | **–6, –7, –8** | |
| $I_{CC}$ | Core Power Supply Current | ECP-17EA | 29.8 | 49.4 | mA |
| | | ECP3-35EA | 53.7 | 89.4 | mA |
| | | ECP3-70EA | 137.3 | 230.7 | mA |
| | | ECP3-95EA | 137.3 | 230.7 | mA |
| | | ECP3-150EA | 219.5 | 370.9 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP-17EA | 18.3 | 19.4 | mA |
| | | ECP3-35EA | 19.6 | 23.1 | mA |
| | | ECP3-70EA | 26.5 | 32.4 | mA |
| | | ECP3-95EA | 26.5 | 32.4 | mA |
| | | ECP3-150EA | 37.0 | 45.7 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (Per PLL) | ECP-17EA | 0.0 | 0.0 | mA |
| | | ECP3-35EA | 0.1 | 0.1 | mA |
| | | ECP3-70EA | 0.1 | 0.1 | mA |
| | | ECP3-95EA | 0.1 | 0.1 | mA |
| | | ECP3-150EA | 0.1 | 0.1 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP-17EA | 1.3 | 1.4 | mA |
| | | ECP3-35EA | 1.3 | 1.4 | mA |
| | | ECP3-70EA | 1.4 | 1.5 | mA |
| | | ECP3-95EA | 1.4 | 1.5 | mA |
| | | ECP3-150EA | 1.4 | 1.5 | mA |
| $I_{CCJ}$ | JTAG Power Supply Current | All Devices | 2.5 | 2.5 | mA |
| $I_{CCA}$ | Transmit, Receive, PLL and Reference Clock Buffer Power Supply | ECP-17EA | 6.1 | 6.1 | mA |
| | | ECP3-35EA | 6.1 | 6.1 | mA |
| | | ECP3-70EA | 18.3 | 18.3 | mA |
| | | ECP3-95EA | 18.3 | 18.3 | mA |
| | | ECP3-150EA | 24.4 | 24.4 | mA |

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

# sysI/O Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ |  | $V_{IH}$ |  | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
|  | Min. (V) | Max. (V) | Min. (V) | Max. (V) |  |  |  |  |
| LVCMOS33 | –0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | –20, –16, –12, -8, –4 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS25 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | –20, –16, –12, –8, –4 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS18 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | –16, –12, –8, –4 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS15 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | –8, –4 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS12 | –0.3 | 0.35 $V_{CC}$ | 0.65 $V_{CC}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | –6, –2 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVTTL33 | –0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | –20, –16, –12, –8, –4 |
|  |  |  |  |  | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| PCI33 | –0.3 | 0.3 $V_{CCIO}$ | 0.5 $V_{CCIO}$ | 3.6 | 0.1 $V_{CCIO}$ | 0.9 $V_{CCIO}$ | 1.5 | –0.5 |
| SSTL18_I | –0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6.7 | –6.7 |
| SSTL18_II (DDR2 Memory) | –0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.28 | $V_{CCIO}$ - 0.28 | 8 | –8 |
|  |  |  |  |  |  |  | 11 | –11 |
| SSTL2_I | –0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.54 | $V_{CCIO}$ - 0.62 | 7.6 | –7.6 |
|  |  |  |  |  |  |  | 12 | –12 |
| SSTL2_II (DDR Memory) | –0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.35 | $V_{CCIO}$ - 0.43 | 15.2 | –15.2 |
|  |  |  |  |  |  |  | 20 | –20 |
| SSTL3_I | –0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.7 | $V_{CCIO}$ - 1.1 | 8 | –8 |
| SSTL3_II | –0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.5 | $V_{CCIO}$ - 0.9 | 16 | –16 |
| SSTL15 (DDR3 Memory) | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.3 | $V_{CCIO}$ - 0.3 | 7.5 | –7.5 |
|  |  |  |  |  |  | $V_{CCIO}$ * 0.8 | 9 | –9 |
| HSTL15_I | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –4 |
|  |  |  |  |  |  |  | 8 | –8 |
| HSTL18_I | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | –8 |
|  |  |  |  |  |  |  | 12 | –12 |
| HSTL18_II | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | –16 |

1. For electromigration, the average DC current drawn by I/O pads between two consecutive $V_{CCIO}$ or GND pad connections, or between the last $V_{CCIO}$ or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed n * 8 mA, where n is the number of I/O pads between the two consecutive bank $V_{CCIO}$ or GND connections or between the last $V_{CCIO}$ and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

## LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

*Figure 3-3. Differential LVPECL33*

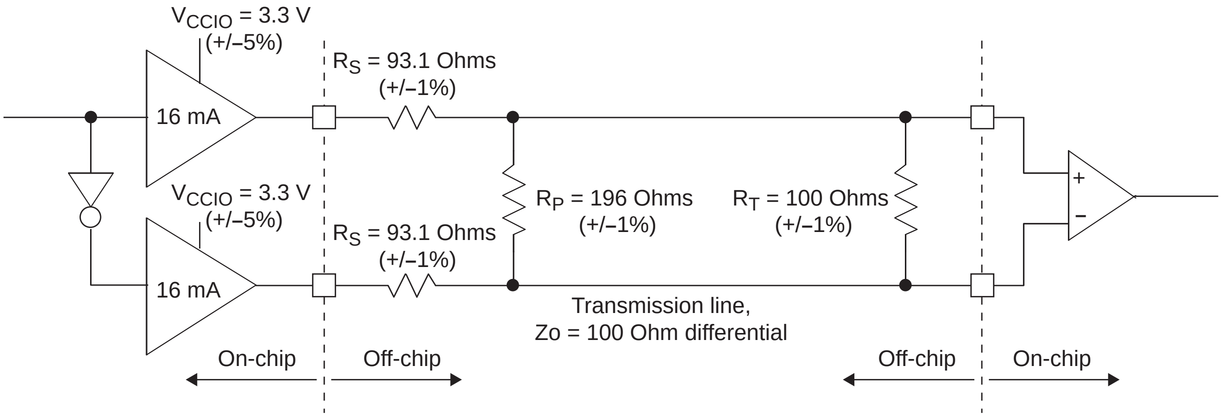


*Table 3-3. LVPECL33 DC Conditions*[1]

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/–5%) | 3.30 | V |
| $Z_{OUT}$ | Driver Impedance | 10 | Ω |
| $R_S$ | Driver Series Resistor (+/–1%) | 93 | Ω |
| $R_P$ | Driver Parallel Resistor (+/–1%) | 196 | Ω |
| $R_T$ | Receiver Termination (+/–1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 2.05 | V |
| $V_{OL}$ | Output Low Voltage | 1.25 | V |
| $V_{OD}$ | Output Differential Voltage | 0.80 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.65 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 12.11 | mA |

1. For input buffer, see LVDS table.

## LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

### Over Recommended Commercial Operating Conditions

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDRX2_RX.ECLK.Aligned) (No CLKDIV)** | | | | | | | | | |
| **Left and Right Sides Using DLLCLKPIN for Clock Input** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | 460 | — | 385 | — | 345 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70EA/95EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70EA/95EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| fMAX_GDDR | DDRX2 Clock Frequency | ECP3-70EA/95EA | — | 460 | — | 385 | — | 311 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-35EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-35EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-35EA | — | 460 | — | 385 | — | 311 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK (Left and Right Sides) | ECP3-17EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-17EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-17EA | — | 460 | — | 385 | — | 311 | MHz |
| **Top Side Using PCLK Pin for Clock Input** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70EA/95EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70EA/95EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-70EA/95EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-35EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-35EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-35EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-17EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-17EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-17EA | — | 235 | — | 170 | — | 130 | MHz |
| **Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) Using DQS Pin for Clock Input** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | 330 | — | 330 | — | 352 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 330 | — | 330 | — | 352 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 400 | — | 400 | — | 375 | MHz |
| **Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 400 | — | 400 | — | 375 | MHz |
| **Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)[10]** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-70EA/95EA | 666 | — | 665 | — | 664 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-70EA/95EA | 666 | — | 665 | — | 664 | — | ps |

## LatticeECP3 Maximum I/O Buffer Speed [1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Buffer | Description | Max. | Units |
|---|---|---|---|
| **Maximum Input Frequency** | | | |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| MLVDS25 | MLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| BLVDS25 | BLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| PPLVDS | Point-to-Point LVDS | 400 | MHz |
| TRLVDS | Transition-Reduced LVDS | 612 | MHz |
| Mini LVDS | Mini LVDS | 400 | MHz |
| LVPECL33 | LVPECL, Emulated, $V_{CCIO}$ = 3.3 V | 400 | MHz |
| HSTL18 (all supported classes) | HSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 400 | MHz |
| HSTL15 | HSTL_15 class I, $V_{CCIO}$ = 1.5 V | 400 | MHz |
| SSTL33 (all supported classes) | SSTL_3 class I, II, $V_{CCIO}$ = 3.3 V | 400 | MHz |
| SSTL25 (all supported classes) | SSTL_2 class I, II, $V_{CCIO}$ = 2.5 V | 400 | MHz |
| SSTL18 (all supported classes) | SSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 400 | MHz |
| LVTTL33 | LVTTL, $V_{CCIO}$ = 3.3 V | 166 | MHz |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | 166 | MHz |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 166 | MHz |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 166 | MHz |
| LVCMOS15 | LVCMOS 1.5, $V_{CCIO}$ = 1.5 V | 166 | MHz |
| LVCMOS12 | LVCMOS 1.2, $V_{CCIO}$ = 1.2 V | 166 | MHz |
| PCI33 | PCI, $V_{CCIO}$ = 3.3 V | 66 | MHz |
| **Maximum Output Frequency** | | | |
| LVDS25E | LVDS, Emulated, $V_{CCIO}$ = 2.5 V | 300 | MHz |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | 612 | MHz |
| MLVDS25 | MLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 300 | MHz |
| RSDS25 | RSDS, Emulated, $V_{CCIO}$ = 2.5 V | 612 | MHz |
| BLVDS25 | BLVDS, Emulated, $V_{CCIO}$ = 2.5 V | 300 | MHz |
| PPLVDS | Point-to-point LVDS | 612 | MHz |
| LVPECL33 | LVPECL, Emulated, $V_{CCIO}$ = 3.3 V | 612 | MHz |
| Mini-LVDS | Mini LVDS | 612 | MHz |
| HSTL18 (all supported classes) | HSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 200 | MHz |
| HSTL15 (all supported classes) | HSTL_15 class I, $V_{CCIO}$ = 1.5 V | 200 | MHz |
| SSTL33 (all supported classes) | SSTL_3 class I, II, $V_{CCIO}$ = 3.3 V | 233 | MHz |
| SSTL25 (all supported classes) | SSTL_2 class I, II, $V_{CCIO}$ = 2.5 V | 233 | MHz |
| SSTL18 (all supported classes) | SSTL_18 class I, II, $V_{CCIO}$ = 1.8 V | 266 | MHz |
| LVTTL33 | LVTTL, $V_{CCIO}$ = 3.3 V | 166 | MHz |
| LVCMOS33 (For all drives) | LVCMOS, 3.3 V | 166 | MHz |
| LVCMOS25 (For all drives) | LVCMOS, 2.5 V | 166 | MHz |
| LVCMOS18 (For all drives) | LVCMOS, 1.8 V | 166 | MHz |
| LVCMOS15 (For all drives) | LVCMOS, 1.5 V | 166 | MHz |
| LVCMOS12 (For all drives except 2 mA) | LVCMOS, $V_{CCIO}$ = 1.2 V | 166 | MHz |
| LVCMOS12 (2 mA drive) | LVCMOS, $V_{CCIO}$ = 1.2 V | 100 | MHz |

# sysCLOCK PLL Timing

### Over Recommended Operating Conditions

| Parameter | Descriptions | Conditions | Clock | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (CLKI, CLKFB) |  | Edge clock | 2 | — | 500 | MHz |
|  |  |  | Primary clock[4] | 2 | — | 420 | MHz |
| $f_{OUT}$ | Output clock frequency (CLKOP, CLKOS) |  | Edge clock | 4 | — | 500 | MHz |
|  |  |  | Primary clock[4] | 4 | — | 420 | MHz |
| $f_{OUT1}$ | K-Divider output frequency | CLKOK |  | 0.03125 | — | 250 | MHz |
| $f_{OUT2}$ | K2-Divider output frequency | CLKOK2 |  | 0.667 | — | 166 | MHz |
| $f_{VCO}$ | PLL VCO frequency |  |  | 500 | — | 1000 | MHz |
| $f_{PFD}$[3] | Phase detector input frequency |  | Edge clock | 2 | — | 500 | MHz |
|  |  |  | Primary clock[4] | 2 | — | 420 | MHz |
| **AC Characteristics** |  |  |  |  |  |  |  |
| $t_{PA}$ | Programmable delay unit |  |  | 65 | 130 | 260 | ps |
| $t_{DT}$ | Output clock duty cycle (CLKOS, at 50% setting) |  | Edge clock | 45 | 50 | 55 | % |
|  |  | $f_{OUT} \leq 250$ MHz | Primary clock | 45 | 50 | 55 | % |
|  |  | $f_{OUT} > 250$ MHz | Primary clock | 30 | 50 | 70 | % |
| $t_{CPA}$ | Coarse phase shift error (CLKOS, at all settings) |  |  | -5 | 0 | +5 | % of period |
| $t_{OPW}$ | Output clock pulse width high or low (CLKOS) |  |  | 1.8 | — | — | ns |
| $t_{OPJIT}$[1] | Output clock period jitter | $f_{OUT} \geq 420$ MHz |  | — | — | 200 | ps |
|  |  | 420 MHz $> f_{OUT} \geq 100$ MHz |  | — | — | 250 | ps |
|  |  | $f_{OUT} < 100$ MHz |  | — | — | 0.025 | UIPP |
| $t_{SK}$ | Input clock to output clock skew when N/M = integer |  |  | — | — | 500 | ps |
| $t_{LOCK}$[2] | Lock time | 2 to 25 MHz |  | — | — | 200 | us |
|  |  | 25 to 500 MHz |  | — | — | 50 | us |
| $t_{UNLOCK}$ | Reset to PLL unlock time to ensure fast reset |  |  | — | — | 50 | ns |
| $t_{HI}$ | Input clock high time | 90% to 90% |  | 0.5 | — | — | ns |
| $t_{LO}$ | Input clock low time | 10% to 10% |  | 0.5 | — | — | ns |
| $t_{IPJIT}$ | Input clock period jitter |  |  | — | — | 400 | ps |
| $t_{RST}$ | Reset signal pulse width high, RSTK |  |  | 10 | — | — | ns |
|  | Reset signal pulse width high, RST |  |  | 500 | — | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

## SERDES/PCS Block Latency

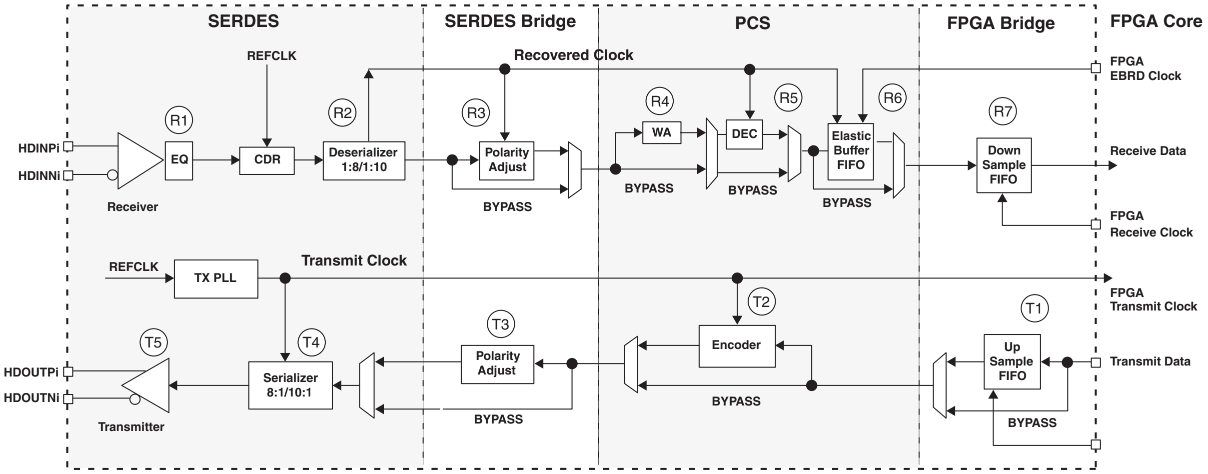
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

*Table 3-8. SERDES/PCS Latency Breakdown*

| Item | Description | Min. | Avg. | Max. | Fixed | Bypass | Units |
|---|---|---|---|---|---|---|---|
| **Transmit Data Latency**[1] | | | | | | | |
| T1 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |
| T2 | 8b10b Encoder | — | — | — | 2 | 1 | word clk |
| T3 | SERDES Bridge transmit | — | — | — | 2 | 1 | word clk |
| T4 | Serializer: 8-bit mode | — | — | — | 15 + Δ1 | — | UI + ps |
| | Serializer: 10-bit mode | — | — | — | 18 + Δ1 | — | UI + ps |
| T5 | Pre-emphasis ON | — | — | — | 1 + Δ2 | — | UI + ps |
| | Pre-emphasis OFF | — | — | — | 0 + Δ3 | — | UI + ps |
| **Receive Data Latency**[2] | | | | | | | |
| R1 | Equalization ON | — | — | — | Δ1 | — | UI + ps |
| | Equalization OFF | — | — | — | Δ2 | — | UI + ps |
| R2 | Deserializer: 8-bit mode | — | — | — | 10 + Δ3 | — | UI + ps |
| | Deserializer: 10-bit mode | — | — | — | 12 + Δ3 | — | UI + ps |
| R3 | SERDES Bridge receive | — | — | — | 2 | — | word clk |
| R4 | Word alignment | 3.1 | — | 4 | — | — | word clk |
| R5 | 8b10b decoder | — | — | — | 1 | — | word clk |
| R6 | Clock Tolerance Compensation | 7 | 15 | 23 | 1 | 1 | word clk |
| R7 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

*Figure 3-12. Transmitter and Receiver Latency Block Diagram*



# Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

## AC and DC Characteristics

*Table 3-15. Transmit*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{RF}$[1] | Differential rise/fall time | 20%-80% | — | 80 | — | ps |
| $Z_{TX\_DIFF\_DC}$ | Differential impedance | | 80 | 100 | 120 | Ohms |
| $J_{TX\_DDJ}$[3, 4, 5] | Output data deterministic jitter | | — | — | 0.17 | UI |
| $J_{TX\_TJ}$[2, 3, 4, 5] | Total output data jitter | | — | — | 0.35 | UI |

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

*Table 3-16. Receive and Jitter Tolerance*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RL_{RX\_DIFF}$ | Differential return loss | From 100 MHz to 2.5 GHz | 10 | — | — | dB |
| $RL_{RX\_CM}$ | Common mode return loss | From 100 MHz to 2.5 GHz | 6 | — | — | dB |
| $Z_{RX\_DIFF}$ | Differential termination resistance | | 80 | 100 | 120 | Ohms |
| $J_{RX\_DJ}$[2, 3, 4, 5] | Deterministic jitter tolerance (peak-to-peak) | | — | — | 0.37 | UI |
| $J_{RX\_RJ}$[2, 3, 4, 5] | Random jitter tolerance (peak-to-peak) | | — | — | 0.18 | UI |
| $J_{RX\_SJ}$[2, 3, 4, 5] | Sinusoidal jitter tolerance (peak-to-peak) | | — | — | 0.10 | UI |
| $J_{RX\_TJ}$[1, 2, 3, 4, 5] | Total jitter tolerance (peak-to-peak) | | — | — | 0.65 | UI |
| $T_{RX\_EYE}$ | Receiver eye opening | | 0.35 | — | — | UI |

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

# SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

## AC and DC Characteristics

*Table 3-19. Transmit*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDO}$ | Serial data rate | | 270 | — | 2975 | Mbps |
| $T_{JALIGNMENT}{}^{2}$ | Serial output jitter, alignment | 270 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}{}^{2}$ | Serial output jitter, alignment | 1485 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}{}^{1,2}$ | Serial output jitter, alignment | 2970Mbps | — | — | 0.30 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 270 Mbps | — | — | 0.20 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 1485 Mbps | — | — | 1.0 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 2970 Mbps | — | — | 2.0 | UI |

Notes:

1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of $f_{SCLK}$ is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

*Table 3-20. Receive*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDI}$ | Serial input data rate | | 270 | — | 2970 | Mbps |
| CID | Stream of non-transitions (=Consecutive Identical Digits) | | 7(3G)/26(SMPTE Triple rates) @ 10-12 BER | — | — | Bits |

*Table 3-21. Reference Clock*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{VCLK}$ | Video output clock frequency | | 27 | — | 74.25 | MHz |
| $DC_{V}$ | Duty cycle, video clock | | 45 | 50 | 55 | % |

## LatticeECP3 sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

| Parameter | Description | | Min. | Max. | Units |
|---|---|---|---|---|---|
| **POR, Configuration Initialization, and Wakeup** | | | | | |
| $t_{ICFG}$ | Time from the Application of $V_{CC}$, $V_{CCAUX}$ or $V_{CCIO8}$* (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN | Master mode | — | 23 | ms |
| | | Slave mode | — | 6 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to the Valid Master MCLK | | — | 5 | µs |
| $t_{PRGM}$ | PROGRAMN Low Time to Start Configuration | | 25 | — | ns |
| $t_{PRGMRJ}$ | PROGRAMN Pin Pulse Rejection | | — | 10 | ns |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INITN Low | | — | 37 | ns |
| $t_{DPPDONE}$ | Delay Time from PROGRAMN Low to DONE Low | | — | 37 | ns |
| $t_{DINIT}$[1] | PROGRAMN High to INITN High Delay | | — | 1 | ms |
| $t_{MWC}$ | Additional Wake Master Clock Signals After DONE Pin is High | | 100 | 500 | cycles |
| $t_{CZ}$ | MCLK From Active To Low To High-Z | | — | 300 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | | — | 100 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | | — | 100 | ns |
| **All Configuration Modes** | | | | | |
| $t_{SUCDI}$ | Data Setup Time to CCLK/MCLK | | 5 | — | ns |
| $t_{HCDI}$ | Data Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{CODO}$ | CCLK/MCLK to DOUT in Flowthrough Mode | | -0.2 | 12 | ns |
| **Slave Serial** | | | | | |
| $t_{SSCH}$ | CCLK Minimum High Pulse | | 5 | — | ns |
| $t_{SSCL}$ | CCLK Minimum Low Pulse | | 5 | — | ns |
| $f_{CCLK}$ | CCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| **Master and Slave Parallel** | | | | | |
| $t_{SUCS}$ | CSN[1:0] Setup Time to CCLK/MCLK | | 7 | — | ns |
| $t_{HCS}$ | CSN[1:0] Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{SUWD}$ | WRITEN Setup Time to CCLK/MCLK | | 7 | — | ns |
| $t_{HWD}$ | WRITEN Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{DCB}$ | CCLK/MCLK to BUSY Delay Time | | — | 12 | ns |
| $t_{CORD}$ | CCLK to Out for Read Data | | — | 12 | ns |
| $t_{BSCH}$ | CCLK Minimum High Pulse | | 6 | — | ns |
| $t_{BSCL}$ | CCLK Minimum Low Pulse | | 6 | — | ns |
| $t_{BSCYC}$ | Byte Slave Cycle Time | | 30 | — | ns |
| $f_{CCLK}$ | CCLK/MCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| **Master and Slave SPI** | | | | | |
| $t_{CFGX}$ | INITN High to MCLK Low | | — | 80 | ns |
| $t_{CSSPI}$ | INITN High to CSSPIN Low | | 0.2 | 2 | µs |
| $t_{SOCDO}$ | MCLK Low to Output Valid | | — | 15 | ns |
| $t_{CSPID}$ | CSSPIN[0:1] Low to First MCLK Edge Setup Time | | 0.3 | | µs |
| $f_{CCLK}$ | CCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| $t_{SSCH}$ | CCLK Minimum High Pulse | | 5 | — | ns |

## Pin Information Summary (Cont.)

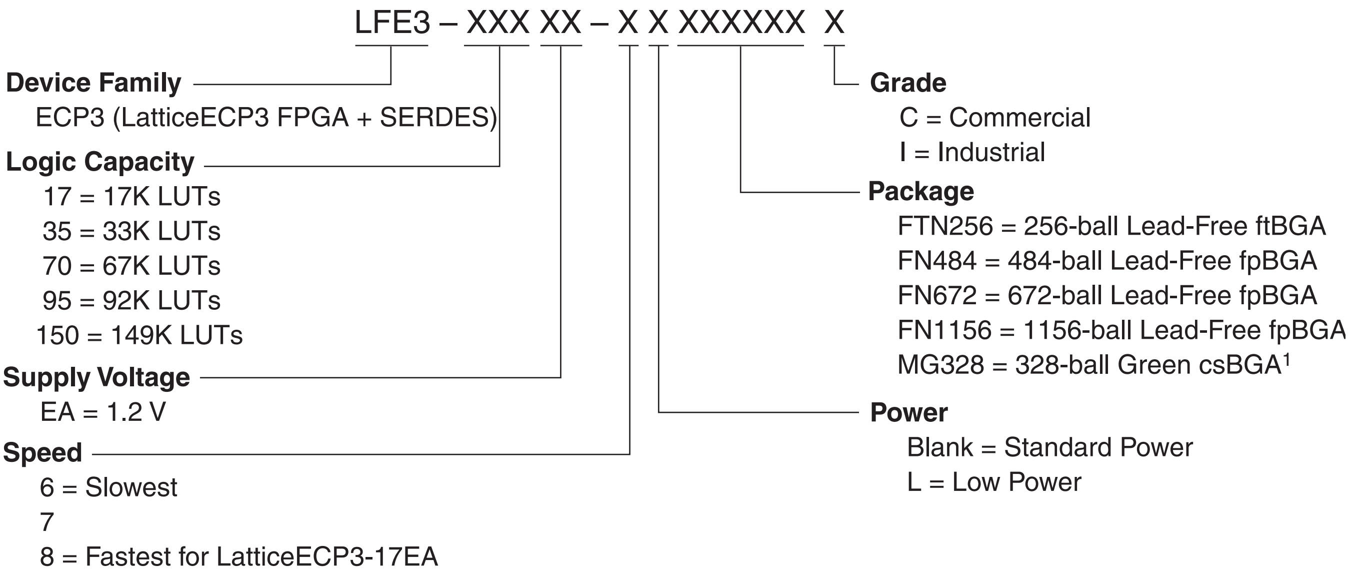
| Pin Information Summary | | ECP3-95EA | | | ECP3-150EA | |
|---|---|---|---|---|---|---|
| Pin Type | | 484 fpBGA | 672 fpBGA | 1156 fpBGA | 672 fpBGA | 1156 fpBGA |
| Emulated Differential I/O per Bank | Bank 0 | 21 | 30 | 43 | 30 | 47 |
| | Bank 1 | 18 | 24 | 39 | 24 | 43 |
| | Bank 2 | 8 | 12 | 13 | 12 | 18 |
| | Bank 3 | 20 | 23 | 33 | 23 | 37 |
| | Bank 6 | 22 | 25 | 33 | 25 | 37 |
| | Bank 7 | 11 | 16 | 18 | 16 | 24 |
| | Bank 8 | 12 | 12 | 12 | 12 | 12 |
| Highspeed Differential I/O per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 6 | 9 | 9 | 9 | 15 |
| | Bank 3 | 9 | 12 | 16 | 12 | 21 |
| | Bank 6 | 11 | 14 | 16 | 14 | 21 |
| | Bank 7 | 9 | 12 | 13 | 12 | 18 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| Total Single Ended/ Total Differential I/O per Bank | Bank 0 | 42/21 | 60/30 | 86/43 | 60/30 | 94/47 |
| | Bank 1 | 36/18 | 48/24 | 78/39 | 48/24 | 86/43 |
| | Bank 2 | 28/14 | 42/21 | 44/22 | 42/21 | 66/33 |
| | Bank 3 | 58/29 | 71/35 | 98/49 | 71/35 | 116/58 |
| | Bank 6 | 67/33 | 78/39 | 98/49 | 78/39 | 116/58 |
| | Bank 7 | 40/20 | 56/28 | 62/31 | 56/28 | 84/42 |
| | Bank 8 | 24/12 | 24/12 | 24/12 | 24/12 | 24/12 |
| DDR Groups Bonded per Bank | Bank 0 | 3 | 5 | 7 | 5 | 7 |
| | Bank 1 | 3 | 4 | 7 | 4 | 7 |
| | Bank 2 | 2 | 3 | 3 | 3 | 4 |
| | Bank 3 | 3 | 4 | 5 | 4 | 7 |
| | Bank 6 | 4 | 4 | 5 | 4 | 7 |
| | Bank 7 | 3 | 4 | 4 | 4 | 6 |
| | Configuration Bank8 | 0 | 0 | 0 | 0 | 0 |
| SERDES Quads | | 1 | 2 | 3 | 2 | 4 |

1.These pins must remain floating on the board.

# LatticeECP3 Family Data Sheet
# Ordering Information

**April 2014** **Data Sheet DS1021**

## LatticeECP3 Part Number Description



LFE3 – XXX XX – X X XXXXXX X

**Device Family**
ECP3 (LatticeECP3 FPGA + SERDES)

**Logic Capacity**
17 = 17K LUTs
35 = 33K LUTs
70 = 67K LUTs
95 = 92K LUTs
150 = 149K LUTs

**Supply Voltage**
EA = 1.2 V

**Speed**
6 = Slowest
7
8 = Fastest for LatticeECP3-17EA

**Grade**
C = Commercial
I = Industrial

**Package**
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN1156 = 1156-ball Lead-Free fpBGA
MG328 = 328-ball Green csBGA[1]

**Power**
Blank = Standard Power
L = Low Power

[1] Green = Halogen free and lead free.

## Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:

**Commercial**

**Industrial**

Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

# LatticeECP3 Family Data Sheet
# Supplemental Information

**February 2014** **Data Sheet DS1021**

## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist
- TN1215, LatticeECP2MS and LatticeECP2S Devices
- TN1216, LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3
- TN1222, LatticeECP3 Slave SPI Port User's Guide

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com