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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn672i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6fn672i</a>

## ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

## Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

**Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family**

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

**Table 2-10. Embedded SRAM in the LatticeECP3 Family**

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

## DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

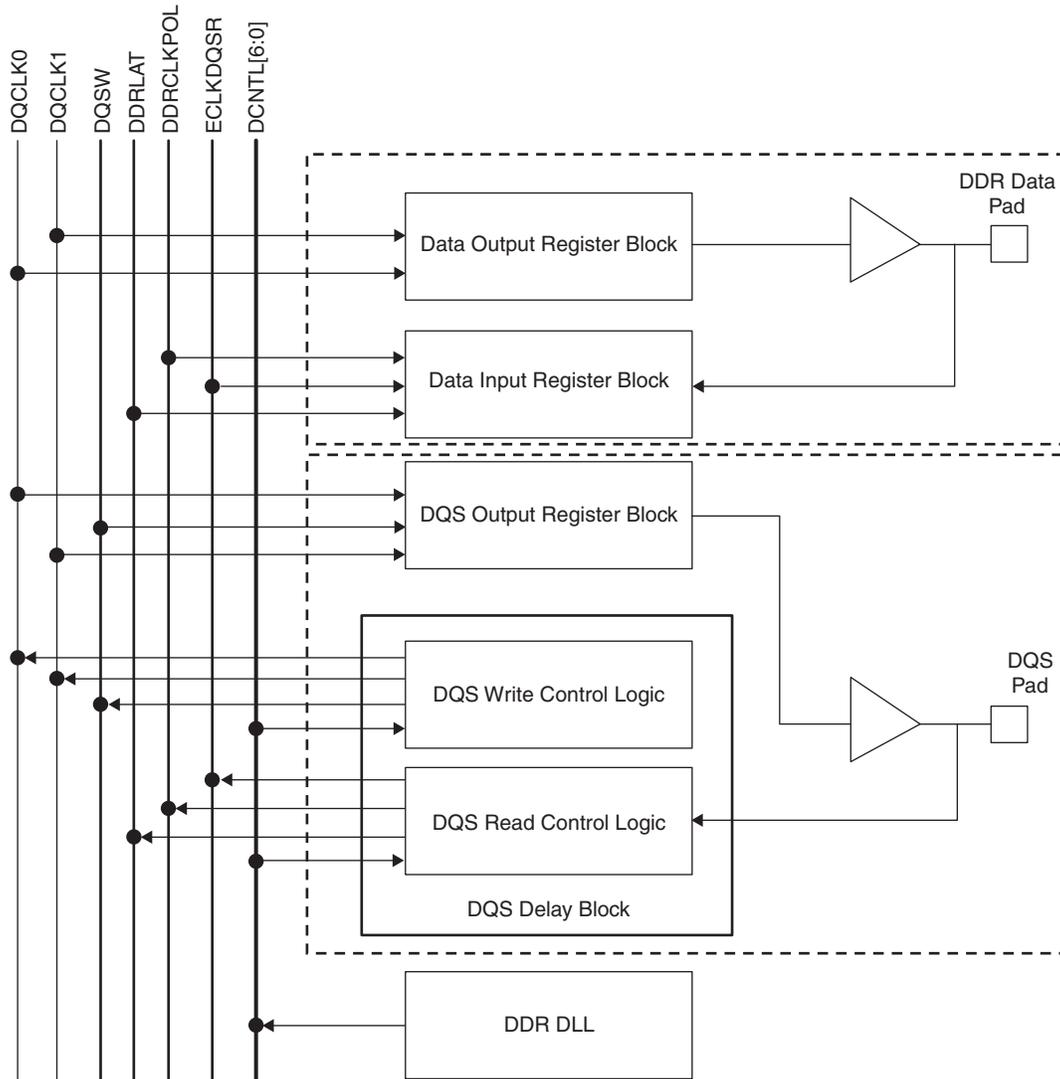
The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Figure 2-37. DQS Local Bus



### Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

### DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on DDR Memory interface implementation in LatticeECP3.

## sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

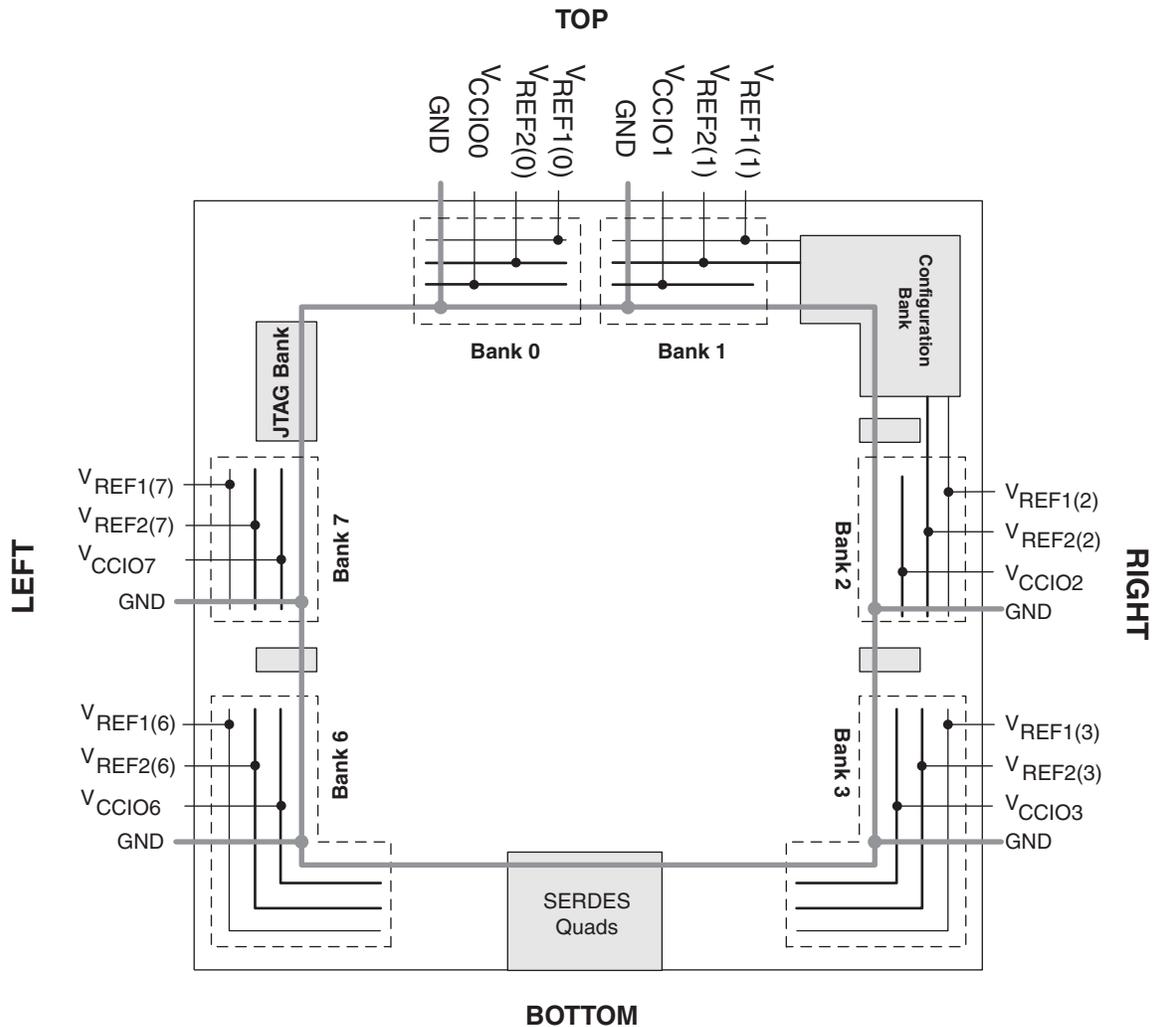
### sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage ( $V_{CCIO}$ ). In addition, each bank, except the Configuration Bank, has voltage references,  $V_{REF1}$  and  $V_{REF2}$ , which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using  $V_{CCIO}$ . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of  $V_{CCIO}$ .

Each bank can support up to two separate  $V_{REF}$  voltages,  $V_{REF1}$  and  $V_{REF2}$ , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)**

The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

**LatticeECP3 Supply Current (Standby)<sup>1, 2, 3, 4, 5, 6</sup>**
**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typical		Units
			-6L, -7L, -8L	-6, -7, -8	
I <sub>CC</sub>	Core Power Supply Current	ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
		ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply Current	ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
		ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
I <sub>CCPLL</sub>	PLL Power Supply Current (Per PLL)	ECP-17EA	0.0	0.0	mA
		ECP3-35EA	0.1	0.1	mA
		ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
I <sub>CCIO</sub>	Bank Power Supply Current (Per Bank)	ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
		ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I <sub>CCJ</sub>	JTAG Power Supply Current	All Devices	2.5	2.5	mA
I <sub>CCA</sub>	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
		ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.
3. Frequency 0 MHz.
4. Pattern represents a "blank" configuration data file.
5. T<sub>J</sub> = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

### LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL33

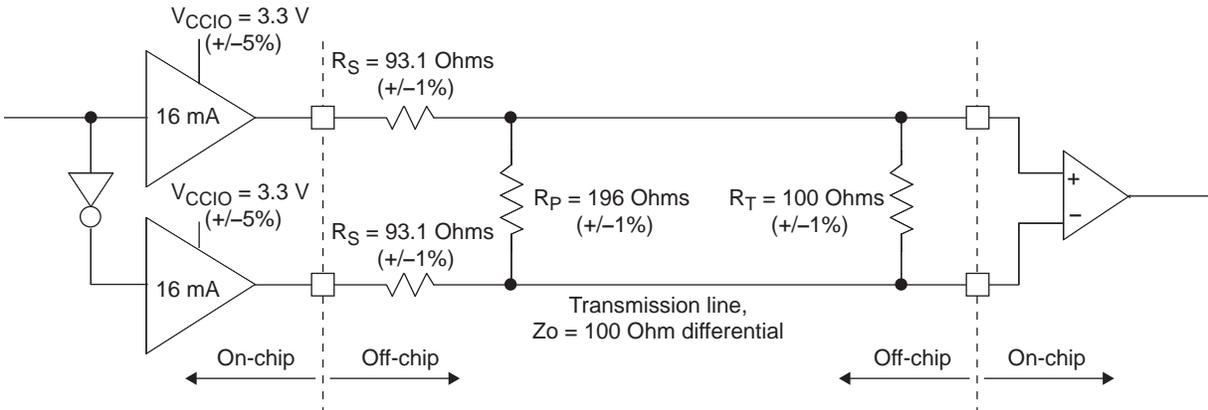


Table 3-3. LVPECL33 DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
$V_{CCIO}$	Output Driver Supply ( $\pm 5\%$ )	3.30	V
$Z_{OUT}$	Driver Impedance	10	$\Omega$
$R_S$	Driver Series Resistor ( $\pm 1\%$ )	93	$\Omega$
$R_P$	Driver Parallel Resistor ( $\pm 1\%$ )	196	$\Omega$
$R_T$	Receiver Termination ( $\pm 1\%$ )	100	$\Omega$
$V_{OH}$	Output High Voltage	2.05	V
$V_{OL}$	Output Low Voltage	1.25	V
$V_{OD}$	Output Differential Voltage	0.80	V
$V_{CM}$	Output Common Mode Voltage	1.65	V
$Z_{BACK}$	Back Impedance	100.5	$\Omega$
$I_{DC}$	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

## Typical Building Block Function Performance

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)<sup>1, 2, 3</sup>

Function	-8 Timing	Units
<b>Basic Functions</b>		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

### Register-to-Register Performance<sup>1, 2, 3</sup>

Function	-8 Timing	Units
<b>Basic Functions</b>		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	500	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
<b>Embedded Memory Functions</b>		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
<b>Distributed Memory Functions</b>		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	400	MHz
<b>DSP Function</b>		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	260	MHz

## LatticeECP3 External Switching Characteristics (Continued)<sup>1, 2, 3, 13</sup>

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>Generic DDRX2 Inputs with Clock and Data (&gt;10bits wide) are Aligned at Pin (GDDR2_RX.ECLK.Aligned) (No CLKDIV)</b>									
<b>Left and Right Sides Using DLLCLKPIN for Clock Input</b>									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
<b>Top Side Using PCLK Pin for Clock Input</b>									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
<b>Generic DDRX2 Inputs with Clock and Data (&lt;10 Bits Wide) Centered at Pin (GDDR2_RX.DQS.Centered) Using DQS Pin for Clock Input</b>									
<b>Left and Right Sides</b>									
t <sub>SUGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
<b>Generic DDRX2 Inputs with Clock and Data (&lt;10 Bits Wide) Aligned at Pin (GDDR2_RX.DQS.Aligned) Using DQS Pin for Clock Input</b>									
<b>Left and Right Sides</b>									
t <sub>DVACLGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
<b>Generic DDRX1 Output with Clock and Data (&gt;10 Bits Wide) Centered at Pin (GDDR1_TX.SCLK.Centered)<sup>10</sup></b>									
t <sub>DVBGDDR</sub>	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t <sub>DVAGDDR</sub>	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f <sub>MAX_GDDR</sub>	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t <sub>DVBGDDR</sub>	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
t <sub>DVAGDDR</sub>	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

**LatticeECP3 Family Timing Adders<sup>1, 2, 3, 4, 5, 7</sup>**
**Over Recommended Commercial Operating Conditions**

Buffer Type	Description	-8	-7	-6	Units
<b>Input Adjusters</b>					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
RS25	RS25, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
PPLVDS	Point-to-Point LVDS	0.03	-0.01	-0.03	ns
TRLVDS	Transition-Reduced LVDS	0.03	0.00	-0.04	ns
Mini MLVDS	Mini LVDS	0.03	-0.01	-0.03	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns
LVTTTL33	LVTTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC33	LVC33, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC25	LVC25, VCCIO = 2.5 V	0.00	0.00	0.00	ns
LVC18	LVC18, VCCIO = 1.8 V	-0.13	-0.13	-0.13	ns
LVC15	LVC15, VCCIO = 1.5 V	-0.07	-0.07	-0.07	ns
LVC12	LVC12, VCCIO = 1.2 V	-0.20	-0.19	-0.19	ns
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns
<b>Output Adjusters</b>					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns
LVDS25	LVDS, VCCIO = 2.5 V	-0.11	-0.07	-0.03	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns

**LatticeECP3 Maximum I/O Buffer Speed** <sup>1, 2, 3, 4, 5, 6</sup>
**Over Recommended Operating Conditions**

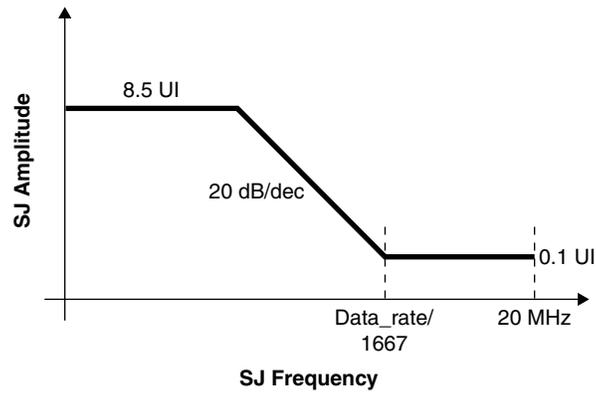
Buffer	Description	Max.	Units
<b>Maximum Input Frequency</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
PPLVDS	Point-to-Point LVDS	400	MHz
TRLVDS	Transition-Reduced LVDS	612	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	400	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
HSTL15	HSTL_15 class I, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, $V_{CCIO} = 3.3\text{ V}$	400	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, $V_{CCIO} = 2.5\text{ V}$	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	166	MHz
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	166	MHz
LVC MOS15	LVC MOS 1.5, $V_{CCIO} = 1.5\text{ V}$	166	MHz
LVC MOS12	LVC MOS 1.2, $V_{CCIO} = 1.2\text{ V}$	166	MHz
PCI33	PCI, $V_{CCIO} = 3.3\text{ V}$	66	MHz
<b>Maximum Output Frequency</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	612	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
RS DS25	RS DS, Emulated, $V_{CCIO} = 2.5\text{ V}$	612	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
PPLVDS	Point-to-point LVDS	612	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	612	MHz
Mini-LVDS	Mini LVDS	612	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	200	MHz
HSTL15 (all supported classes)	HSTL_15 class I, $V_{CCIO} = 1.5\text{ V}$	200	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, $V_{CCIO} = 3.3\text{ V}$	233	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, $V_{CCIO} = 2.5\text{ V}$	233	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	266	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS33 (For all drives)	LVC MOS, 3.3 V	166	MHz
LVC MOS25 (For all drives)	LVC MOS, 2.5 V	166	MHz
LVC MOS18 (For all drives)	LVC MOS, 1.8 V	166	MHz
LVC MOS15 (For all drives)	LVC MOS, 1.5 V	166	MHz
LVC MOS12 (For all drives except 2 mA)	LVC MOS, $V_{CCIO} = 1.2\text{ V}$	166	MHz
LVC MOS12 (2 mA drive)	LVC MOS, $V_{CCIO} = 1.2\text{ V}$	100	MHz

**Table 3-11. Periodic Receiver Jitter Tolerance Specification**

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

## Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

### AC and DC Characteristics

**Table 3-15. Transmit**

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$T_{RF}^1$	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
$J_{TX\_DDJ}^{3,4,5}$	Output data deterministic jitter		—	—	0.17	UI
$J_{TX\_TJ}^{2,3,4,5}$	Total output data jitter		—	—	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

**Table 3-16. Receive and Jitter Tolerance**

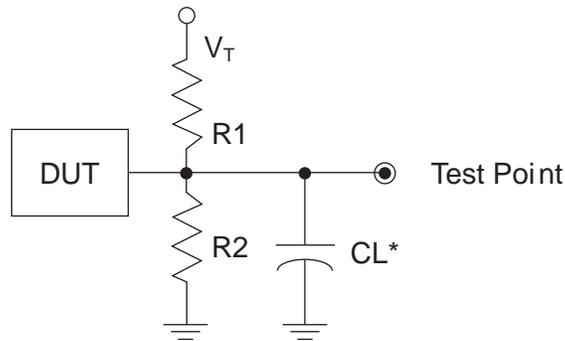
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
$RL_{RX\_DIFF}$	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
$RL_{RX\_CM}$	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
$Z_{RX\_DIFF}$	Differential termination resistance		80	100	120	Ohms
$J_{RX\_DJ}^{2,3,4,5}$	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
$J_{RX\_RJ}^{2,3,4,5}$	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
$J_{RX\_SJ}^{2,3,4,5}$	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
$J_{RX\_TJ}^{1,2,3,4,5}$	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
$T_{RX\_EYE}$	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

## Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

**Figure 3-33. Output Test Load, LVTTTL and LVCMOS Standards**



\*CL Includes Test Fixture and Probe Capacitance

**Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V <sub>OH</sub> - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

**Pin Information Summary (Cont.)**

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	30	47
	Bank 1	18	24	39	24	43
	Bank 2	8	12	13	12	18
	Bank 3	20	23	33	23	37
	Bank 6	22	25	33	25	37
	Bank 7	11	16	18	16	24
	Bank 8	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	6	9	9	9	15
	Bank 3	9	12	16	12	21
	Bank 6	11	14	16	14	21
	Bank 7	9	12	13	12	18
	Bank 8	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	60/30	94/47
	Bank 1	36/18	48/24	78/39	48/24	86/43
	Bank 2	28/14	42/21	44/22	42/21	66/33
	Bank 3	58/29	71/35	98/49	71/35	116/58
	Bank 6	67/33	78/39	98/49	78/39	116/58
	Bank 7	40/20	56/28	62/31	56/28	84/42
	Bank 8	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	5	7
	Bank 1	3	4	7	4	7
	Bank 2	2	3	3	3	4
	Bank 3	3	4	5	4	7
	Bank 6	4	4	5	4	7
	Bank 7	3	4	4	4	6
	Configuration Bank8	0	0	0	0	0
SERDES Quads		1	2	3	2	4

1. These pins must remain floating on the board.

## Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at <http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3> and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools > Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

## Thermal Management

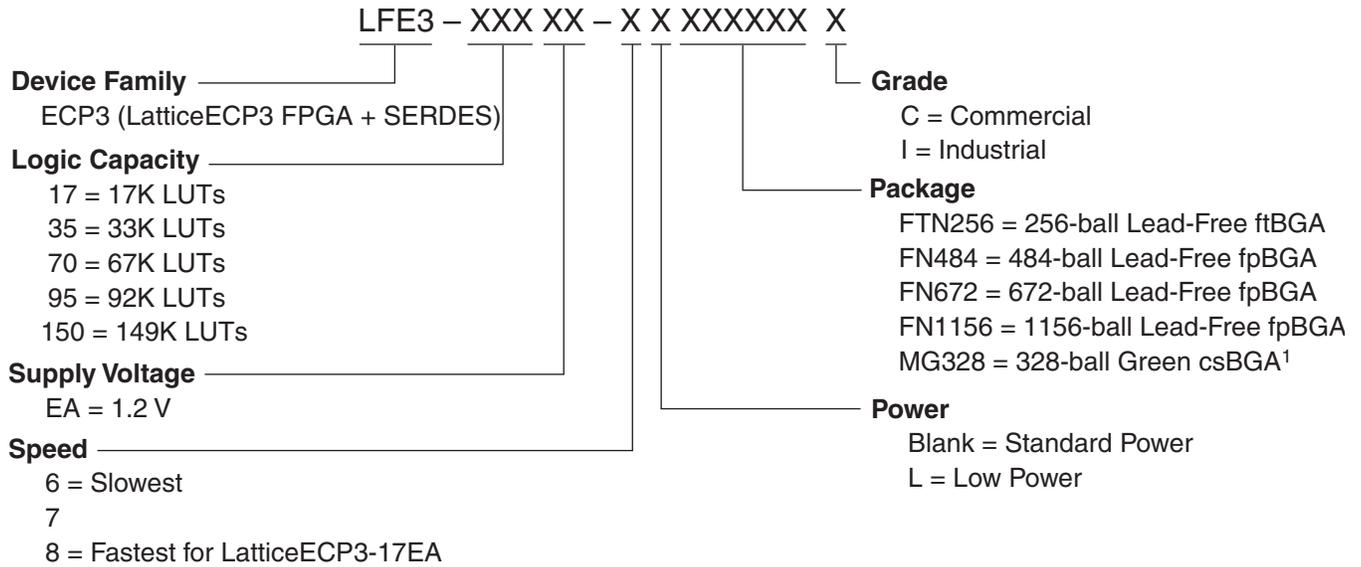
Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

## For Further Information

For further information regarding Thermal Management, refer to the following:

- [Thermal Management](#) document
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from [www.latticesemi.com/software](http://www.latticesemi.com/software)

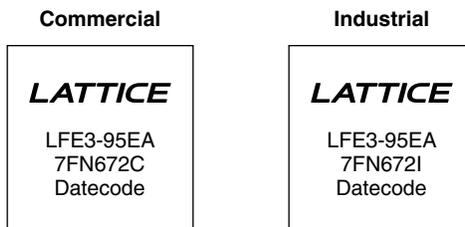
## LatticeECP3 Part Number Description



1. Green = Halogen free and lead free.

## Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:



Note: See [PCN 05A-12](#) for information regarding a change to the top-side mark logo.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW <sup>1</sup>	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW <sup>1</sup>	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW <sup>1</sup>	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW <sup>1</sup>	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW <sup>1</sup>	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW <sup>1</sup>	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*spFNpkgCTW* and LFE3-150EA-*spFNpkgITW* devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*spFNpkgC* and LFE3-150EA-*spFNpkgI* devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250 V.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	92

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