

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

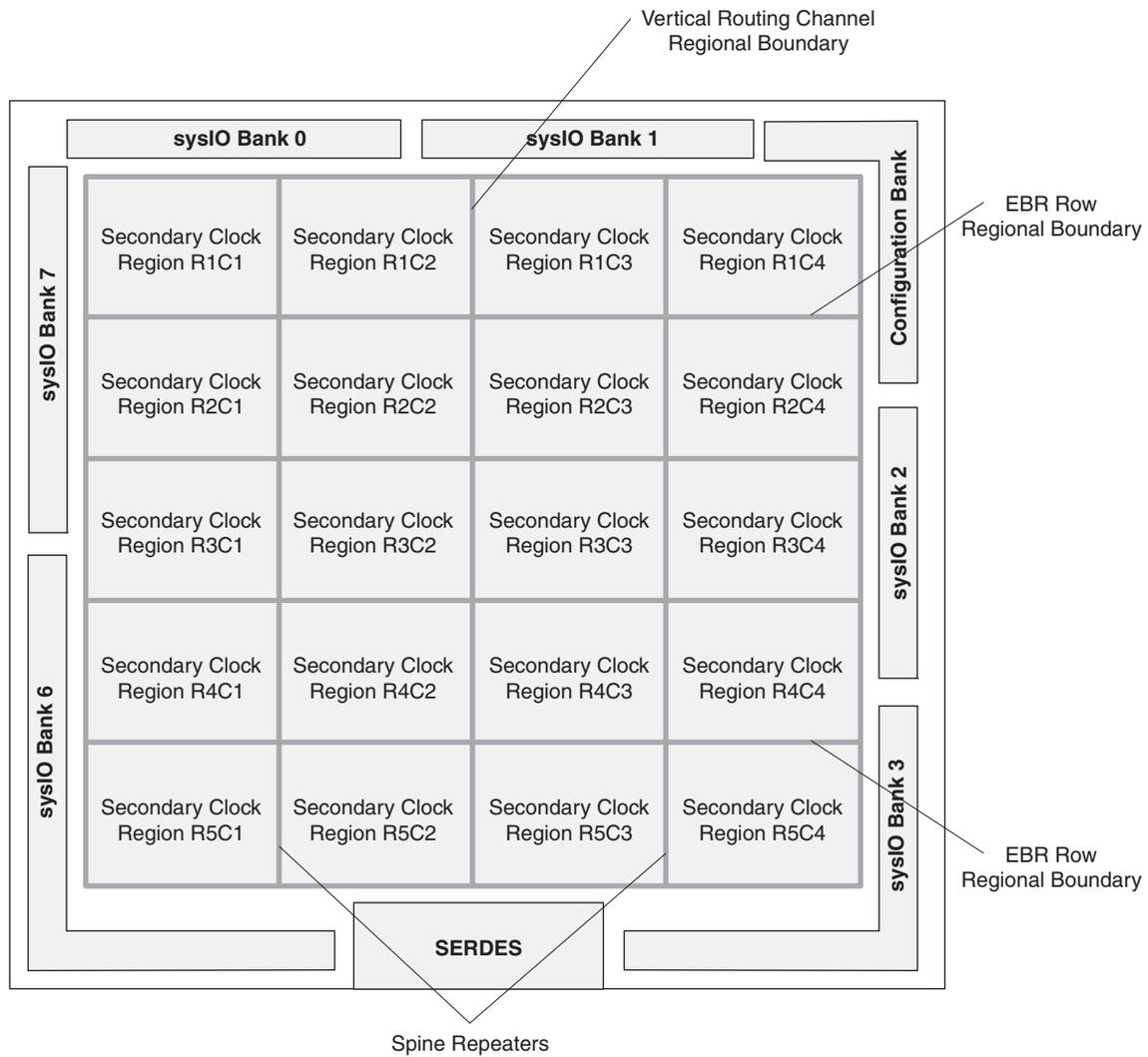
Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-6lfn1156c

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

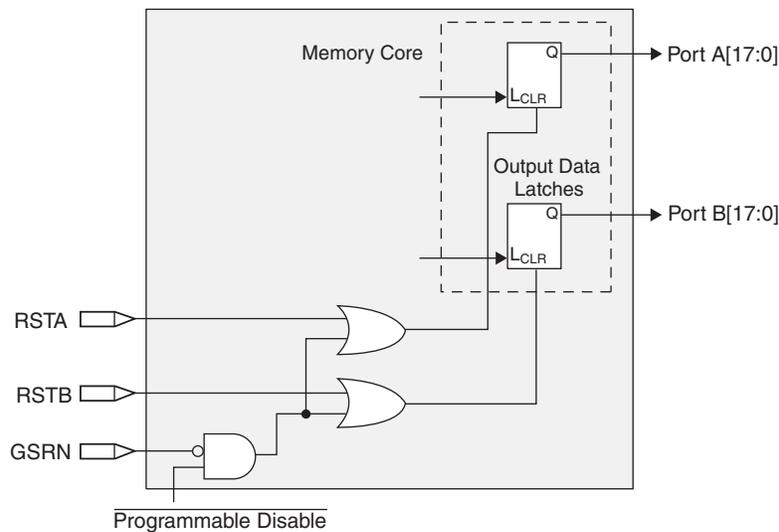
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

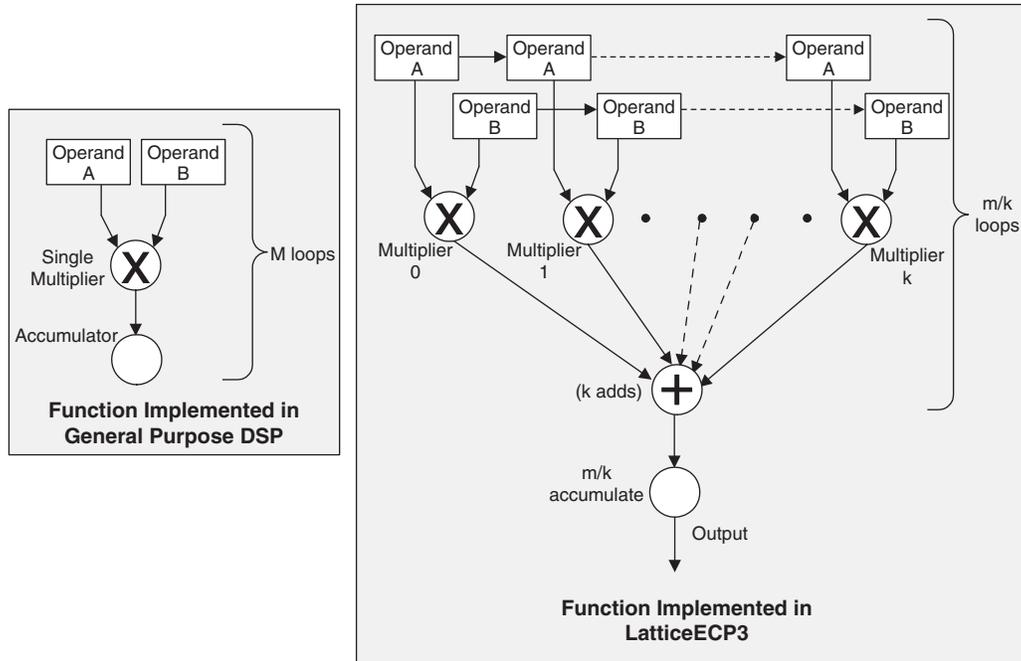
The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches



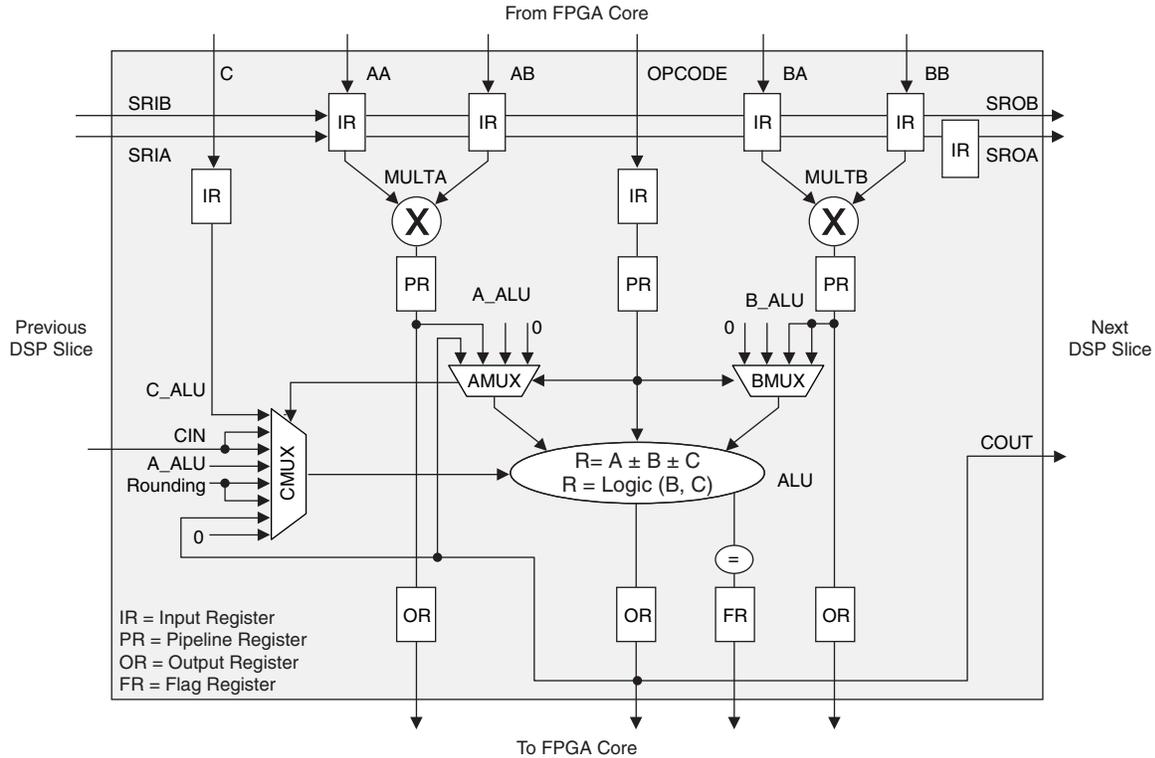
LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multipliers per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multipliers feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA, BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, please refer to TN1182, [LatticeECP3 sysDSP Usage Guide](#).

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element

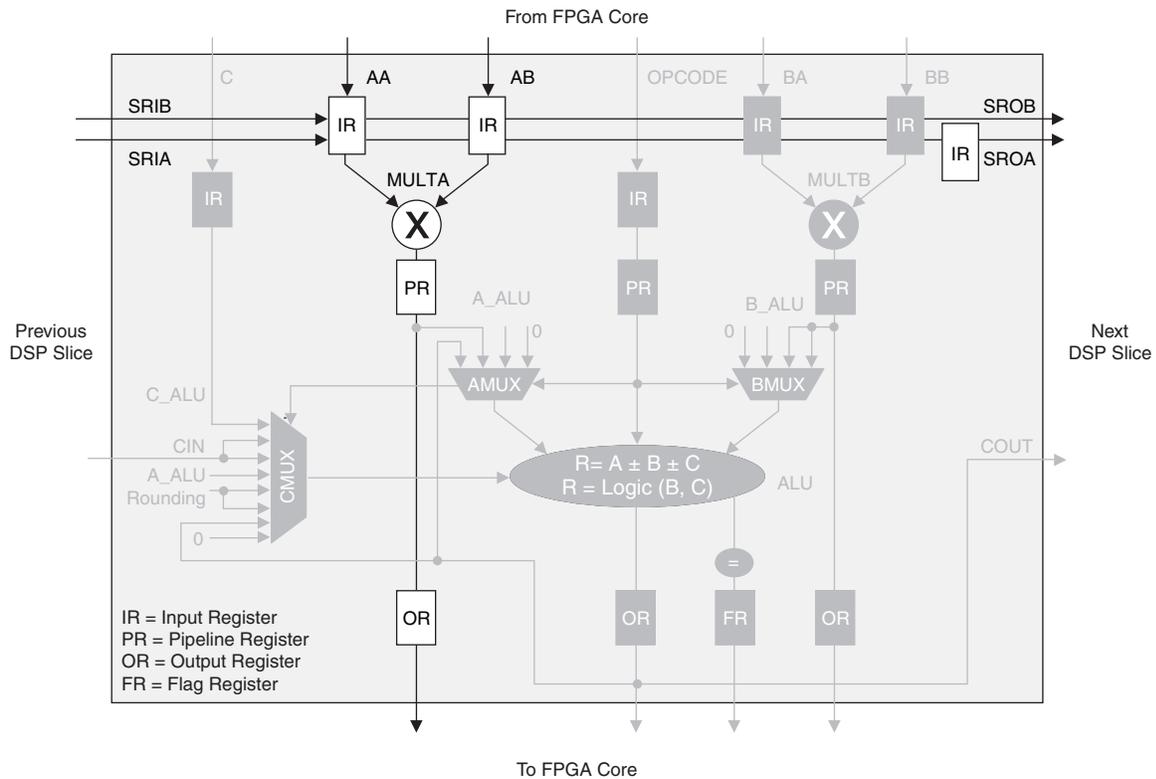
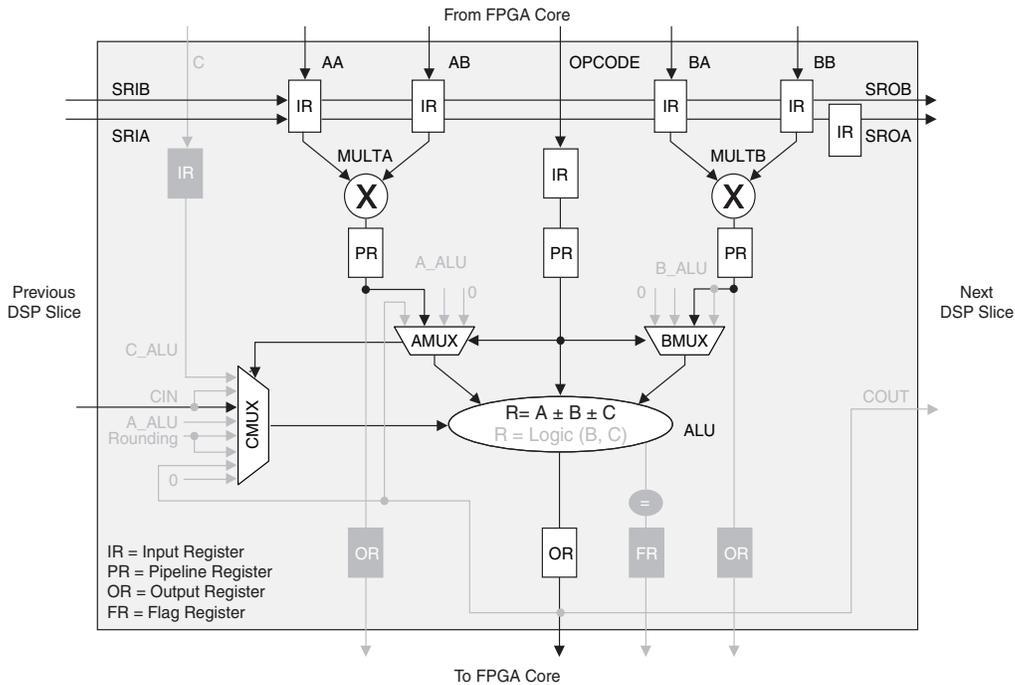


Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Please see TN1177, [LatticeECP3 sysIO Usage Guide](#) for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel $\div 1$, $\div 2$ and $\div 11$ rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

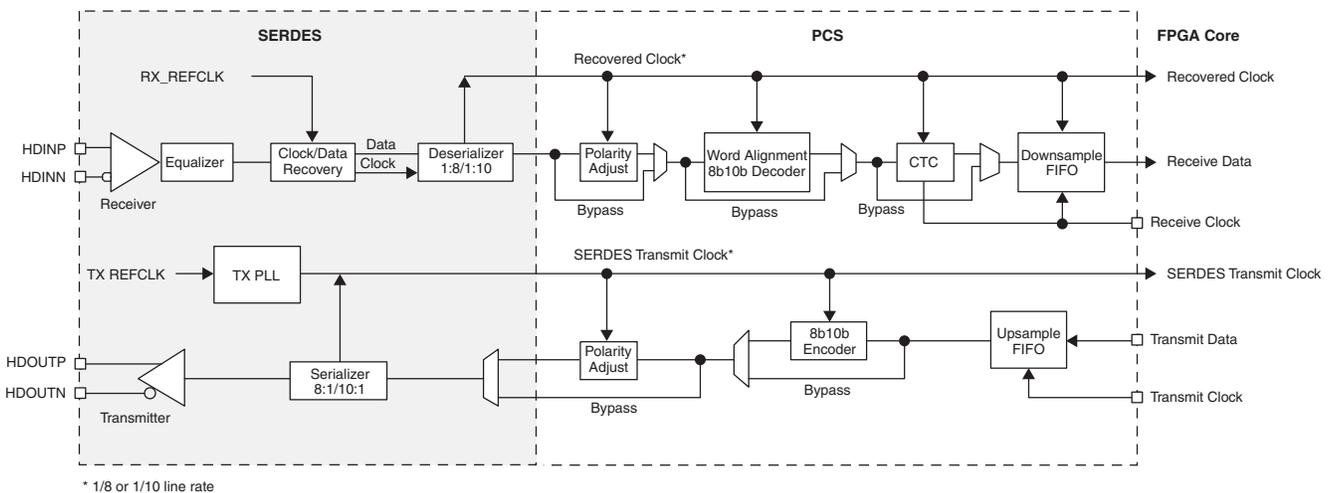
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.



LatticeECP3 Family Data Sheet

DC and Switching Characteristics

April 2014

Data Sheet DS1021

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.32 V
Supply Voltage V_{CCAUX}	-0.5 V to 3.75 V
Supply Voltage V_{CCJ}	-0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied ⁴	-0.5 V to 3.75 V
Storage Temperature (Ambient)	-65 V to 150 °C
Junction Temperature (T_J)	+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^2	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^{2,4}$	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
$V_{CCIO}^{2,3}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^2	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}^5	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply⁶				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/ μ s during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.

© 2014 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

SERDES Power Supply Requirements^{1, 2, 3}
Over Recommended Operating Conditions

Symbol	Description	Typ.	Max.	Units
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} current (per channel)	3	5	mA
I _{CCIB-SB}	Input buffer current (per channel)	—	—	mA
I _{CCOB-SB}	Output buffer current (per channel)	—	—	mA
Operating (Data Rate = 3.2 Gbps)				
I _{CCA-OP}	V _{CCA} current (per channel)	68	77	mA
I _{CCIB-OP}	Input buffer current (per channel)	5	7	mA
I _{CCOB-OP}	Output buffer current (per channel)	19	25	mA
Operating (Data Rate = 2.5 Gbps)				
I _{CCA-OP}	V _{CCA} current (per channel)	66	76	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 1.25 Gbps)				
I _{CCA-OP}	V _{CCA} current (per channel)	62	72	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 250 Mbps)				
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA
Operating (Data Rate = 150 Mbps)				
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.

2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

3. Pre-emphasis adds 20 mA to I_{CCA-OP} data.

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	683	—	688	—	690	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	—	688	—	690	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	—	688	—	690	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data Aligned at Pin (GDDR1_TX.SCLK.Aligned)¹⁰									
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA	—	335	—	338	—	341	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-70EA/95EA	—	339	—	343	—	347	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-70EA/95EA	—	339	—	343	—	347	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-35EA	—	322	—	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-35EA	—	322	—	320	—	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-17EA	—	322	—	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-17EA	—	322	—	320	—	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR1_TX.DQS.Centered)¹⁰									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	670	—	675	—	676	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	—	676	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDR2_TX.Aligned)									
Left and Right Sides									
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDR2_TX.DQSDLL.Centered)¹¹									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400	—	400	—	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400	—	400	—	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz

LatticeECP3 Internal Switching Characteristics^{1, 2, 5} (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141	—	0.145	—	0.149	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087	—	0.096	—	0.104	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066	—	-0.080	—	-0.094	—	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071	—	-0.070	—	-0.068	—	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118	—	0.098	—	0.077	—	ns
DSP Block Timing³								
t _{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t _{HI_DSP}	Input Register Hold Time	-0.17	—	-0.19	—	-0.21	—	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t _{HP_DSP}	Pipeline Register Hold Time	-1.02	—	-1.09	—	-1.15	—	ns
t _{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.67	—	-1.76	—	-1.84	—	ns
t _{COI_DSP}	Input Register Clock to Output Time	—	3.05	—	3.35	—	3.73	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t _{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t _{HOPT_DSP}	Opcode Register Hold Time	-0.20	—	-0.24	—	-0.27	—	ns
t _{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69	—	1.94	—	2.14	—	ns
t _{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.58	—	-0.80	—	-0.97	—	ns

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Figure 3-16. Jitter Transfer – 1.25 Gbps

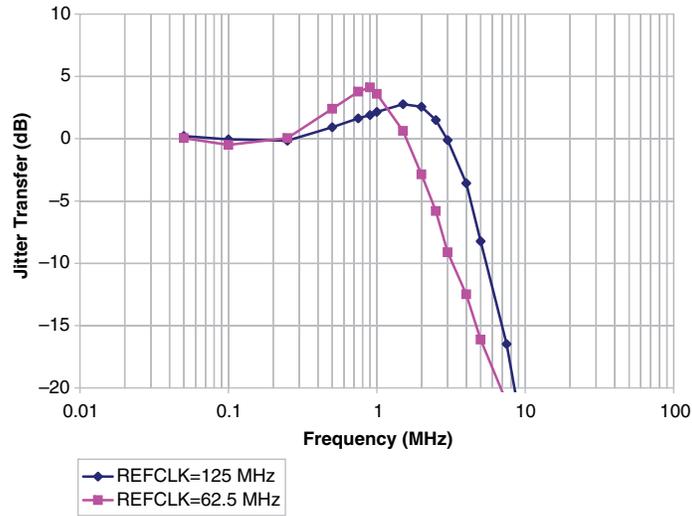


Figure 3-17. Jitter Transfer – 622 Mbps

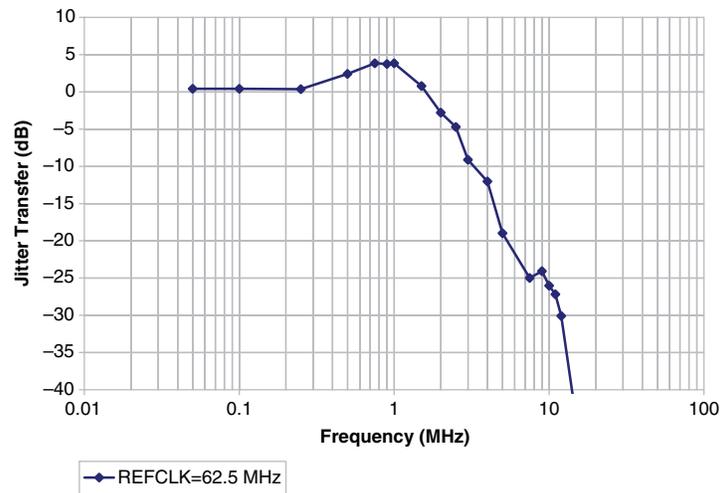
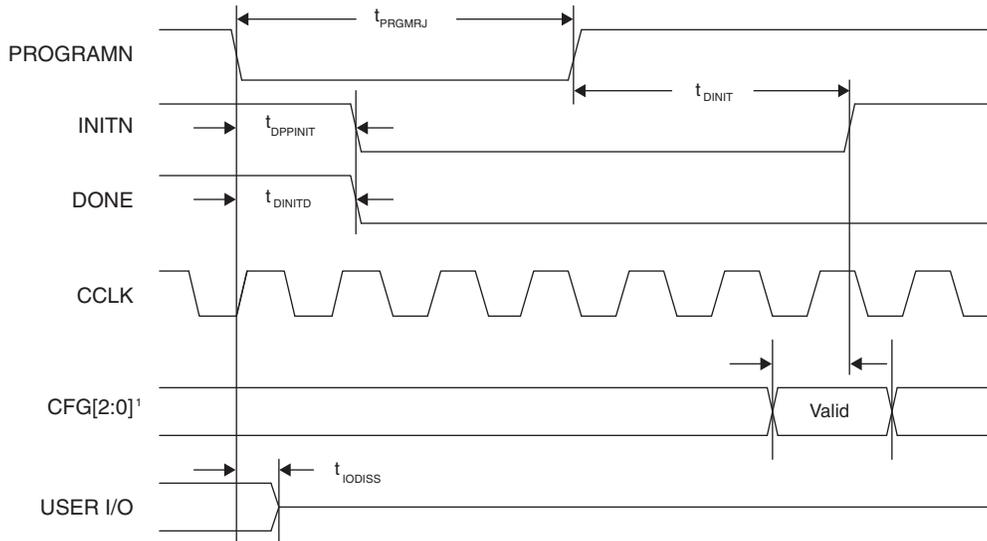
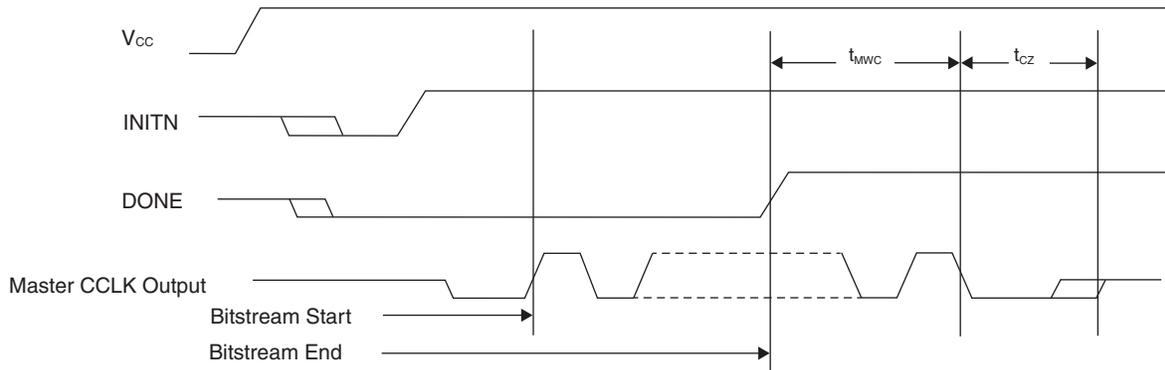


Figure 3-26. Configuration from PROGRAMN Timing

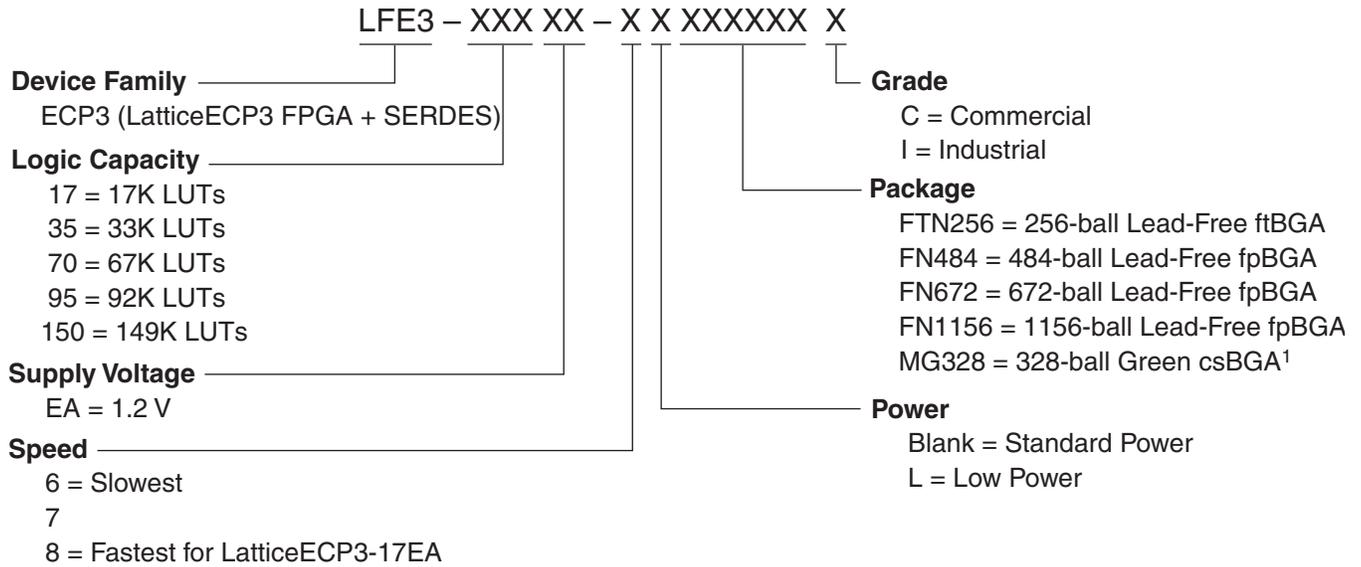


1. The CFG pins are normally static (hard wired)

Figure 3-27. Wake-Up Timing



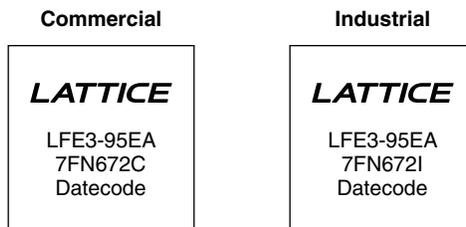
LatticeECP3 Part Number Description



1. Green = Halogen free and lead free.

Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:



Note: See [PCN 05A-12](#) for information regarding a change to the top-side mark logo.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Date	Version	Section	Change Summary
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characteristics	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI} , t_{W_EDGE} and $t_{SKEW_EDGE_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT} .
			External Reference Clock Specification (refclkp/refclkcn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$.
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC} .
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
			Updated Mini LVDS table.
August 2009	01.3	DC and Switching Characteristics	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
July 2009	01.2	Multiple	Changed references of "multi-boot" to "dual-boot" throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characteristics	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.