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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

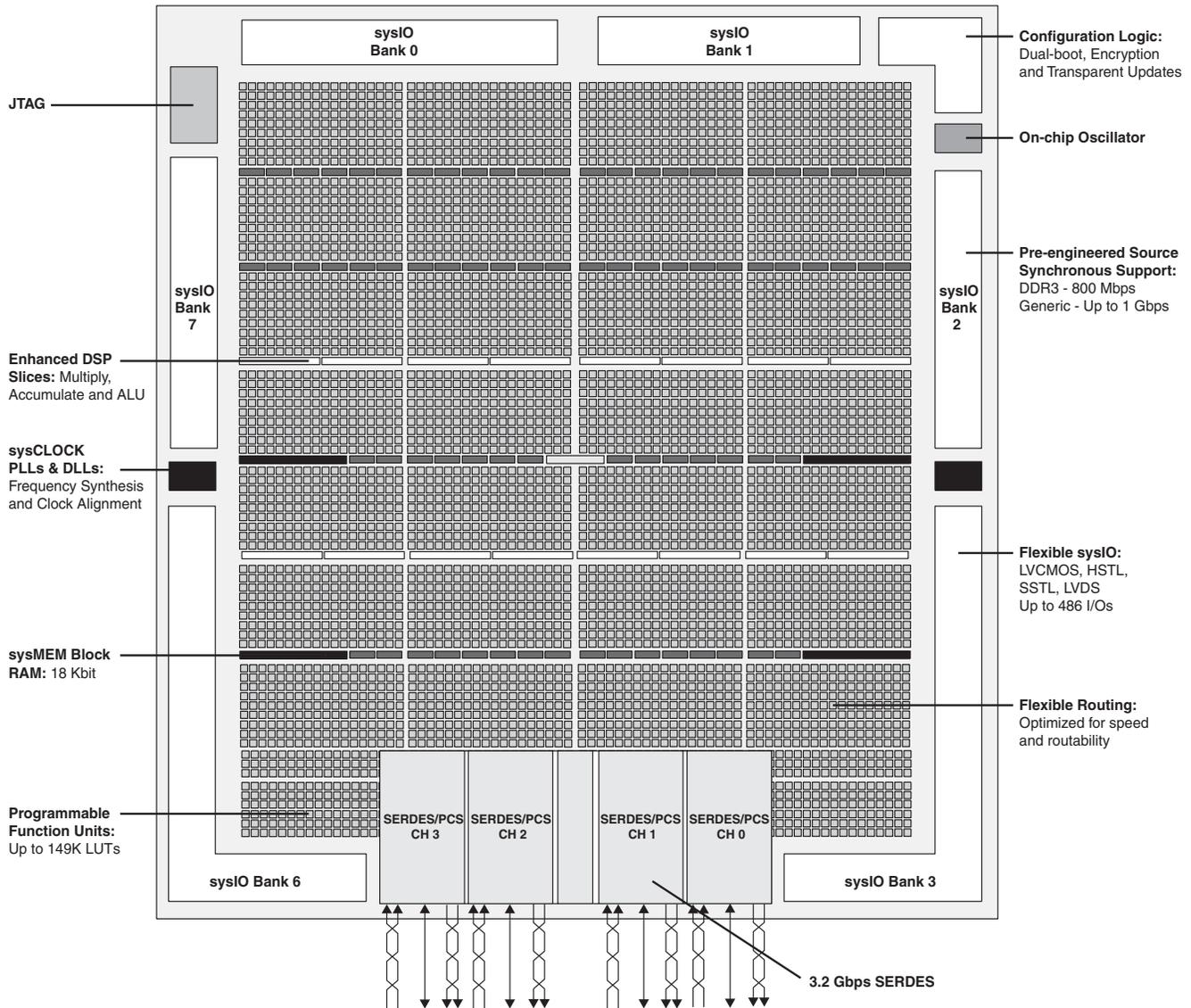
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-7fn1156c

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-4. General Purpose PLL Diagram

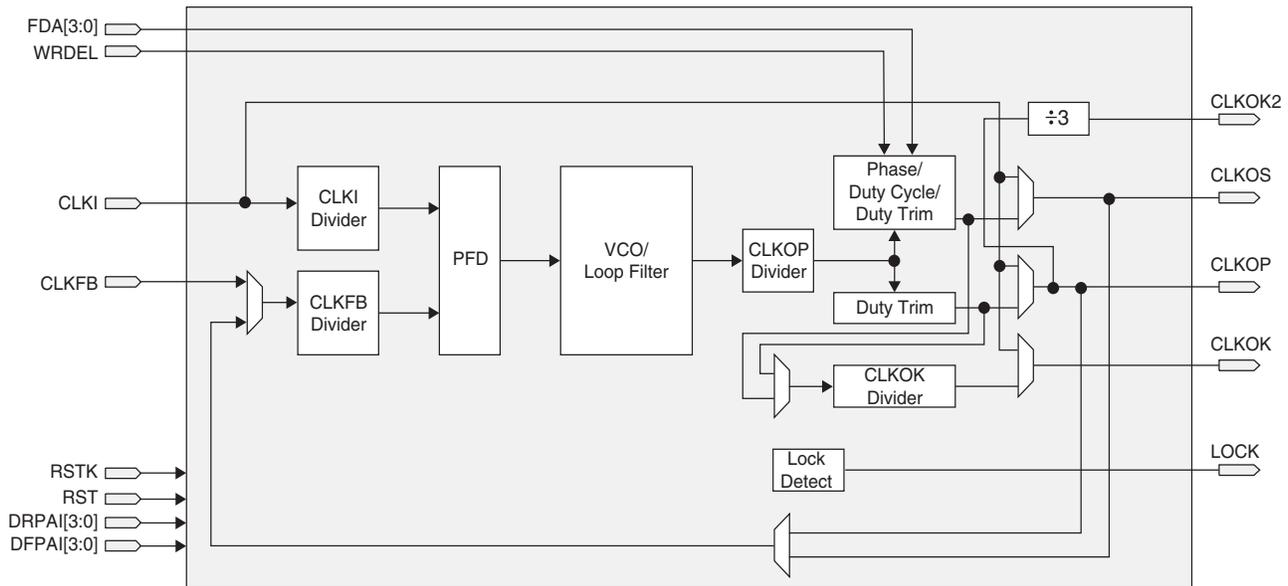


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

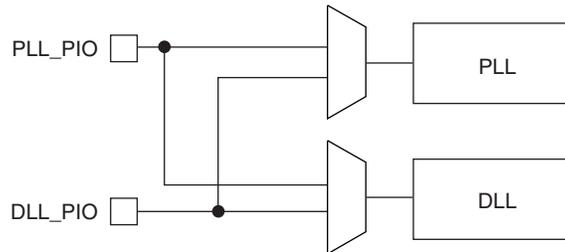
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 4$ or $\div 8$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#). Figure 2-8 shows the clock divider connections.

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions

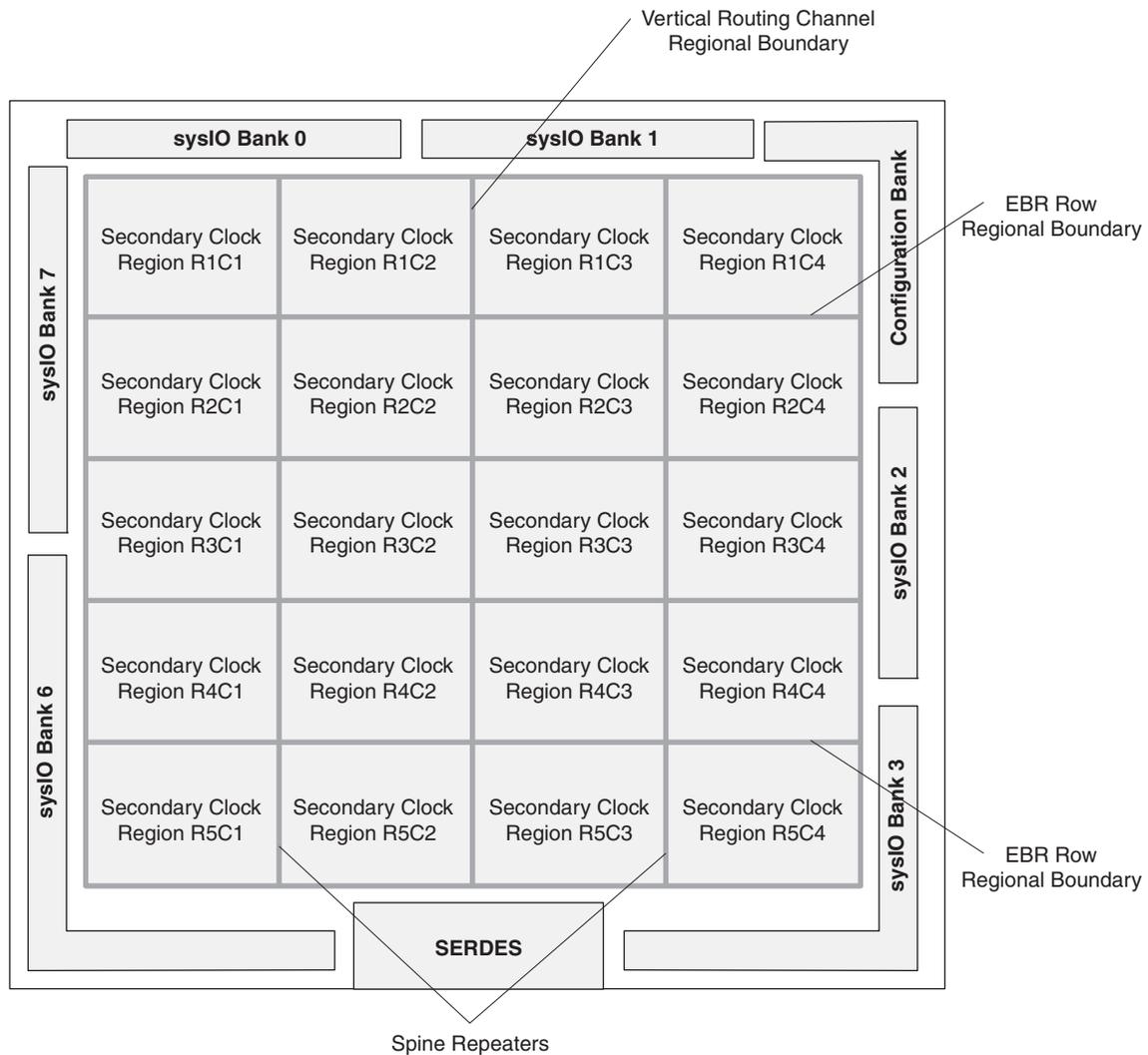
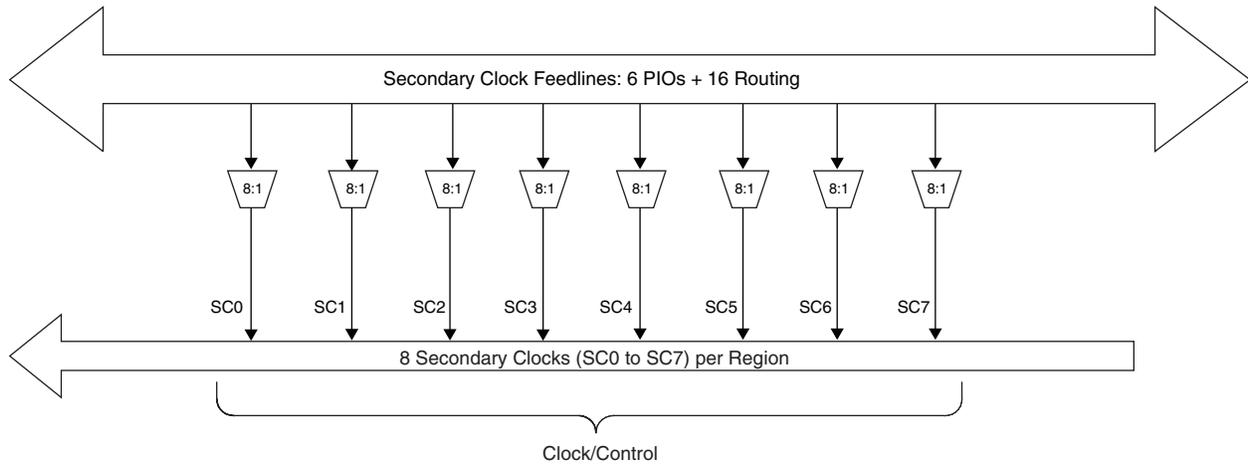


Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

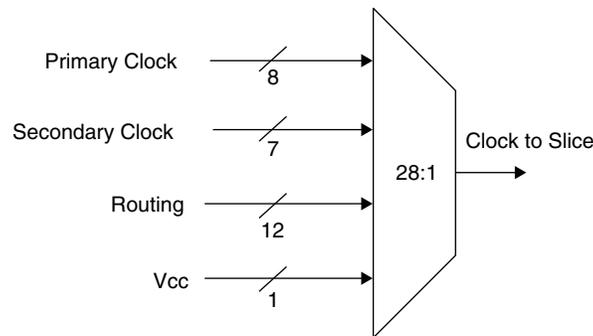
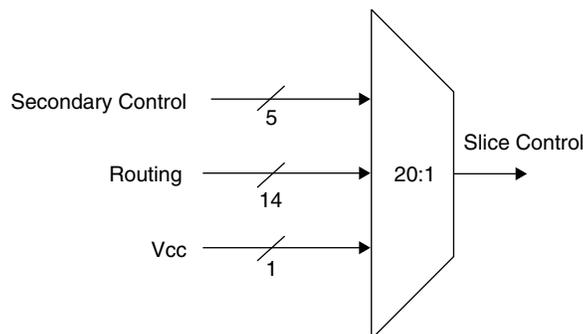


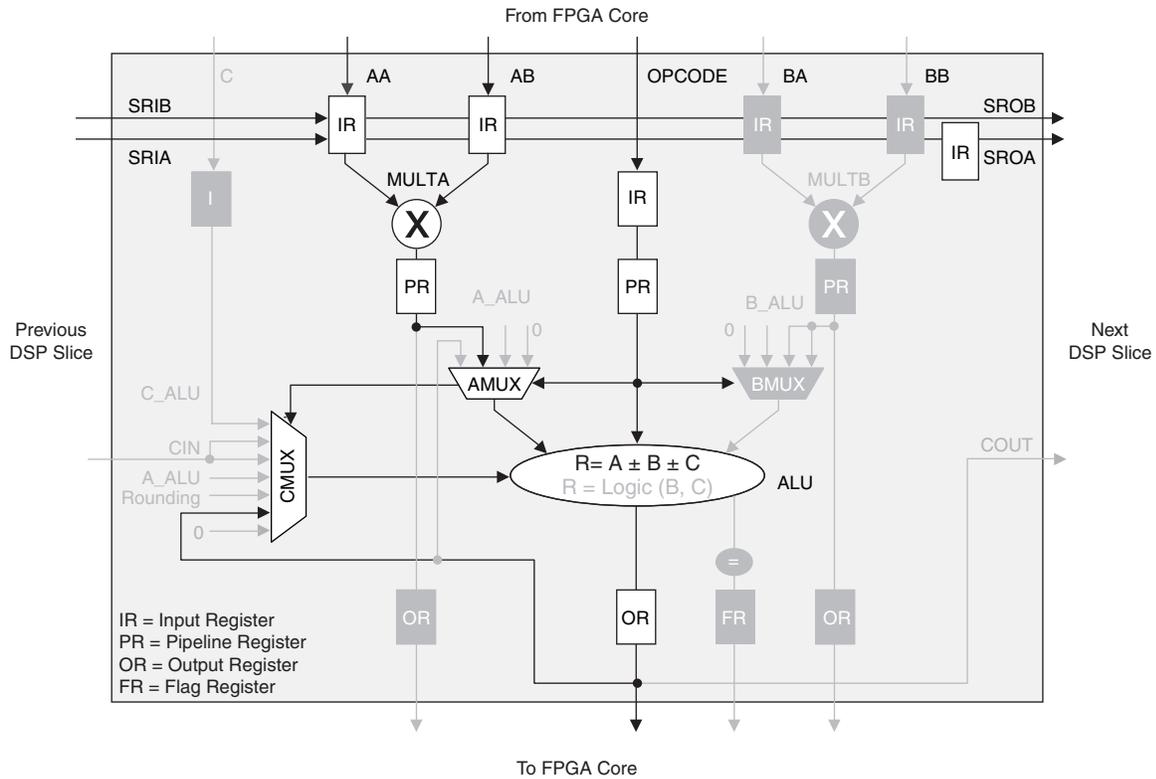
Figure 2-18. Slice0 through Slice2 Control Selection



MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

Figure 2-27. MAC DSP Element



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

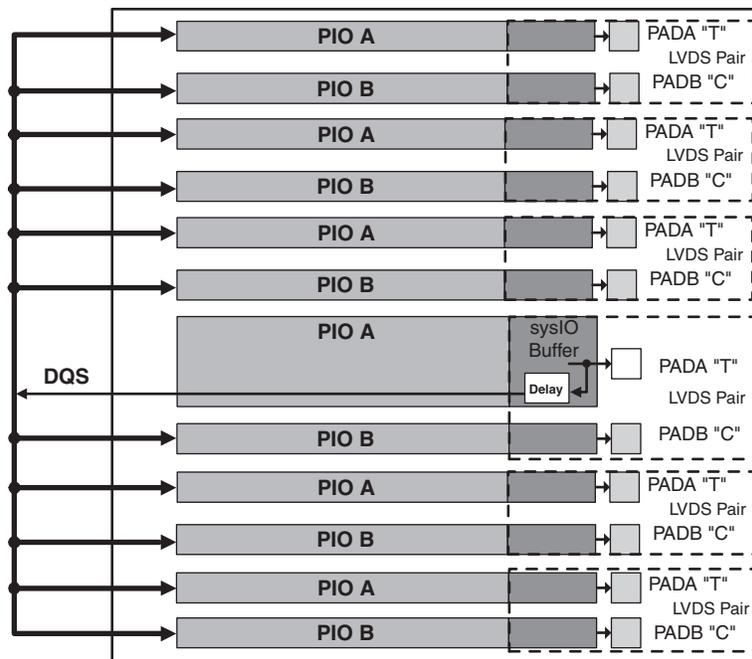
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

2. Dual-Boot Image Support

Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, [LatticeECP3 sysCONFIG Usage Guide](#).

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, [LatticeECP3 Soft Error Detection \(SED\) Usage Guide](#).

External Resistor

LatticeECP3 devices require a single external, 10 kOhm $\pm 1\%$ value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz $\pm 15\%$ CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, [LatticeECP3 sysCONFIG Usage Guide](#).

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.32 V
Supply Voltage V_{CCAUX}	-0.5 V to 3.75 V
Supply Voltage V_{CCJ}	-0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied ⁴ . . .	-0.5 V to 3.75 V
Storage Temperature (Ambient)	-65 V to 150 °C
Junction Temperature (T_J)	+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^2	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^{2,4}$	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
$V_{CCIO}^{2,3}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^2	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}^5	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply⁶				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2 \text{ V})$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2 \text{ V}) < V_{IN} \leq 3.6 \text{ V}$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-210	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (\text{MAX}) \leq V_{IN} \leq V_{CCIO}$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (\text{MAX})$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (\text{MAX})$	$V_{IL} (\text{MAX})$	—	$V_{IH} (\text{MIN})$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	7	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

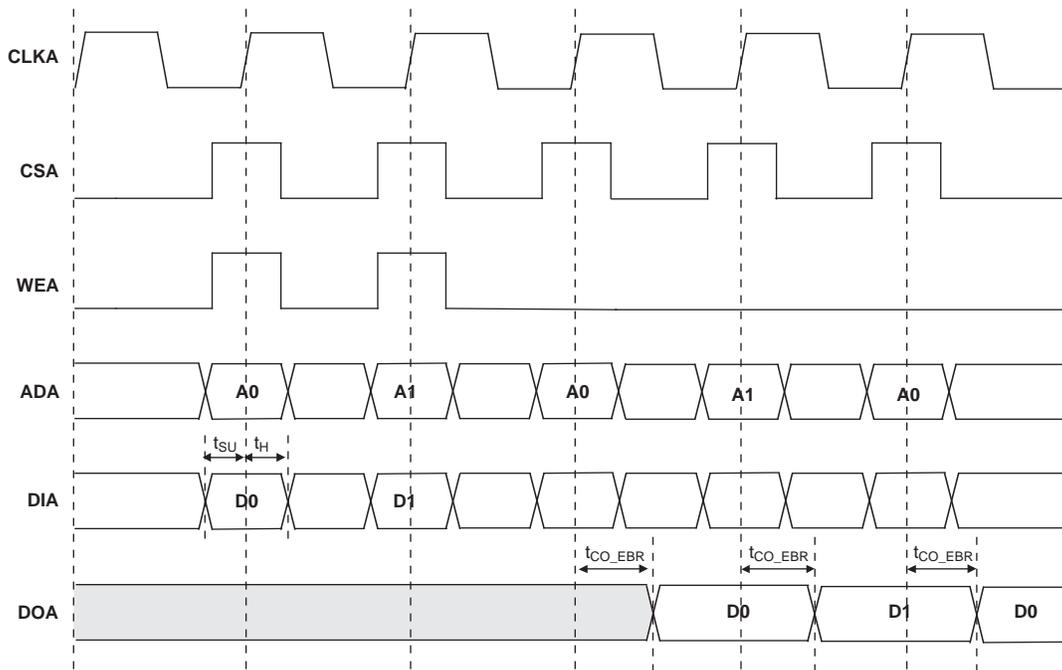
2. T_A 25 °C, $f = 1.0 \text{ MHz}$.

3. Applicable to general purpose I/Os in top and bottom banks.

4. When used as V_{REF} maximum leakage= 25 μA .

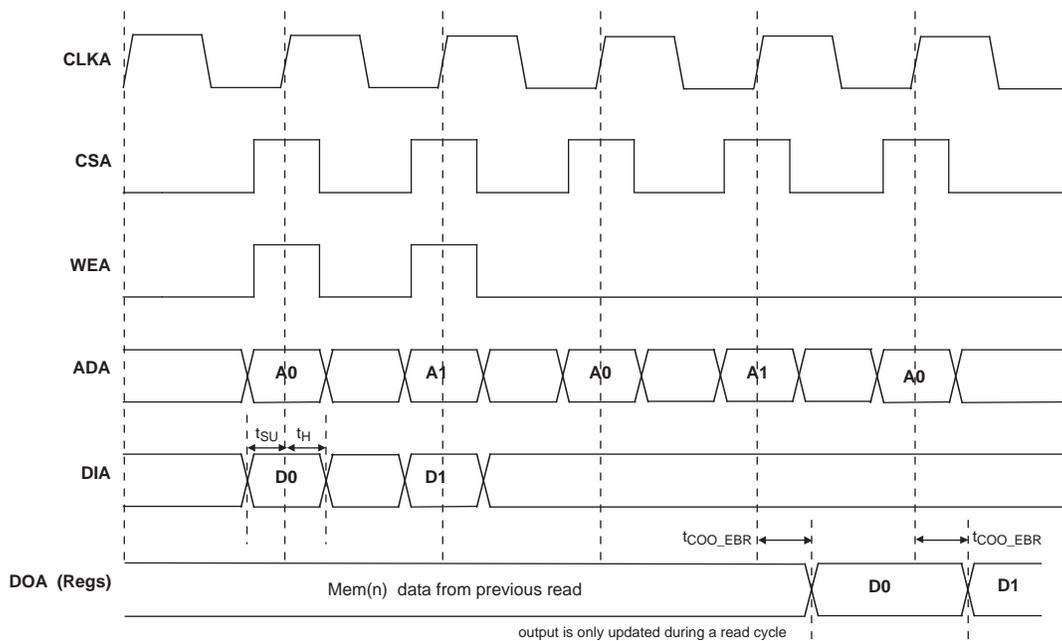
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7}
Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
Input Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
RS25	RS25, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
PPLVDS	Point-to-Point LVDS	0.03	-0.01	-0.03	ns
TRLVDS	Transition-Reduced LVDS	0.03	0.00	-0.04	ns
Mini MLVDS	Mini LVDS	0.03	-0.01	-0.03	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns
LVTTTL33	LVTTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC33	LVC33, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC25	LVC25, VCCIO = 2.5 V	0.00	0.00	0.00	ns
LVC18	LVC18, VCCIO = 1.8 V	-0.13	-0.13	-0.13	ns
LVC15	LVC15, VCCIO = 1.5 V	-0.07	-0.07	-0.07	ns
LVC12	LVC12, VCCIO = 1.2 V	-0.20	-0.19	-0.19	ns
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns
Output Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns
LVDS25	LVDS, VCCIO = 2.5 V	-0.11	-0.07	-0.03	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns

PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min	Typ	Max	Units
Transmit¹						
UI	Unit interval		399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output voltage		0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio		-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage		—	—	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection		—	—	600	mV
V _{TX-DC-CM}	Tx DC common mode voltage		0	—	V _{CCOB} + 5%	V
I _{TX-SHORT}	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	—	—	90	mA
Z _{TX-DIFF-DC}	Differential output impedance		80	100	120	Ohms
RL _{TX-DIFF}	Differential return loss		10	—	—	dB
RL _{TX-CM}	Common mode return loss		6.0	—	—	dB
T _{TX-RISE}	Tx output rise time	20 to 80%	0.125	—	—	UI
T _{TX-FALL}	Tx output fall time	20 to 80%	0.125	—	—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link		—	—	1.3	ns
T _{TX-EYE}	Transmitter eye width		0.75	—	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median		—	—	0.125	UI
Receive^{1, 2}						
UI	Unit Interval		399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage		0.34 ³	—	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage		65	—	340 ³	mV
V _{RX-CM-AC_P}	Receiver common mode voltage for AC coupling		—	—	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance		80	100	120	Ohms
Z _{RX-DC}	DC input impedance		40	50	60	Ohms
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance		200K	—	—	Ohms
RL _{RX-DIFF}	Differential return loss		10	—	—	dB
RL _{RX-CM}	Common mode return loss		6.0	—	—	dB
T _{RX-IDLE-DET-DIFF-ENTERTIME}	Maximum time required for receiver to recognize and signal an unexpected idle on link		—	—	—	ms

1. Values are measured at 2.5 Gbps.

2. Measured with external AC-coupling on the receiver.

3. Not in compliance with PCI Express 1.1 standard.

SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ^{1,2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

- Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
- Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
- All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
- The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

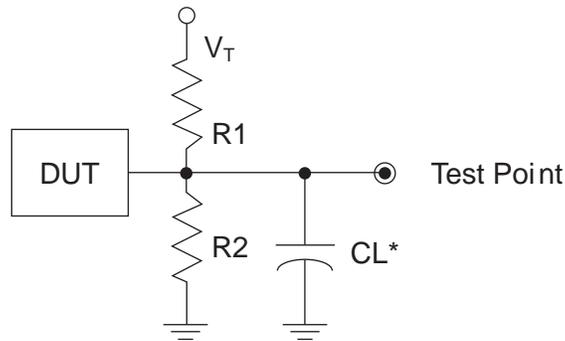
Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F _{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC _V	Duty cycle, video clock		45	50	55	%

Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Date	Version	Section	Change Summary
			Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification
December 2010	01.7EA	Multiple	Data sheet made final. Removed “preliminary” headings.
			Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices.
			Updated for Lattice Diamond design software.
		Introduction	Corrected number of user I/Os
		Architecture	Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices.
			Updated description of General Purpose PLL
			Added additional information in the Flexible Quad SERDES Architecture section.
			Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal).
			Updated Figure 2-16, Per Region Secondary Clock Selection.
			Updated description for On-Chip Programmable Termination.
			Added information about number of rows of DSP slices.
			Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes.
			Updated information for sysIO buffer pairs.
			Corrected minimum number of General Purpose PLLs (was 4, now 2).
			DC and Switching Characteristics
		Added t_{V} (clock pulse width) in External Switching Characteristics table.	
		Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table.	
		Added Jitter Transfer figures in SERDES External Reference Clock section.	
		Corrected capacitance information in the DC Electrical Characteristics table.	
		Corrected data in the Register-to-Register Performance table.	
		Corrected GDDR Parameter name HOGDDR.	
		Corrected RSDS25 -7 data in Family Timing Adders table.	
		Added footnotes 10-12 to DDR data information in the External Switching Characteristics table.	
		Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDR2 Parameters).	
		Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differential Signaling)) and 3-6 (Generic DDRX1/DDR2 (With Clock and Data Edges Aligned)).	
		Updated Supply Current table.	
		Added GDDR interface information to the External Switching and Characteristics table.	
		Added footnote to sysIO Recommended Operating Conditions table.	
		Added footnote to LVDS25 table.	
		Corrected DDR section footnotes and references.	
		Corrected Hot Socketing support from “top and bottom banks” to “top and bottom I/O pins”.	
		Pinout Information	Updated description for VTTx.

Date	Version	Section	Change Summary
March 2010	01.6	Architecture	Added Read-Before-Write information.
		DC and Switching Characteristics	Added footnote #6 to Maximum I/O Buffer Speed table.
			Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table.
		Pinout Information	Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices.
		Ordering Information	Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices.
Removed dual mark information.			
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.
			Updated Table 2-13, SERDES Standard Support to include SONET/SDH and updated footnote 2.
		DC and Switching Characteristics	Added footnote to ESD Performance table.
			Updated SERDES Power Supply Requirements table and footnotes.
			Updated Maximum I/O Buffer Speed table.
			Updated Pin-to-Pin Performance table.
			Updated sysCLOCK PLL Timing table.
			Updated DLL timing table.
			Updated High-Speed Data Transmitter tables.
			Updated High-Speed Data Receiver table.
			Updated footnote for Receiver Total Jitter Tolerance Specification table.
			Updated Periodic Receiver Jitter Tolerance Specification table.
			Updated SERDES External Reference Clock Specification table.
			Updated PCI Express Electrical and Timing AC and DC Characteristics.
			Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics.
			Updated SMPTE AC/DC Characteristics Transmit table.
			Updated Mini LVDS table.
			Updated RSDS table.
			Added Supply Current (Standby) table for EA devices.
			Updated Internal Switching Characteristics table.
			Updated Register-to-Register Performance table.
			Added HDMI Electrical and Timing Characteristics data.
		Updated Family Timing Adders table.	
		Updated sysCONFIG Port Timing Specifications table.	
Updated Recommended Operating Conditions table.			
Updated Hot Socket Specifications table.			
Updated Single-Ended DC table.			
Updated TRLVDS table and figure.			
Updated Serial Data Input Specifications table.			
Updated HDMI Transmit and Receive table.			
Ordering Information	Added LFE3-150EA "TW" devices and footnotes to the Commercial and Industrial tables.		