# E: Lattice Semiconductor Corporation - LFE3-150EA-7FN672C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-7fn672c

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# LatticeECP3 Family Data Sheet Introduction

#### February 2012

# **Features**

- Higher Logic Density for Increased System Integration
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- Embedded SERDES
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

# ■ sysDSP<sup>™</sup>

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
  - -Half 36x36, two 18x18 or four 9x9 multipliers
  - Advanced 18x36 MAC and 18x18 Multiply-
  - Multiply-Accumulate (MMAC) operations

# ■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM<sup>™</sup> Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
   Two DLLs and up to ten PLLs per device
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells

# Table 1-1. LatticeECP3™ Family Selection Guide

• Dedicated read/write levelling functionality

Data Sheet DS1021

- Dedicated gearing logic
- Source synchronous standards support
  ADC/DAC, 7:1 LVDS, XGMII
  Link Speed ADC/DAC devices
  - -High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- Programmable sysl/O<sup>™</sup> Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

# Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

# System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- · On-chip oscillator for initialization & general use
- 1.2 V core power supply

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2/2	4/2	10/2	10 / 2	10/2
Packages and SERDES Channels	/ I/O Combinatio	ns		•	
328 csBGA (10 x 10 mm)	2/116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

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chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.



Figure 2-5. Delay Locked Loop Diagram (DLL)

\* This signal is not user accessible. This can only be used to feed the slave delay line.



# Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36





Spine Repeaters



# Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



# MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

# Figure 2-27. MAC DSP Element





Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

#### Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA <sup>1</sup> , OPOSB, ONEGB <sup>1</sup>	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR <sup>1</sup>	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL <sup>1</sup>	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT <sup>1</sup>	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 <sup>1</sup> , DQCLK1 <sup>1</sup>	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW <sup>2</sup>	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID <sup>1</sup>	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

# PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

# Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.



# 2. Left and Right (Banks 2, 3, 6 and 7) sysl/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysl/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

# 3. Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysl/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end.

# Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO8}$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V<sub>CC</sub> and V<sub>CCAUX</sub> supply the power to the FPGA core fabric, whereas the V<sub>CCIO</sub> supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V<sub>CCIO</sub> supplies should be powered-up before or together with the V<sub>CC</sub> and V<sub>CCAUX</sub> supplies.

# Supported sysl/O Standards

The LatticeECP3 sysl/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysl/O buffer to support a variety of standards please see TN1177, LatticeECP3 syslO Usage Guide.



Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

# SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



# PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.



# sysl/O Single-Ended DC Electrical Characteristics

Input/Output	VIL VIH Vol		V <sub>IH</sub>		Voi	Vou		
Standard	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	l <sub>OL</sub> <sup>1</sup> (mA)	I <sub>OH</sub> <sup>1</sup> (mA)
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V <sub>CCIO</sub> - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V <sub>CCIO</sub> - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V <sub>CCIO</sub>	0.65 V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
	-03	0.35 Vacua	0.65 Vacia	36	0.4	V <sub>CCIO</sub> - 0.4	8, 4	-8, -4
	-0.5	0.00 VCCIO	0.03 VCCIO	5.0	0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
	-0.3	0.35 Vaa	0.65 Vaa	3.6	0.4	V <sub>CCIO</sub> - 0.4	6, 2	-6, -2
LVONICOTZ	-0.0	0.00 VCC	0.03 VCC	0.0	0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V <sub>CCIO</sub> - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V <sub>CCIO</sub>	0.5 V <sub>CCIO</sub>	3.6	0.1 V <sub>CCIO</sub>	0.9 V <sub>CCIO</sub>	1.5	-0.5
SSTL18_I	-0.3	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	3.6	0.4	V <sub>CCIO</sub> - 0.4	6.7	-6.7
SSTL18_II	_0.3	V0 125	V + 0.125	3.6	0.28	V 0 28	8	-8
(DDR2 Memory)	-0.5	V <sub>REF</sub> - 0.123	V <sub>REF</sub> + 0.125	5.0	0.20	V CCIO - 0.20	11	-11
SSTI 2 1	_0.3	V0 18	V \ 0.18	3.6	0.54	V	7.6	-7.6
551L2_1	-0.5	V <sub>REF</sub> - 0.10	V <sub>REF</sub> + 0.10	5.0	0.54	V CCIO - 0.02	12	-12
SSTL2_II	_0.3	V0.18	V \ 0.18	3.6	0.35	V	15.2	-15.2
(DDR Memory)	-0.5	V <sub>REF</sub> - 0.10	V <sub>REF</sub> + 0.10	5.0	0.00	V CCIO - 0.43	20	-20
SSTL3_I	-0.3	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	3.6	0.7	V <sub>CCIO</sub> - 1.1	8	-8
SSTL3_II	-0.3	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	3.6	0.5	V <sub>CCIO</sub> - 0.9	16	-16
SSTL15	0.2	V 01	V + 0.1	2.6	0.2	V <sub>CCIO</sub> - 0.3	7.5	-7.5
(DDR3 Memory)	-0.3	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	3.0	0.5	V <sub>CCIO</sub> * 0.8	9	-9
	_0.3	V01	V 101	3.6	0.4	V 0 4	4	-4
	-0.5	V <sub>REF</sub> - 0.1	VREF + 0.1	5.0	0.4	V CCIO - 0.4	8	-8
	_0.3	V01	V + 0 1	3.6	0.4	V04	8	-8
	-0.3	VREF - 0.1	VREF + 0.1	3.0	0.4	VCCIO - 0.4	12	-12
HSTL18_II	-0.3	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	3.6	0.4	V <sub>CCIO</sub> - 0.4	16	-16

1. For electromigration, the average DC current drawn by I/O pads between two consecutive V<sub>CCIO</sub> or GND pad connections, or between the last V<sub>CCIO</sub> or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed n \* 8 mA, where n is the number of I/O pads between the two consecutive bank V<sub>CCIO</sub> or GND connections or between the last V<sub>CCIO</sub> and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.



# MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.





Table 3-5. MLVDS25 DC Conditions<sup>1</sup>

		Тур	ical	
Parameter	Description	<b>Ζο=50</b> Ω	<b>Ζο=70</b> Ω	Units
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R <sub>TR</sub>	Receiver Termination (+/-1%)	50.00	70.00	Ω
V <sub>OH</sub>	Output High Voltage	1.52	1.60	V
V <sub>OL</sub>	Output Low Voltage	0.98	0.90	V
V <sub>OD</sub>	Output Differential Voltage	0.54	0.70	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.



# sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2		500	MHz
'IN	CLKFB)		Primary clock <sup>4</sup>	2		420	MHz
4	Output clock frequency (CLKOP,		Edge clock	4		500	MHz
OUT	CLKOS)		Primary clock <sup>4</sup>	4		420	MHz
f <sub>OUT1</sub>	K-Divider output frequency	CLKOK		0.03125		250	MHz
f <sub>OUT2</sub>	K2-Divider output frequency	CLKOK2		0.667		166	MHz
f <sub>VCO</sub>	PLL VCO frequency			500		1000	MHz
f <sub>PFD</sub> <sup>3</sup>	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock <sup>4</sup>	2		420	MHz
AC Charac	teristics						
t <sub>PA</sub>	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t <sub>DT</sub>	Output clock duty cycle	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f <sub>OUT</sub> > 250 MHz	Primary clock	30	50	70	%
t <sub>CPA</sub>	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t <sub>OPW</sub>	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
		$f_{OUT} \ge 420 \text{ MHz}$			_	200	ps
t <sub>OPJIT</sub> 1	Output clock period jitter	420 MHz > f <sub>OUT</sub> ≥ 100 MHz		—		250	ps
		f <sub>OUT</sub> < 100 MHz		—	—	0.025	UIPP
t <sub>SK</sub>	Input clock to output clock skew when N/M = integer			—		500	ps
. 2		2 to 25 MHz			_	200	us
LOCK_		25 to 500 MHz		—	—	50	us
t <sub>UNLOCK</sub>	Reset to PLL unlock time to ensure fast reset			_		50	ns
t <sub>HI</sub>	Input clock high time	90% to 90%		0.5		_	ns
t <sub>LO</sub>	Input clock low time	10% to 10%		0.5	_	_	ns
t <sub>IPJIT</sub>	Input clock period jitter			_	—	400	ps
	Reset signal pulse width high, RSTK			10		_	ns
<sup>I</sup> RST	Reset signal pulse width high, RST			500	_	_	ns

# **Over Recommended Operating Conditions**

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 4$  MHz. For  $f_{PFD} < 4$  MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for  $f_{PFD} < 4$  MHz.

4. When using internal feedback, maximum can be up to 500 MHz.



# **DLL** Timing

# **Over Recommended Operating Conditions**

Parameter	Description	Condition	Min.	Тур.	Max.	Units
f <sub>REF</sub>	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f <sub>FB</sub>	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f <sub>CLKOP</sub> 1	Output clock frequency, CLKOP		133	—	500	MHz
f <sub>CLKOS<sup>2</sup></sub>	Output clock frequency, CLKOS		33.3	—	500	MHz
t <sub>PJIT</sub>	Output clock period jitter (clean input)			—	200	ps p-p
	Output clock duty cycle (at 50% levels, 50% duty	Edge Clock	40		60	%
t <sub>DUTY</sub>	off, time reference delay mode)	Primary Clock	30		70	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	45		55	%
t <sub>DUTYTRD</sub>	duty cycle input clock, 50% duty cycle circuit	Primary Clock ≥ 250 MHz	30		70	%
	enabled, time reference delay mode)	Edge Clock	45		55	%
	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL	Primary Clock < 250 MHz	40		60	%
t <sub>DUTYCIR</sub> duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading		Primary Clock ≥ 250 MHz	30		70	%
	Edge Clock	45		55	%	
t <sub>SKEW</sub> <sup>3</sup>	Output clock to clock skew between two outputs with the same phase setting		_	—	100	ps
t <sub>PHASE</sub>	Phase error measured at device pads between off-chip reference clock and feedback clocks		_	—	+/-400	ps
t <sub>PWH</sub>	Input clock minimum pulse width high (at 80% level)		550	_	_	ps
t <sub>PWL</sub>	Input clock minimum pulse width low (at 20% level)		550	—	_	ps
t <sub>INSTB</sub>	Input clock period jitter			—	500	ps
t <sub>LOCK</sub>	DLL lock time		8	—	8200	cycles
t <sub>RSWD</sub>	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t <sub>DEL</sub>	Delay step size		27	45	70	ps
t <sub>RANGE1</sub>	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t <sub>RANGE4</sub>	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a "path-matching" design guideline and is not a measurable specification.



# Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).



# Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

# AC and DC Characteristics

#### Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T <sub>RF</sub>	Differential rise/fall time	20%-80%	—	80		ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance		80	100	120	Ohms
J <sub>TX_DDJ</sub> <sup>3, 4, 5</sup>	Output data deterministic jitter		_	—	0.10	UI
J <sub>TX_TJ</sub> <sup>2, 3, 4, 5</sup>	Total output data jitter			_	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 1.25 Gbps.

#### Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 1.25 GHz	10			dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 1.25 GHz	6			dB
Z <sub>RX_DIFF</sub>	Differential termination resistance		80	100	120	Ohms
J <sub>RX_DJ</sub> <sup>1, 2, 3, 4, 5</sup>	Deterministic jitter tolerance (peak-to-peak)		_	_	0.34	UI
J <sub>RX_RJ</sub> <sup>1, 2, 3, 4, 5</sup>	Random jitter tolerance (peak-to-peak)		_		0.26	UI
J <sub>RX_SJ</sub> <sup>1, 2, 3, 4, 5</sup>	Sinusoidal jitter tolerance (peak-to-peak)		_		0.11	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4, 5</sup>	Total jitter tolerance (peak-to-peak)		_	_	0.71	UI
T <sub>RX_EYE</sub>	Receiver eye opening		0.29	_	_	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 1.25 Gbps.



# Figure 3-21. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

# Figure 3-22. sysCONFIG Master Serial Port Timing









# **Signal Descriptions (Cont.)**

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals <sup>3</sup>		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	0	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	0	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm		Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm		Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.



# PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins					
For Left and Right Edges of the Device							
D[Edgo] [n 2]	А	DQ					
	В	DQ					
P[Edge] [n-2]	А	DQ					
	В	DQ					
D[Edgo] [n 1]	A	DQ					
	В	DQ					
P[Edge] [n]	А	[Edge]DQSn					
	В	DQ					
P[Edge] [n 1]	А	DQ					
	В	DQ					
D[Edgo] [n 2]	A	DQ					
r[Euge][II+2]	В	DQ					
For Top Edge of the Device							
P[Edge] [n-3]	А	DQ					
	В	DQ					
P[Edge] [n-2]	А	DQ					
	В	DQ					
P[Edge] [n-1]	А	DQ					
	В	DQ					
P[Edge] [n]	А	[Edge]DQSn					
i [⊏uge] [ii]	В	DQ					
P[Edge] [n+1]	А	DQ					
i [Euge] [iit i]	В	DQ					
P[Edge] [n 2]	А	DQ					
י נבטשכן נוידבן	В	DQ					

Note: "n" is a row PIC number.



# Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package <sup>1</sup>	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break- down table.
		Pinout Information	"Logic Signal Connections" section heading renamed "Package Pinout Information". Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V <sub>CCA</sub> signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for $\ensuremath{t_{RST}}$
		Ordering Information	Updated topside marks with new logos in the Ordering Information sec- tion.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 Exter- nal Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL TIming table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, $t_{J T}\!.$
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t <sub>SUWBEN EBB</sub> and t <sub>HWBEN EBB</sub> .
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications



Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t <sub>SKEW_PRIB</sub> to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t <sub>DINIT</sub> information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$ .
			Added footnote 4 to sysCLOCK PLL Timing table for t <sub>PFD</sub> .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Out- put Jitter, Typical Building Block Function Performance, Register-to- Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	_	Initial release.