# E: Lattice Semiconductor Corporation - LFE3-150EA-7FN672I Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-7fn672i

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# LatticeECP3 Family Data Sheet Introduction

#### February 2012

### **Features**

- Higher Logic Density for Increased System Integration
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- Embedded SERDES
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

#### ■ sysDSP<sup>™</sup>

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
  - -Half 36x36, two 18x18 or four 9x9 multipliers
  - Advanced 18x36 MAC and 18x18 Multiply-
  - Multiply-Accumulate (MMAC) operations

#### ■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM<sup>™</sup> Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
   Two DLLs and up to ten PLLs per device
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells

#### Table 1-1. LatticeECP3™ Family Selection Guide

• Dedicated read/write levelling functionality

Data Sheet DS1021

- Dedicated gearing logic
- Source synchronous standards support
   ADC/DAC, 7:1 LVDS, XGMII
   Link Speed ADC/DAC devices
  - -High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- Programmable sysl/O<sup>™</sup> Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

#### Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

#### System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- · On-chip oscillator for initialization & general use
- 1.2 V core power supply

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2/2	4/2	10/2	10 / 2	10/2
Packages and SERDES Channels	/ I/O Combinatio	ns		•	
328 csBGA (10 x 10 mm)	2/116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

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#### Figure 2-16. Per Region Secondary Clock Selection



### **Slice Clock Selection**

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

#### Figure 2-17. Slice0 through Slice2 Clock Selection



Figure 2-18. Slice0 through Slice2 Control Selection





#### Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



### MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

#### Figure 2-27. MAC DSP Element





### ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

### **Clock, Clock Enable and Reset Resources**

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

### **Resources Available in the LatticeECP3 Family**

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

#### Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA <sup>1</sup> , OPOSB, ONEGB <sup>1</sup>	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR <sup>1</sup>	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL <sup>1</sup>	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT <sup>1</sup>	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 <sup>1</sup> , DQCLK1 <sup>1</sup>	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW <sup>2</sup>	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID <sup>1</sup>	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

### PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.



### **On-Chip Programmable Termination**

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

#### Figure 2-39. On-Chip Termination



Programmable resistance (40, 50 and 60 Ohms)
Parallel Single-Ended Input

Differential Input

See Table 2-12 for termination options for input modes.

#### Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT <sup>1, 2</sup>	DIFFERENTIAL TERMINATION RESISTOR <sup>1</sup>
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature. Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in

an I/O bank.

On-chip termination tolerance +/- 20%

2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.



Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

### **Equalization Filter**

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

### **Hot Socketing**

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

### SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel  $\div$ 1,  $\div$ 2 and  $\div$ 11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.



### SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

### Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

#### Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI



MCCLK (MHz)	MCCLK (MHz)
	10
2.5 <sup>1</sup>	13
4.3	15 <sup>2</sup>
5.4	20
6.9	26
8.1	33 <sup>3</sup>
9.2	

 Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

### **Density Shifting**

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the LatticeECP3 Pin Migration Tables and Diamond software for specific restrictions and limitations.



### **Typical Building Block Function Performance**

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)<sup>1, 2, 3</sup>

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

### Register-to-Register Performance<sup>1, 2, 3</sup>

Function	–8 Timing	Units			
Basic Functions					
16-bit Decoder	500	MHz			
32-bit Decoder	500	MHz			
64-bit Decoder	500	MHz			
4:1 MUX	500	MHz			
8:1 MUX	500	MHz			
16:1 MUX	500	MHz			
32:1 MUX	445	MHz			
8-bit adder	500	MHz			
16-bit adder	500	MHz			
64-bit adder	305	MHz			
16-bit counter	500	MHz			
32-bit counter	460	MHz			
64-bit counter	320	MHz			
64-bit accumulator	315	MHz			
Embedded Memory Functions					
512x36 Single Port RAM, EBR Output Registers	340	MHz			
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz			
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	130	MHz			
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz			
Distributed Memory Functions					
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz			
32x4 Pseudo-Dual Port RAM	500	MHz			
64x8 Pseudo-Dual Port RAM	400	MHz			
DSP Function					
18x18 Multiplier (All Registers)	400	MHz			
9x9 Multiplier (All Registers)	400	MHz			
36x36 Multiply (All Registers)	260	MHz			



# LatticeECP3 Internal Switching Characteristics<sup>1, 2, 5</sup>

		-	8	_	7	-	6	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
PFU/PFF Logi	PFU/PFF Logic Mode Timing							
t <sub>LUT4_PFU</sub>	LUT4 delay (A to D inputs to F output)	—	0.147	_	0.163	_	0.179	ns
t <sub>LUT6_PFU</sub>	LUT6 delay (A to D inputs to OFX output)	—	0.281		0.335	_	0.379	ns
t <sub>LSR_PFU</sub>	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t <sub>LSRREC_PFU</sub>	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t <sub>SUM_PFU</sub>	Clock to Mux (M0,M1) Input Setup Time	0.134	_	0.144	_	0.153		ns
t <sub>HM_PFU</sub>	Clock to Mux (M0,M1) Input Hold Time	-0.097	_	-0.103	_	-0.109	_	ns
t <sub>SUD_PFU</sub>	Clock to D input setup time	0.061	_	0.068	_	0.075		ns
t <sub>HD_PFU</sub>	Clock to D input hold time	0.019	_	0.013	_	0.015		ns
t <sub>CK2Q_PFU</sub>	Clock to Q delay, (D-type Register Configuration)	_	0.243	_	0.273	_	0.303	ns
PFU Dual Port	Memory Mode Timing							
t <sub>CORAM_PFU</sub>	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t <sub>SUDATA_PFU</sub>	Data Setup Time	-0.137	_	-0.155	_	-0.174		ns
t <sub>HDATA_PFU</sub>	Data Hold Time	0.188	_	0.217	_	0.246	_	ns
t <sub>SUADDR_PFU</sub>	Address Setup Time	-0.227	_	-0.257	_	-0.286		ns
t <sub>HADDR_PFU</sub>	Address Hold Time	0.240	_	0.275	_	0.310	_	ns
t <sub>SUWREN_PFU</sub>	Write/Read Enable Setup Time	-0.055		-0.055	-	-0.063	_	ns
t <sub>HWREN_</sub> PFU	Write/Read Enable Hold Time	0.059	_	0.059	_	0.071	_	ns
PIC Timing								
PIO Input/Out	out Buffer Timing							
t <sub>IN_PIO</sub>	Input Buffer Delay (LVCMOS25)		0.423		0.466		0.508	ns
t <sub>OUT_PIO</sub>	Output Buffer Delay (LVCMOS25)	—	1.241	_	1.301	_	1.361	ns
IOLOGIC Inpu	t/Output Timing							
t <sub>SUI_PIO</sub>	Input Register Setup Time (Data Before Clock)	0.956		1.124		1.293		ns
t <sub>HI_PIO</sub>	Input Register Hold Time (Data after Clock)	0.225		0.184		0.240		ns
t <sub>COO_PIO</sub>	Output Register Clock to Output Delay <sup>4</sup>	-	1.09	-	1.16	-	1.23	ns
t <sub>SUCE_PIO</sub>	Input Register Clock Enable Setup Time	0.220	_	0.185	_	0.150	_	ns
t <sub>HCE_PIO</sub>	Input Register Clock Enable Hold Time	-0.085		-0.072		-0.058		ns
t <sub>SULSR_PIO</sub>	Set/Reset Setup Time	0.117	_	0.103	_	0.088	_	ns
t <sub>HLSR_PIO</sub>	Set/Reset Hold Time	-0.107	_	-0.094	_	-0.081	_	ns
EBR Timing								
t <sub>CO_EBR</sub>	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t <sub>COO_EBR</sub>	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t <sub>SUDATA_EBR</sub>	Setup Data to EBR Memory	-0.218	_	-0.227	_	-0.237	_	ns
t <sub>HDATA_EBR</sub>	Hold Data to EBR Memory	0.249		0.257		0.265	—	ns
t <sub>SUADDR_EBR</sub>	Setup Address to EBR Memory	-0.071		-0.070		-0.068		ns
t <sub>HADDR_EBR</sub>	Hold Address to EBR Memory	0.118		0.098		0.077		ns
t <sub>SUWREN_EBR</sub>	Setup Write/Read Enable to EBR Memory	-0.107	_	-0.106	_	-0.106	—	ns

### **Over Recommended Commercial Operating Conditions**







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



# LatticeECP3 Family Timing Adders<sup>1, 2, 3, 4, 5, 7</sup> (Continued)

<b>Over Recommended Commercial</b>	Operating	Conditions
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Buffer Type	Description	-8	-7	-6	Units
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	-0.12	-0.13	-0.14	ns

1. Timing adders are characterized but not tested on every device.

2. LVCMOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.

5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

6. This data does not apply to the LatticeECP3-17EA device.

7. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



### sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2		500	MHz
'IN	CLKFB)		Primary clock <sup>4</sup>	2		420	MHz
f	Output clock frequency (CLKOP,		Edge clock	4	_	500	MHz
OUT	CLKOS)		Primary clock <sup>4</sup>	4	_	420	MHz
f <sub>OUT1</sub>	K-Divider output frequency	CLKOK		0.03125	_	250	MHz
f <sub>OUT2</sub>	K2-Divider output frequency	CLKOK2		0.667	_	166	MHz
f <sub>VCO</sub>	PLL VCO frequency			500	_	1000	MHz
f <sub>PFD</sub> <sup>3</sup>	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock <sup>4</sup>	2	_	420	MHz
AC Charac	teristics					-	
t <sub>PA</sub>	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t <sub>DT</sub>	CLKOS at 50% setting)	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f <sub>OUT</sub> > 250 MHz	Primary clock	30	50	70	%
t <sub>CPA</sub>	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t <sub>OPW</sub>	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
		$f_{OUT} \ge 420 \text{ MHz}$		—	_	200	ps
t <sub>OPJIT</sub> 1	Output clock period jitter	420 MHz > f <sub>OUT</sub> ≥ 100 MHz		_	_	250	ps
		f <sub>OUT</sub> < 100 MHz		—	_	0.025	UIPP
t <sub>SK</sub>	Input clock to output clock skew when N/M = integer			_		500	ps
+ 2	Look time	2 to 25 MHz		—	_	200	us
LOCK		25 to 500 MHz		—		50	us
t <sub>UNLOCK</sub>	Reset to PLL unlock time to ensure fast reset			_		50	ns
t <sub>HI</sub>	Input clock high time	90% to 90%		0.5	_	—	ns
t <sub>LO</sub>	Input clock low time	10% to 10%		0.5	_	—	ns
t <sub>IPJIT</sub>	Input clock period jitter			—	_	400	ps
	Reset signal pulse width high, RSTK			10		_	ns
'RST	Reset signal pulse width high, RST			500	_	_	ns

#### **Over Recommended Operating Conditions**

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 4$  MHz. For  $f_{PFD} < 4$  MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for  $f_{PFD} < 4$  MHz.

4. When using internal feedback, maximum can be up to 500 MHz.



#### Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



### Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

### **AC and DC Characteristics**

### Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T <sub>RF</sub> <sup>1</sup>	Differential rise/fall time	20%-80%	—	80	—	ps
Z <sub>TX_DIFF_DC</sub>	Differential impedance		80	100	120	Ohms
J <sub>TX_DDJ</sub> <sup>3, 4, 5</sup>	Output data deterministic jitter		_	_	0.17	UI
J <sub>TX_TJ</sub> <sup>2, 3, 4, 5</sup>	Total output data jitter		_	_	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 2.5 Gbps.

#### Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL <sub>RX_DIFF</sub>	Differential return loss	From 100 MHz to 2.5 GHz	10	_	_	dB
RL <sub>RX_CM</sub>	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z <sub>RX_DIFF</sub>	Differential termination resistance		80	100	120	Ohms
J <sub>RX_DJ</sub> <sup>2, 3, 4, 5</sup>	Deterministic jitter tolerance (peak-to-peak)		_	—	0.37	UI
J <sub>RX_RJ</sub> <sup>2, 3, 4, 5</sup>	Random jitter tolerance (peak-to-peak)		_	_	0.18	UI
J <sub>RX_SJ</sub> <sup>2, 3, 4, 5</sup>	Sinusoidal jitter tolerance (peak-to-peak)		_	_	0.10	UI
J <sub>RX_TJ</sub> <sup>1, 2, 3, 4, 5</sup>	Total jitter tolerance (peak-to-peak)		_	_	0.65	UI
T <sub>RX_EYE</sub>	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.



### **Switching Test Conditions**

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

### Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards



\*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Te	est Fixture Required	Components,	Non-Terminated Interfaces
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Test Condition	R <sub>1</sub>	R <sub>2</sub>	CL	Timing Ref.	V <sub>T</sub>
LVTTL and other LVCMOS settings (L -> H, H -> L)		8		LVCMOS 3.3 = 1.5V	
				LVCMOS 2.5 = $V_{CCIO}/2$	
	$\infty$		0 pF	LVCMOS 1.8 = V <sub>CCIO</sub> /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	_
LVCMOS 2.5 I/O (Z -> H)	8	1MΩ	0 pF	V <sub>CCIO</sub> /2	
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	$\infty$	0 pF	V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H -> Z)	8	100	0 pF	V <sub>OH</sub> - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	x	0 pF	V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.



# **Pin Information Summary**

Pin Information Summary		ECP3-17EA			ECP3-35EA			ECP3-70EA		
Pin Tyr	De	256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
	Bank 0	26	20	36	26	42	48	42	60	86
	Bank 1	14	10	24	14	36	36	36	48	78
	Bank 2	6	7	12	6	24	24	24	34	36
General Purpose	Bank 3	18	12	44	16	54	59	54	59	86
	Bank 6	20	11	44	18	63	61	63	67	86
	Bank 7	19	26	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24	24
	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4	4	8	8
General Purpose Inputs	Bank 3	0	0	0	2	4	4	4	12	12
per Bank	Bank 6	0	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0	0
	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
General Purpose Out-	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0	0
Total Single-Ended User	I/O	133	116	222	133	295	310	295	380	490
VCC		6	16	16	6	16	32	16	32	32
VCCAUX		4	5	8	4	8	12	8	12	16
VTT		4	7	4	4	4	4	4	4	8
VCCA		4	6	4	4	4	8	4	8	16
VCCPLL		2	2	4	2	4	4	4	4	4
	Bank 0	2	3	2	2	2	4	2	4	4
	Bank 1	2	3	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	2	4	2	4	4
VCCIO	Bank 3	2	3	2	2	2	4	2	4	4
	Bank 6	2	3	2	2	2	4	2	4	4
	Bank 7	2	3	2	2	2	4	2	4	4
	Bank 8	1	2	2	1	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139	98	139	233
NC		0	0	73	0	0	96	0	0	238
Reserved <sup>1</sup>		0	0	2	0	2	2	2	2	2
SERDES		26	18	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672	484	672	1156



Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW <sup>1</sup>	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW <sup>1</sup>	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW <sup>1</sup>	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW <sup>1</sup>	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW <sup>1</sup>	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW <sup>1</sup>	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.