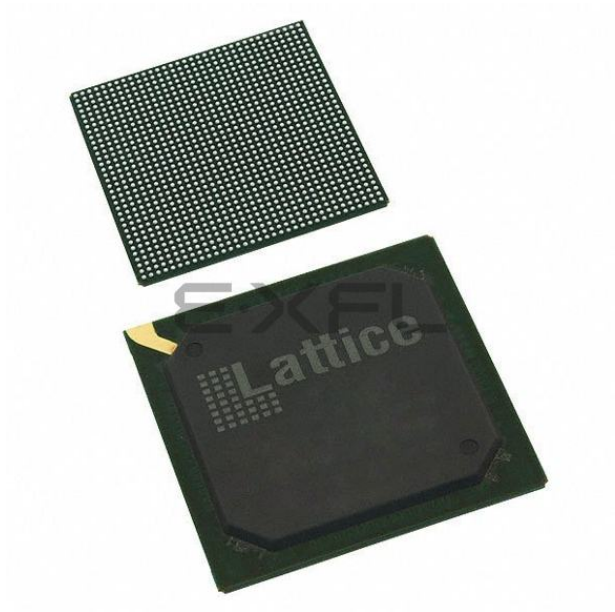
Lattice Semiconductor Corporation - LFE3-150EA-7LFN1156C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-7lfn1156c

Figure 2-4. General Purpose PLL Diagram

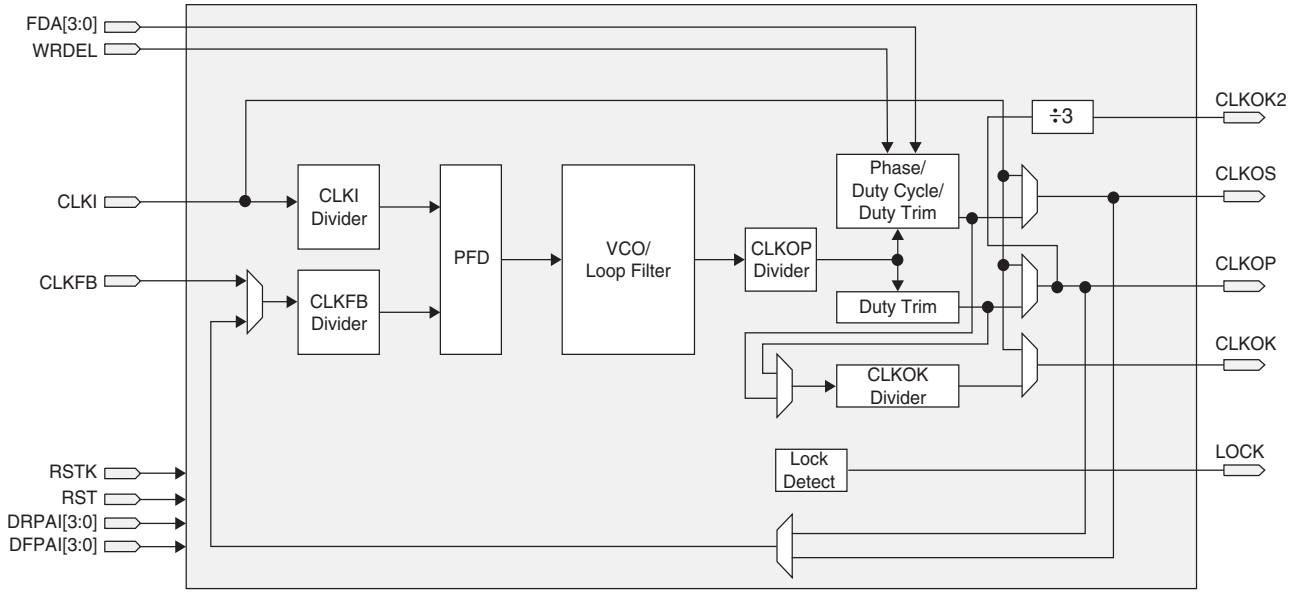


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	“1” to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	“1” to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	“1” indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

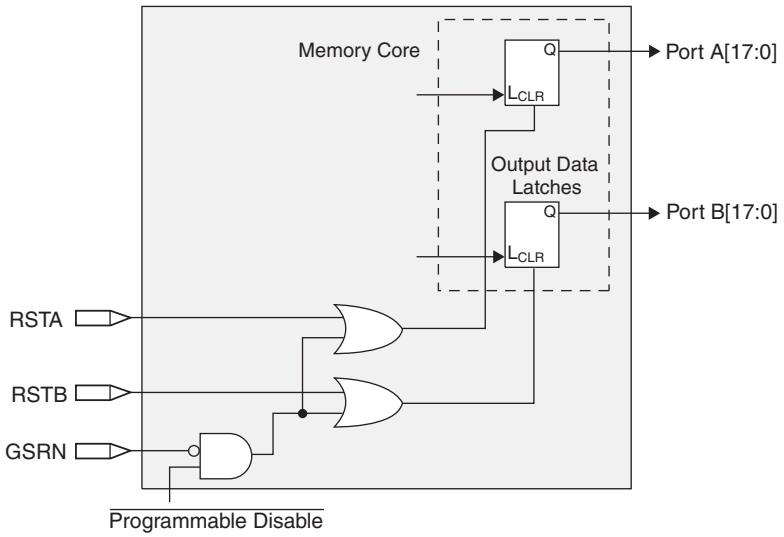
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

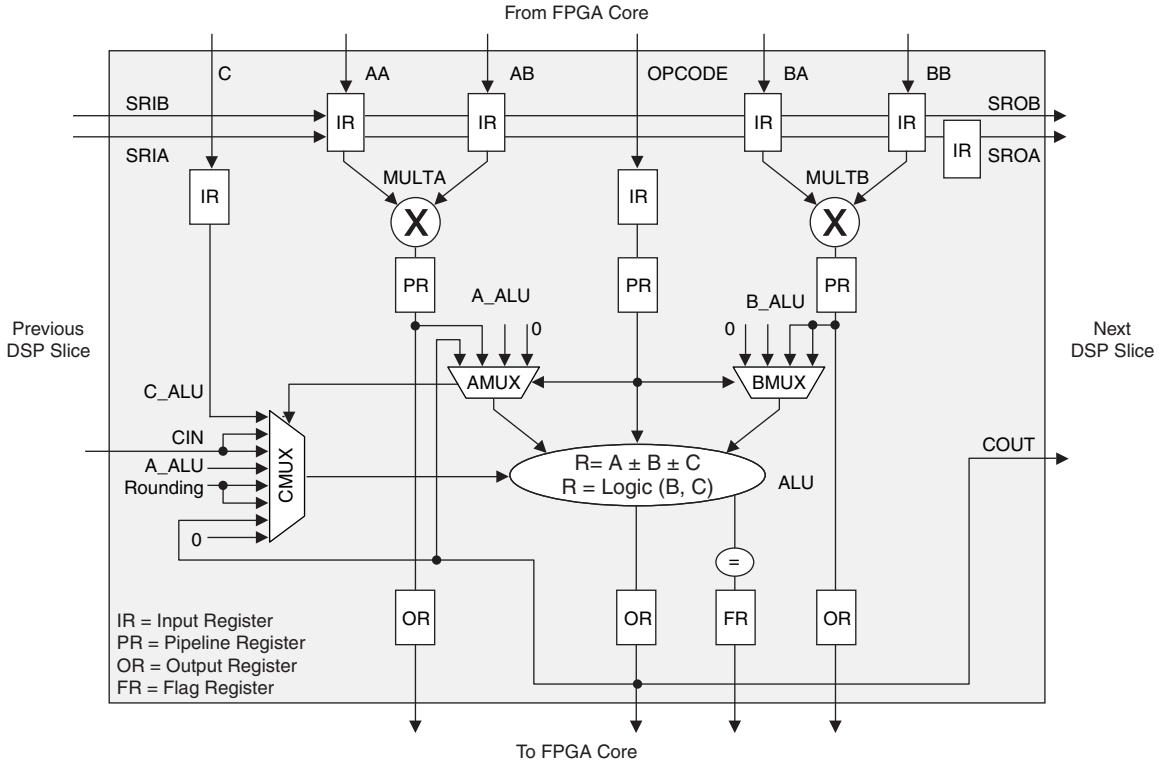
sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB

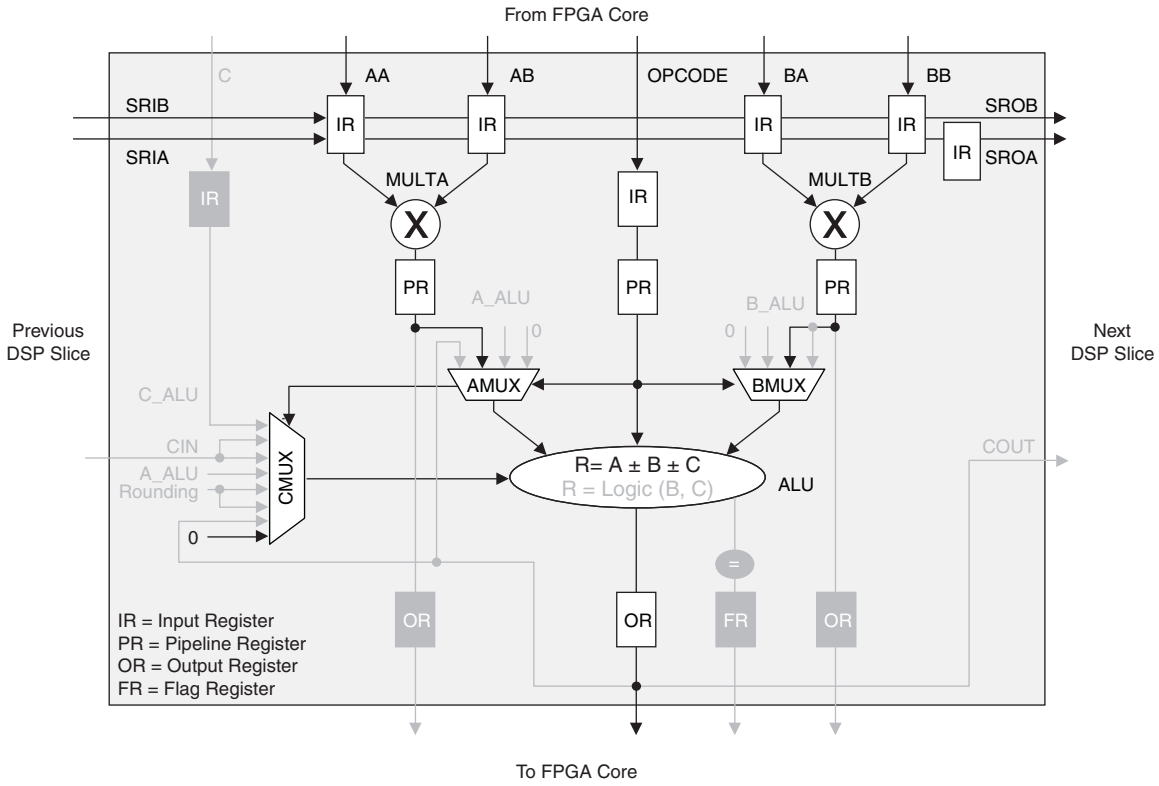
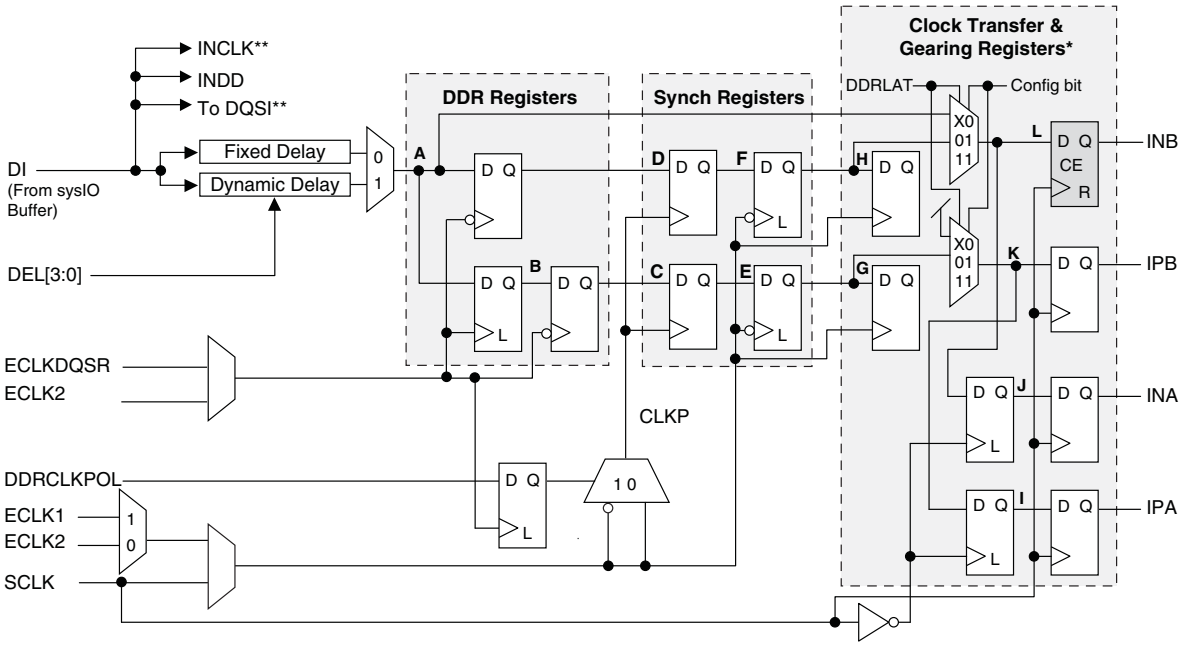


Figure 2-33. Input Register Block for Left, Right and Top Edges



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)

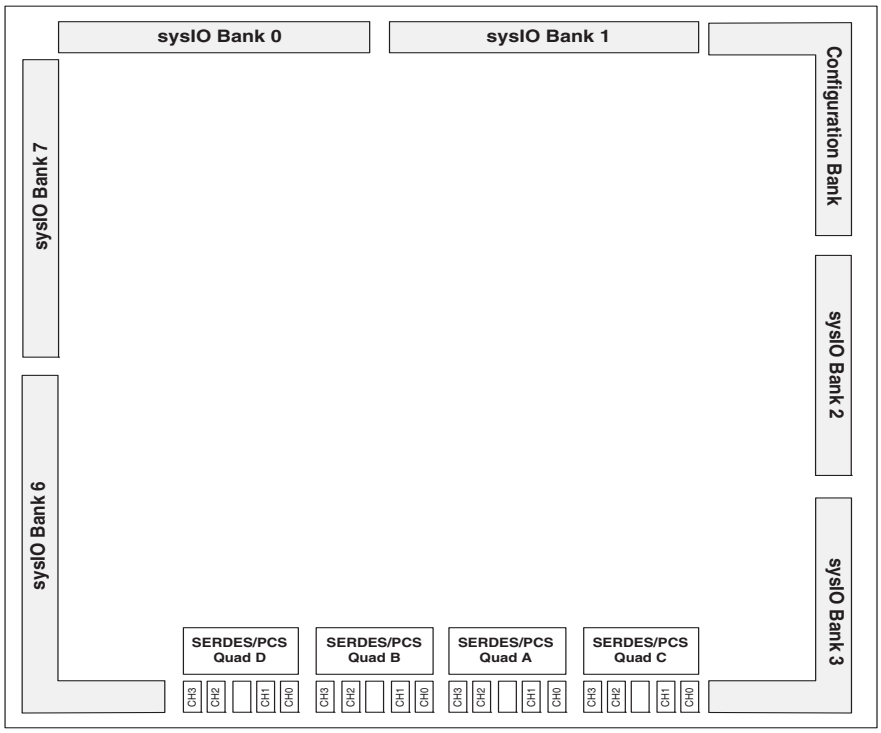


Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143[1], 177[1], 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3[2]	155.52	x1	N/A
SONET-STS-12[2]	622.08	x1	N/A
SONET-STS-48[2]	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.
2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical		Units
			–6L, –7L, –8L	–6, –7, –8	
I_{CC}	Core Power Supply Current	ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
		ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
		ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
I_{CCPLL}	PLL Power Supply Current (Per PLL)	ECP-17EA	0.0	0.0	mA
		ECP3-35EA	0.1	0.1	mA
		ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
		ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I_{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
I_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
		ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDRX2_RX.ECLK.Aligned) (No CLKDIV)									
Left and Right Sides Using DLLCLKPIN for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t_{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)[10]									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)[10]									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing									
t_{CH} (avg)[9]	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{CL} (avg)[9]	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{JIT} (per, lck)[9]	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	–90	90	–90	90	–90	90	ps
t_{JIT} (cc, lck)[9]	Output Cycle-to-Cycle Period Jitter During DLL Locking Period	All ECP3 Devices	—	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
9. Using settings generated by IPexpress.
10. These numbers are generated using best case PLL located in the center of the device.
11. Uses SSTL25 Class II Differential I/O Standard.
12. All numbers are generated with ispLEVER 8.1 software.
13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Figure 3-16. Jitter Transfer – 1.25 Gbps

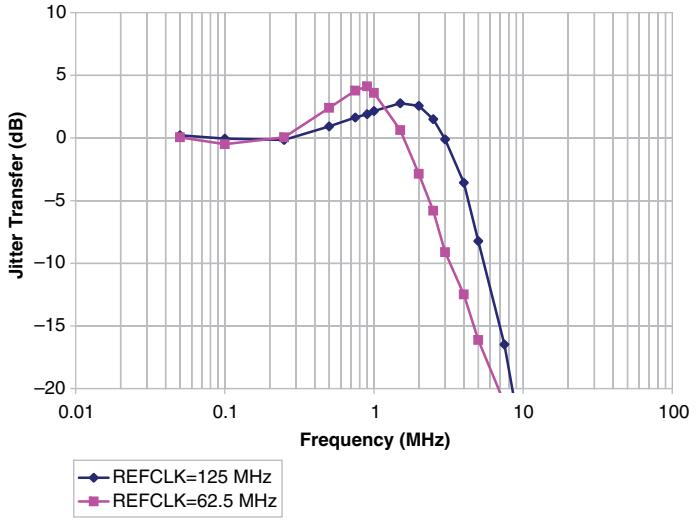


Figure 3-17. Jitter Transfer – 622 Mbps

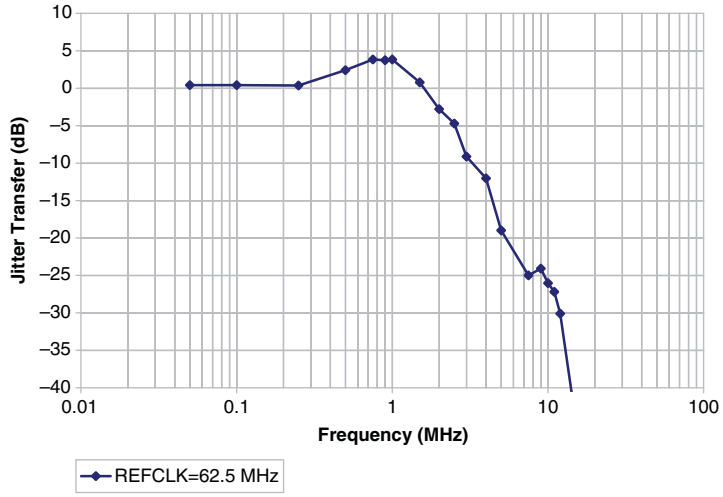
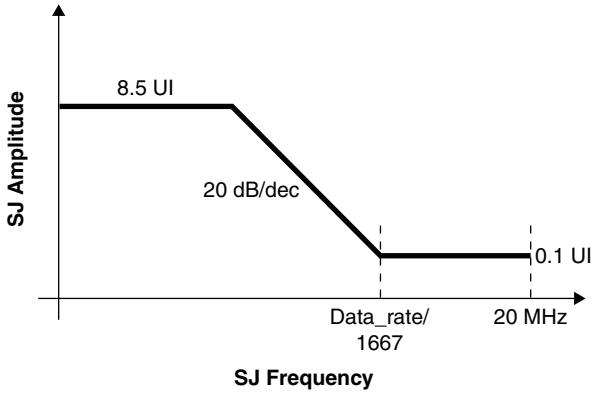


Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

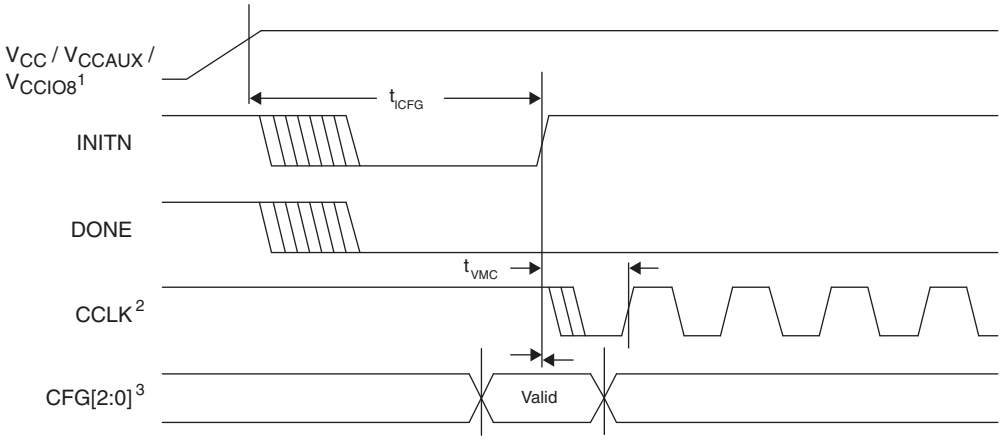
AC and DC Characteristics

Table 3-22. Transmit and Receive[1, 2]

Symbol	Description	Spec. Compliance		Units
		Min. Spec.	Max. Spec.	
Transmit				
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive				
R_T	Termination Resistance	40	60	Ohms
V_{ICM}	Input AC Common Mode Voltage (50-Ohm Setting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

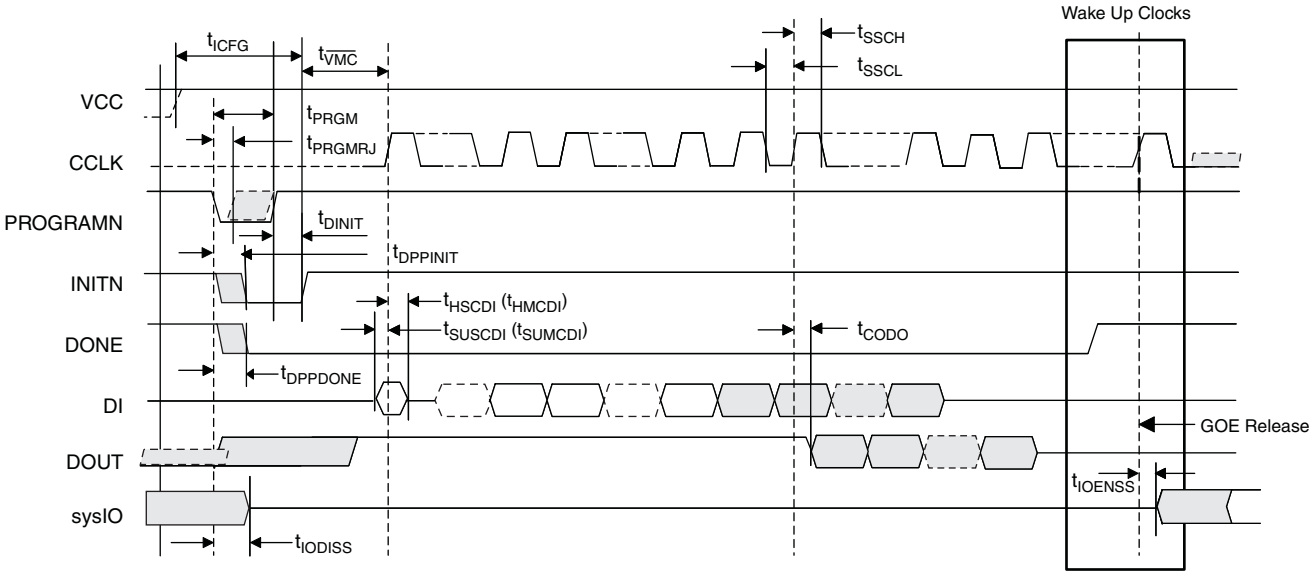
1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.
2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.

Figure 3-24. Power-On-Reset (POR) Timing



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

Figure 3-25. sysCONFIG Port Timing



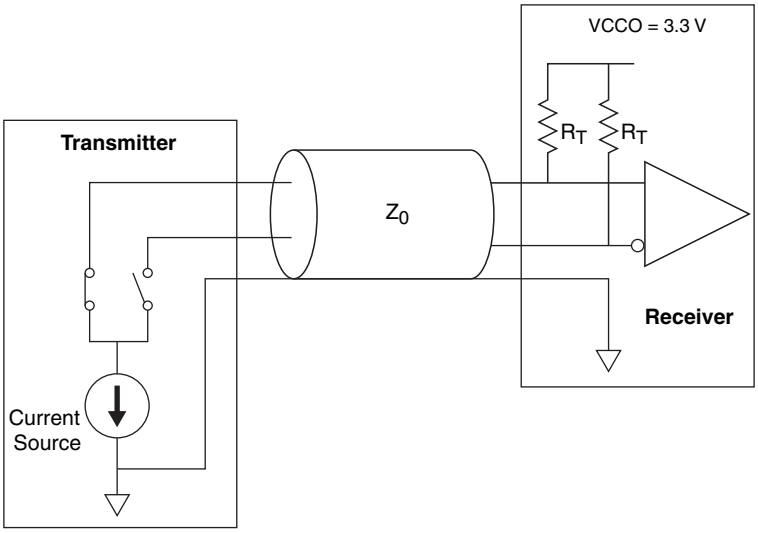
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/– 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Typ.	Max.	Units
Output driver supply (+/– 5%)	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 Ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43
	Bank 1	18	24	39
	Bank 2	8	12	13
	Bank 3	20	23	33
	Bank 6	22	25	33
	Bank 7	11	16	18
	Bank 8	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0
	Bank 1	0	0	0
	Bank 2	6	9	9
	Bank 3	9	12	16
	Bank 6	11	14	16
	Bank 7	9	12	13
	Bank 8	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49
	Bank 6	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12
DDR Groups Bonded per Bank[1]	Bank 0	3	5	7
	Bank 1	3	4	7
	Bank 2	2	3	3
	Bank 3	3	4	5
	Bank 6	4	4	5
	Bank 7	3	4	4
	Configuration Bank 8	0	0	0
SERDES Quads		1	2	3

1. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package[1]	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	–6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	–7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	–8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	–6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	–7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	–8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	–6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	–7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	–8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	–6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	–7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	–8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	–6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	–7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	–8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	–6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	–7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	–8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.