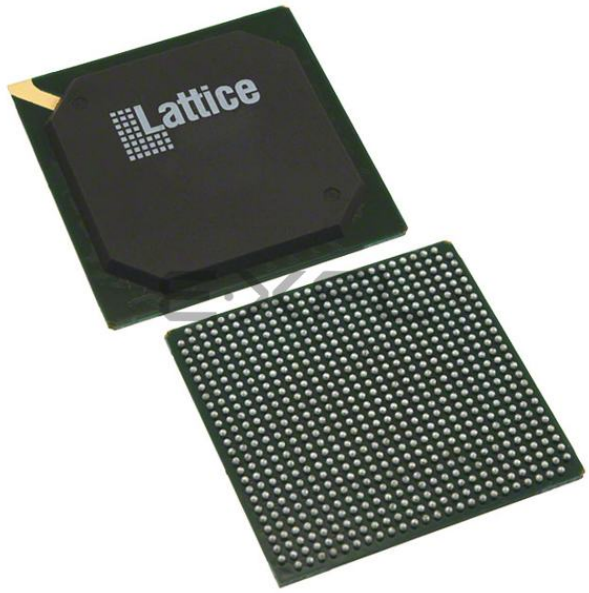
Lattice Semiconductor Corporation - LFE3-150EA-7LFN672I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-7lfn672i

LatticeECP3 Family Data Sheet Architecture

June 2013 Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

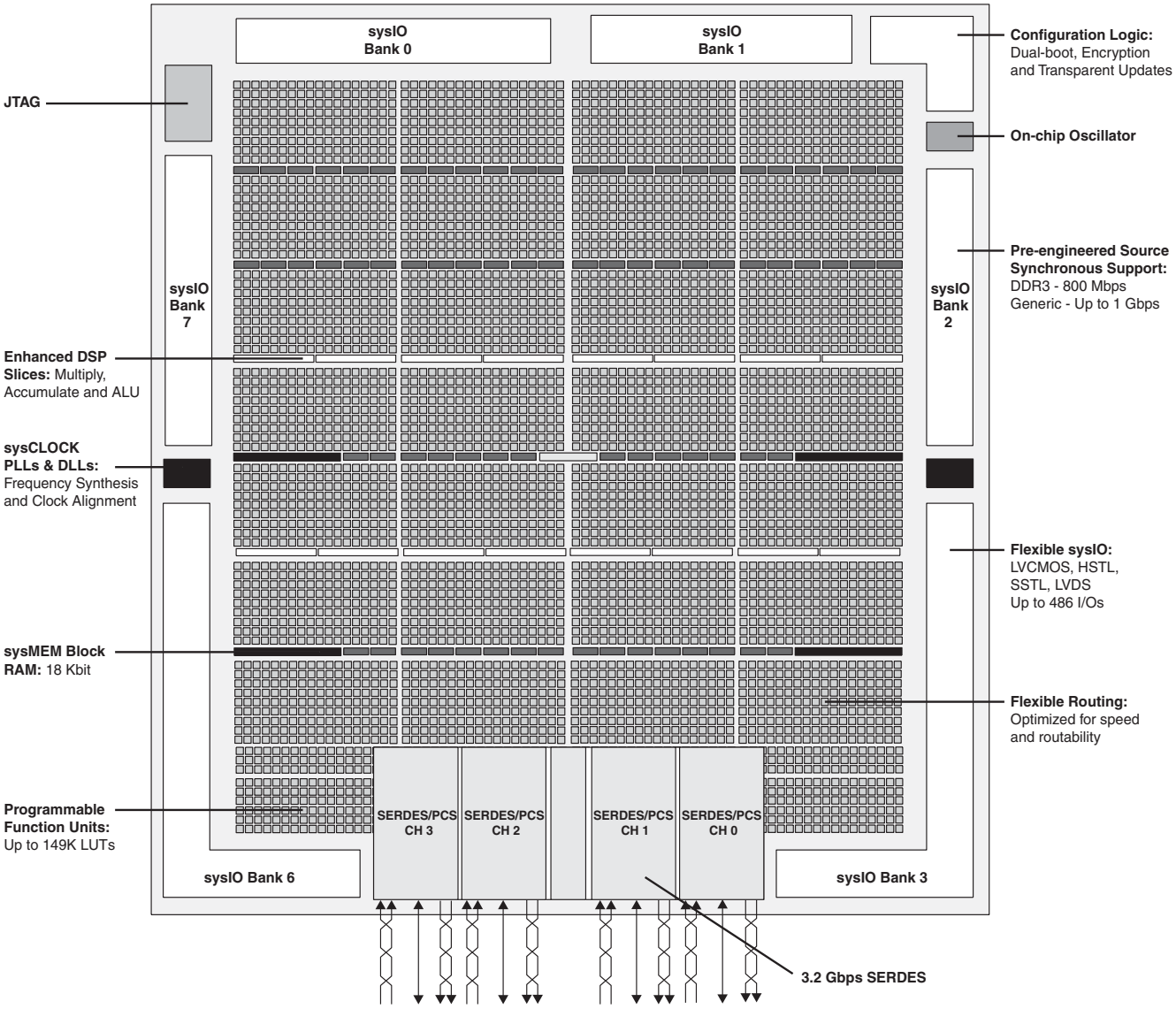
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



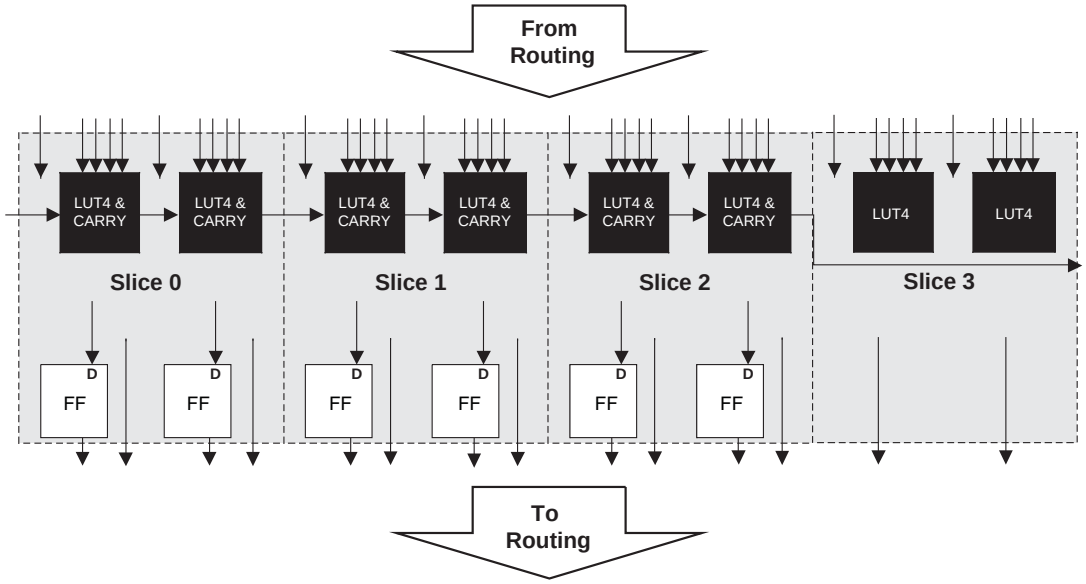
Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

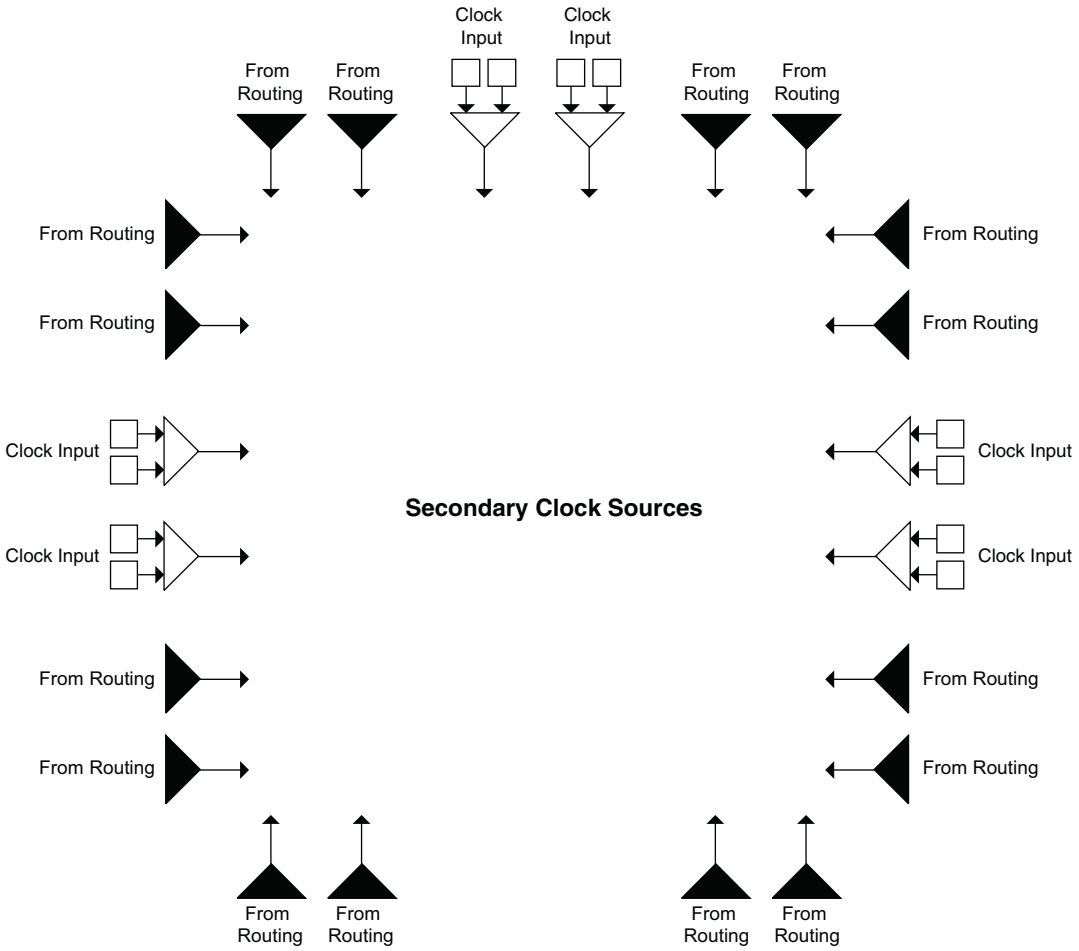
Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

Figure 2-14. Secondary Clock Sources



Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions

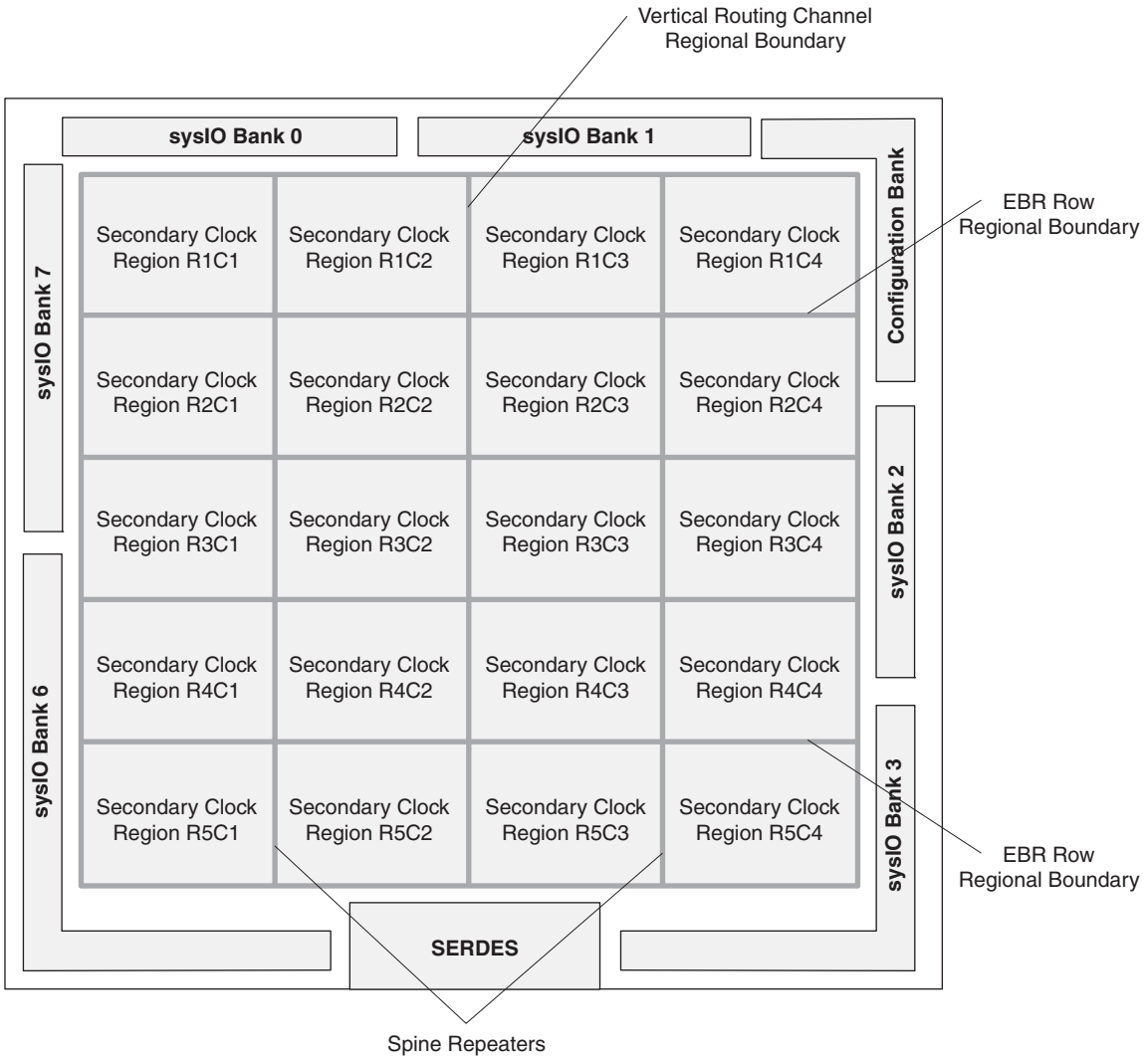
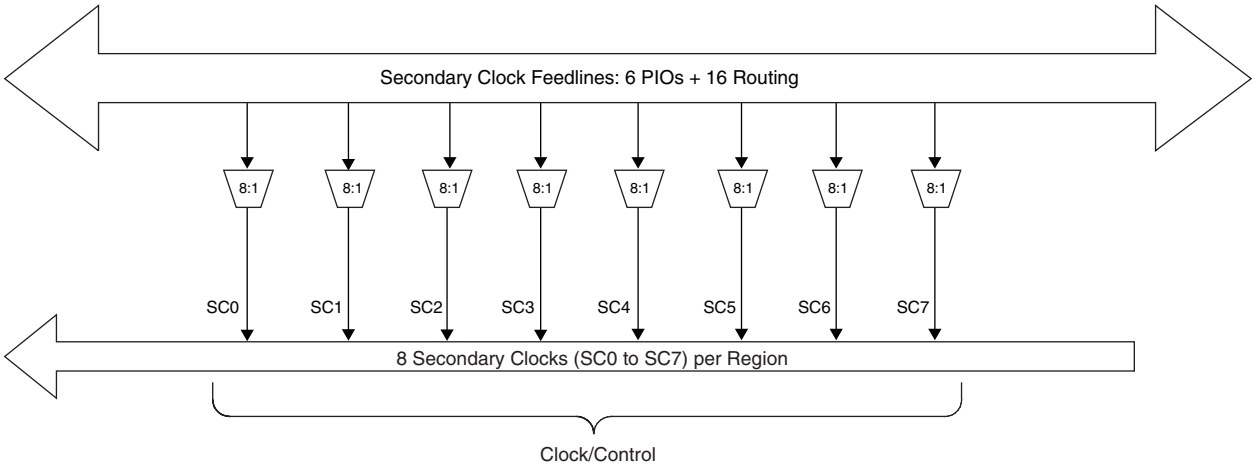


Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

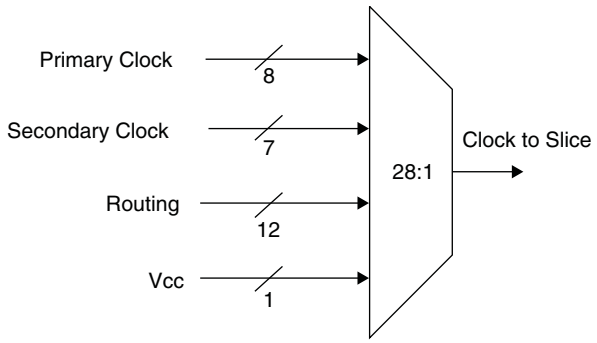
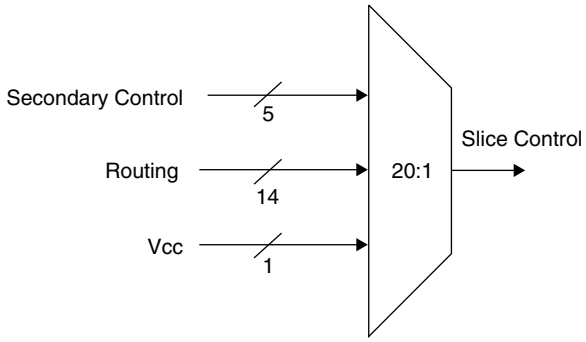


Figure 2-18. Slice0 through Slice2 Control Selection

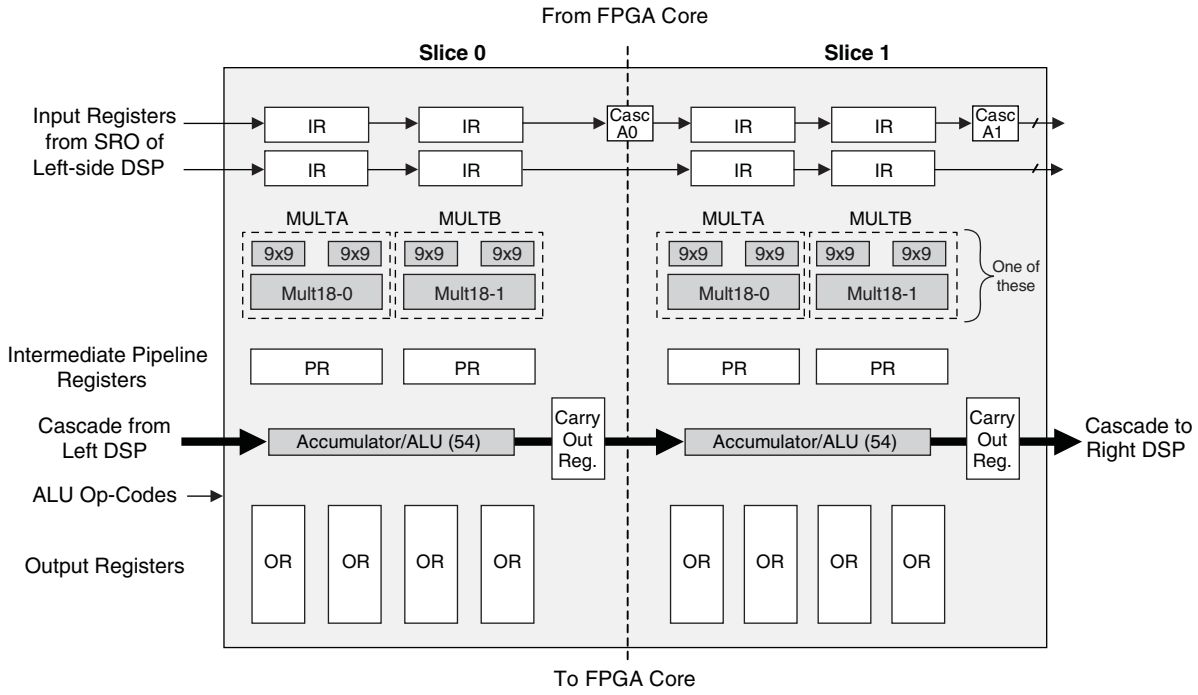


as, overflow, underflow and convergent rounding, etc.
— Flexible cascading across slices to get larger functions

- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-24, the LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2™ sysDSP block, such that, legacy applications can be targeted to the LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LatticeECP3 sysDSP slices, as shown in Figure 2-25.

Figure 2-24. Simplified sysDSP Slice Block Diagram



To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

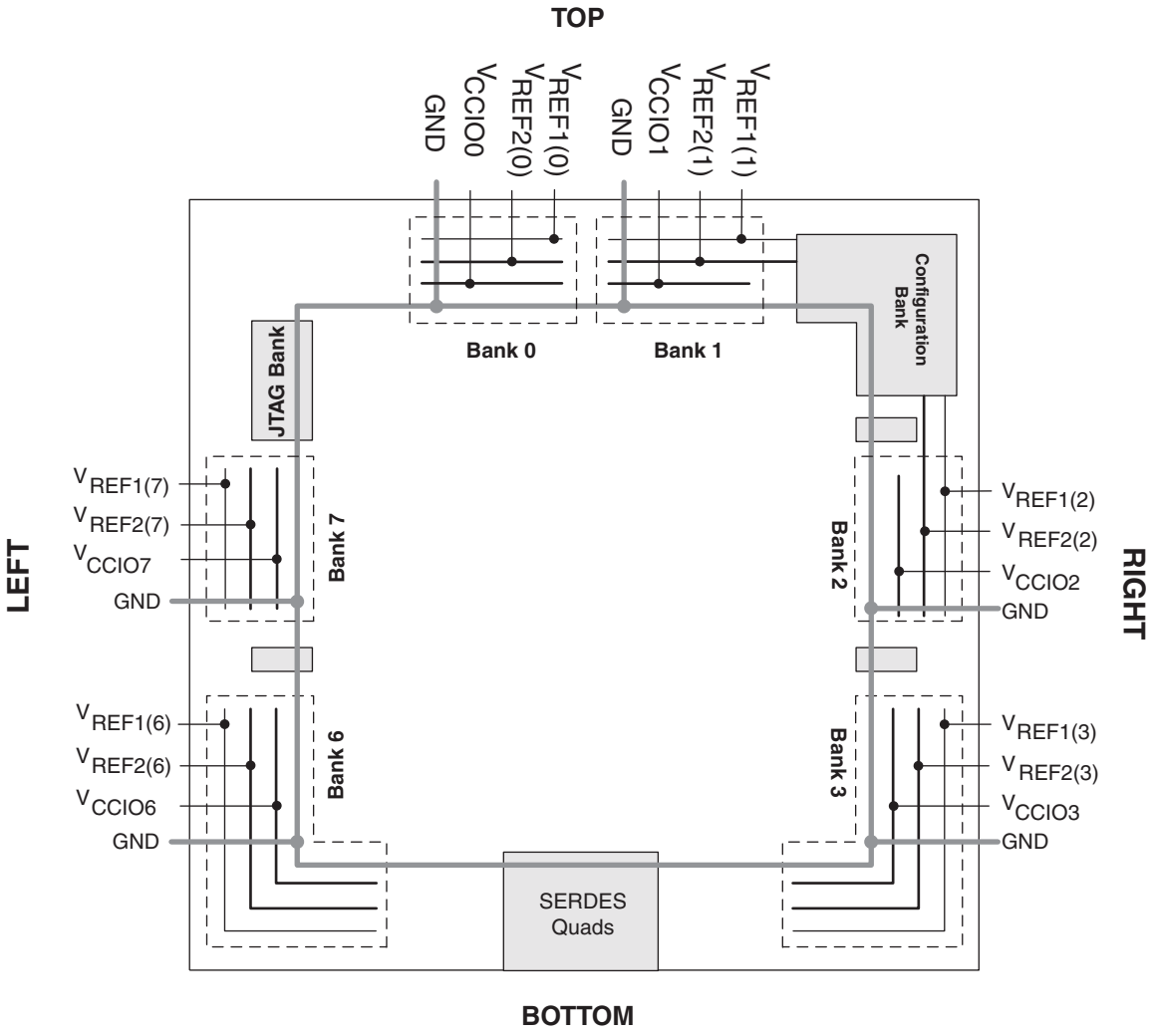
sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

   The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

LatticeECP3 Family Data Sheet DC and Switching Characteristics

April 2014 Data Sheet DS1021

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.32 V

Supply Voltage V_{CCAUX} . . . . . –0.5 V to 3.75 V

Supply Voltage V_{CCJ} . . . . . –0.5 V to 3.75 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.75 V

Input or I/O Tristate Voltage Applied[4]. . . –0.5 V to 3.75 V

Storage Temperature (Ambient) . . . . . .–65 V to 150 °C

Junction Temperature (T_J) . . . . . .+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.7	—	0.8	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.6	—	1.8	—	2.0	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.2	—	3.4	—	3.6	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.6	—	0.7	—	0.8	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-35EA	0.3	—	0.3	—	0.4	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.6	—	1.7	—	1.8	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.0	—	3.3	—	3.5	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.6	—	0.7	—	0.8	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-17EA	0.3	—	0.3	—	0.4	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.6	—	1.7	—	1.8	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
Generic DDR[12]									
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input									
t_{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	480	—	480	—	480	—	ps
t_{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	480	—	480	—	480	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input									
Data Left, Right, and Top Sides and Clock Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input									
Data Left, Right and Top Sides and Clock Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_RX.DQS.Centered) Using DQS Pin for Clock Input									
t_{SUGDDR}	Data Setup After CLK	All ECP3EA Devices	535	—	535	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	535	—	535	—	535	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (<10bits wide) Aligned at Pin (GDDRX1_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Data and Clock Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI

LatticeECP3 Maximum I/O Buffer Speed (Continued)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
PCI33	PCI, V_{CCIO} = 3.3 V	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z		–20%	50/75/HiZ	+20%	Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/– 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms

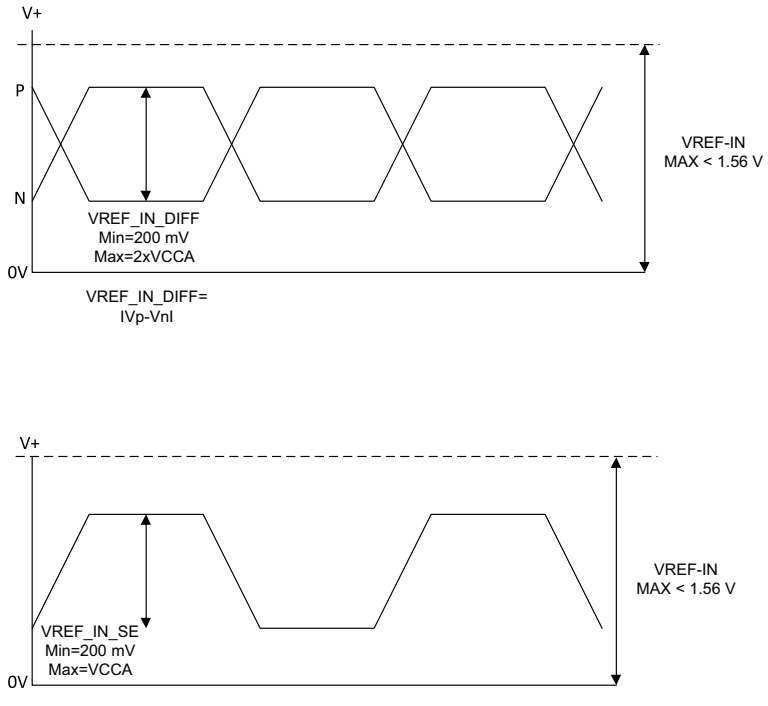
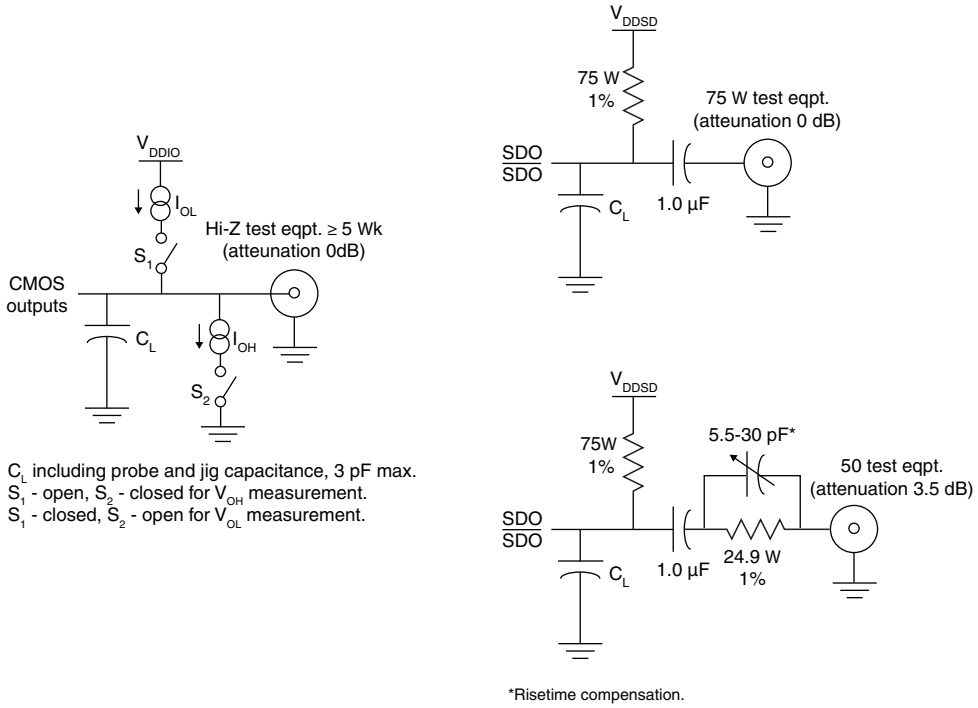


Figure 3-19. Test Loads

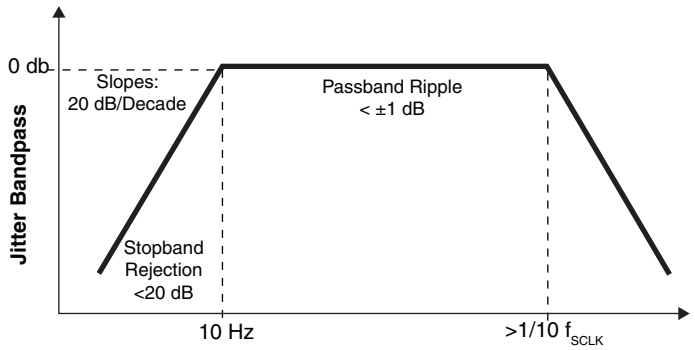
Test Loads



C_L including probe and jig capacitance, 3 pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

Timing Jitter Bandpass



LatticeECP3 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description		Min.	Max.	Units
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8}* (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Master mode	—	23	ms
		Slave mode	—	6	ms
t_{VMC}	Time from t_{ICFG} to the Valid Master MCLK		—	5	µs
t_{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low		—	37	ns
t_{DINIT}[1]	PROGRAMN High to INITN High Delay		—	1	ms
t_{MWC}	Additional Wake Master Clock Signals After DONE Pin is High		100	500	cycles
t_{CZ}	MCLK From Active To Low To High-Z		—	300	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low		—	100	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence		—	100	ns
All Configuration Modes					
t_{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t_{HCDI}	Data Hold Time to CCLK/MCLK		1	—	ns
t_{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Serial					
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns
t_{SSCL}	CCLK Minimum Low Pulse		5	—	ns
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave Parallel					
t_{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t_{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	—	ns
t_{HWD}	WRITEN Hold Time to CCLK/MCLK		1	—	ns
t_{DCB}	CCLK/MCLK to BUSY Delay Time		—	12	ns
t_{CORD}	CCLK to Out for Read Data		—	12	ns
t_{BSCH}	CCLK Minimum High Pulse		6	—	ns
t_{BSCL}	CCLK Minimum Low Pulse		6	—	ns
t_{BSCYC}	Byte Slave Cycle Time		30	—	ns
f_{CCLK}	CCLK/MCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave SPI					
t_{CFGX}	INITN High to MCLK Low		—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low		0.2	2	µs
t_{SOCDO}	MCLK Low to Output Valid		—	15	ns
t_{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		µs
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns

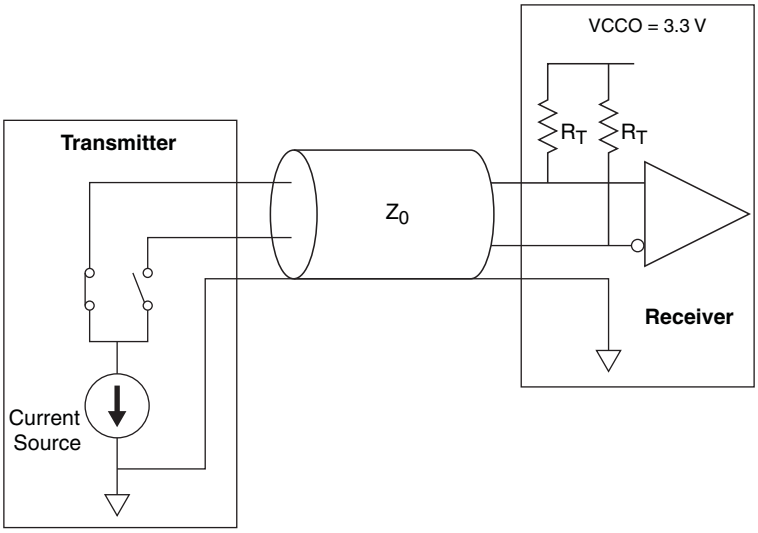
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/– 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250V.

Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t_{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX\text{-}DIFF\text{-}S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD}.
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	—	Initial release.