E. Lattice Semiconductor Corporation - LFE3-150EA-8FN1156I Datasheet



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18625
Number of Logic Elements/Cells	149000
Total RAM Bits	7014400
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-150ea-8fn1156i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- 1. **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- 3. **Read-Before-Write (EA devices only)** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP[™] Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

	PIO A	↓	PADA "T"
	PIO B		PADB "C"
	PIO A		PADA "T"
	PIO B	+	PADB "C"
	PIO A		PADA "T"
	PIO B	L+	PADB "C"
_ DQS	PIO A	SysIO Buffer Delay ◀	PADA "T" LVDS Pair
	PIO B		PADB "C"
	PIO A		PADA "T" LVDS Pair
	→ PIO A → PIO B		PADA "T" LVDS Pair PADB "C"
	→ PIO A → PIO B → PIO A		PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
			PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



2. Left and Right (Banks 2, 3, 6 and 7) sysl/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysl/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysl/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysl/O Standards

The LatticeECP3 sysl/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysl/O buffer to support a variety of standards please see TN1177, LatticeECP3 syslO Usage Guide.



SERDES Power Supply Requirements^{1, 2, 3}

Symbol	Description	Тур.	Max.	Units
Standby (Power Do	own)	•		1
I _{CCA-SB}	V _{CCA} current (per channel)	3	5	mA
I _{CCIB-SB}	Input buffer current (per channel)		—	mA
I _{CCOB-SB}	Output buffer current (per channel)	—	_	mA
Operating (Data Ra	ite = 3.2 Gbps)			•
I _{CCA-OP}	V _{CCA} current (per channel)	68	77	mA
I _{CCIB-OP}	Input buffer current (per channel)	5	7	mA
I _{CCOB-OP}	Output buffer current (per channel)	19	25	mA
Operating (Data Ra	ite = 2.5 Gbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	66	76	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Ra	ite = 1.25 Gbps)			·
I _{CCA-OP}	V _{CCA} current (per channel)	62	72	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Ra	ite = 250 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA
Operating (Data Ra	ite = 150 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.

2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

3. Pre-emphasis adds 20 mA to ICCA-OP data.



LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.





Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



Units V

Ω

Ω

Ω

Ω

٧

٧

V

V

mΑ

BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS25 DC Conditions¹

V_{CCIO}

ZOUT

R_S

R_{TL}

 R_{TR} V_{OH}

VOL

VOD

V_{CM}

	-	-		
		Тур	ical	
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	
CCIO	Output Driver Supply (+/– 5%)	2.50	2.50	

10.00

90.00

45.00

45.00

1.38

1.12

0.25

1.25

11.24

10.00

90.00

90.00

90.00

1.48

1.02

0.46

1.25

10.20

Over Recommended Operating Conditions

 I_{DC} 1. For input buffer, see LVDS table.

Driver Impedance

Output High Voltage

Output Low Voltage

DC Output Current

Output Differential Voltage

Output Common Mode Voltage

Driver Series Resistor (+/- 1%)

Driver Parallel Resistor (+/- 1%)

Receiver Termination (+/- 1%)



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

	-8 -7		-7	-6					
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 In	puts with Clock and Data (>10bits	s wide) are Aligned at I	Pin (GDD	RX2_RX	.ECLK.A	ligned)	1		
(No CLKDIV)									
Left and Right Side	es Using DLLCLKPIN for Clock Ir			0.005	1	0.005	1	0.005	
^t DVACLKGDDR	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225	
	Data Hold After CLK	ECP3-150EA	0.775	-	0.775		0.775		
^T MAX_GDDR	DDRX2 Clock Frequency	ECP3-150EA	_	460	_	385	_	345	MHZ
^t DVACLKGDDR	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI
^t DVECLKGDDR	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775		0.775	—	UI
fMAX_GDDR	DDRX2 Clock Frequency	ECP3-70EA/95EA		460		385		311	MHZ
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	_	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	—	0.790	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	460	_	385	_	311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	_	0.210	_	0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA		460		385		311	MHz
Top Side Using PC	LK Pin for Clock Input								
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	235	—	170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	235		170	—	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	_	0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA		235		170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA		0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790		0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	235		170		130	MHz
Generic DDRX2 In Input	puts with Clock and Data (<10 Bit	ts Wide) Centered at P	in (GDDF	RX2_RX.I	DQS.Cen	tered) U	sing DQ	S Pin for	Clock
Left and Right Side	es								
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	_	330		352		ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	_	ps
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	_	375	MHz
Generic DDRX2 In	puts with Clock and Data (<10 Bit	ts Wide) Aligned at Pin	(GDDR)	(2_RX.D0	QS.Align	ed) Using	g DQS Pi	n for Clo	ck Input
Left and Right Side	es								
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	_	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	_	0.775	_	UI
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz
Generic DDRX1 O	utput with Clock and Data (>10 B	its Wide) Centered at P	in (GDD	RX1_TX.	SCLK.Ce	ntered)10)		
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670		670		ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665		664	—	ps
	Data Valid After CLK	ECP3-70EA/95EA	666		665		664		ps
BIAGDDIT	1	1		I		l			· ·

Over Recommended Commercial Operating Conditions







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5 V	-0.07	-0.04	-0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	-0.22	-0.19	-0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.3V	-0.06	-0.06	-0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.3V	-0.01	-0.02	-0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.3V	-0.07	-0.07	-0.08	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.3V	-0.12	-0.13	-0.14	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	-0.06	-0.06	-0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	-0.01	-0.02	-0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	-0.07	-0.07	-0.08	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	-0.05	-0.06	-0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns

Over Recommended Commercial Operating Conditions



SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmi	t Data Latency ¹				•	•	
	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
T1	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	_	_	2	1	word clk
Т3	SERDES Bridge transmit	—		_	2	1	word clk
тл	Serializer: 8-bit mode		_		15 + Δ1	—	UI + ps
14	Serializer: 10-bit mode	—	_		18 + Δ1	—	UI + ps
TE	Pre-emphasis ON		_		1 + ∆2	—	UI + ps
15	Pre-emphasis OFF	—	—	—	0 + ∆3	—	UI + ps
Receive	Data Latency ²				•		
D1	Equalization ON			_	Δ1	_	UI + ps
	Equalization OFF		_		Δ2	—	UI + ps
D 2	Deserializer: 8-bit mode	—	_	_	10 + ∆3	—	UI + ps
Π <u>Ζ</u>	Deserializer: 10-bit mode	—	—	_	12 + ∆3	—	UI + ps
R3	SERDES Bridge receive	—	—	_	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	_	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
R7	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. $\Delta 1 = -245 \text{ ps}, \Delta 2 = +88 \text{ ps}, \Delta 3 = +112 \text{ ps}.$

2. $\Delta 1 = +118$ ps, $\Delta 2 = +132$ ps, $\Delta 3 = +700$ ps.







Figure 3-16. Jitter Transfer – 1.25 Gbps



Figure 3-17. Jitter Transfer – 622 Mbps





Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).



Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF}	Differential rise/fall time	20%-80%	_	80		ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{3, 4, 5}	Output data deterministic jitter		_	—	0.10	UI
J _{TX_TJ} ^{2, 3, 4, 5}	Total output data jitter			_	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 1.25 Gbps.

Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10			dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6			dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{1, 2, 3, 4, 5}	Deterministic jitter tolerance (peak-to-peak)		_	_	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4, 5}	Random jitter tolerance (peak-to-peak)		-		0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4, 5}	Sinusoidal jitter tolerance (peak-to-peak)		-		0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4, 5}	Total jitter tolerance (peak-to-peak)		_	_	0.71	UI
T _{RX_EYE}	Receiver eye opening		0.29	_	_	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 1.25 Gbps.



Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Te	est Fixture Required	Components,	Non-Terminated Interfaces
----------------	----------------------	-------------	---------------------------

Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
				LVCMOS 3.3 = 1.5V	V _T V _{CCIO}
				LVCMOS 2.5 = $V_{CCIO}/2$	
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 1.8 = V _{CCIO} /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> H)	8	1MΩ	0 pF	V _{CCIO} /2	
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	8	100	0 pF	V _{OH} - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	x	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Pin Information Summary (Cont.)

Pin Information Sun	ECP3-17EA			ECP3-35EA			
Pin Type	256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	
	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
Emulated Differential I/O per	Bank 3	4	2	13	5	20	19
Dank	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
Highspeed Differential I/O per	Bank 3	5	4	9	4	9	12
Dank	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
Differential I/O per Bank	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
DDR Groups Bonded per	Bank 3	1	0	3	1	3	4
Bank [∠]	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

These pins must remain floating on the board.
 Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.



Package Pinout Information

Package pinout information can be found under "Data Sheets" on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software



LatticeECP3 Family Data Sheet Supplemental Information

February 2014

Data Sheet DS1021

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at <u>www.latticesemi.com</u>.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist
- TN1215, LatticeECP2MS and LatticeECP2S Devices
- TN1216, LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3
- TN1222, LatticeECP3 Slave SPI Port User's Guide

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

© 2014 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Date	Version	Section	Change Summary
			Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification
December 2010	01.7EA	Multiple	Data sheet made final. Removed "preliminary" headings.
			Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices.
			Updated for Lattice Diamond design software.
		Introduction	Corrected number of user I/Os
		Architecture	Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices.
			Updated description of General Purpose PLL
			Added additional information in the Flexible Quad SERDES Architecture section.
			Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal).
			Updated Figure 2-16, Per Region Secondary Clock Selection.
			Updated description for On-Chip Programmable Termination.
			Added information about number of rows of DSP slices.
			Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes.
			Updated information for sysIO buffer pairs.
			Corrected minimum number of General Purpose PLLs (was 4, now 2).
		DC and Switching Characteristics	Regenerated sysCONFIG Port Timing figure.
			Added ${\rm t}_{\rm W}$ (clock pulse width) in External Switching Characteristics table.
			Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table.
			Added Jitter Transfer figures in SERDES External Reference Clock section.
			Corrected capacitance information in the DC Electrical Characteristics table.
			Corrected data in the Register-to-Register Performance table.
			Corrected GDDR Parameter name HOGDDR.
			Corrected RSDS25 -7 data in Family Timing Adders table.
			Added footnotes 10-12 to DDR data information in the External Switch- ing Characteristics table.
			Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDRX2 Parameters).
			Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differ- ential Signaling)) and 3-6 (Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)).
			Updated Supply Current table.
			Added GDDR interface information to the External Switching and Characteristics table.
			Added footnote to sysIO Recommended Operating Conditions table.
			Added footnote to LVDS25 table.
			Corrected DDR section footnotes and references.
			Corrected Hot Socketing support from "top and bottom banks" to "top and bottom I/O pins".
		Pinout Information	Updated description for VTTx.