# Lattice Semiconductor Corporation - LFE3-17EA-6FN484I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

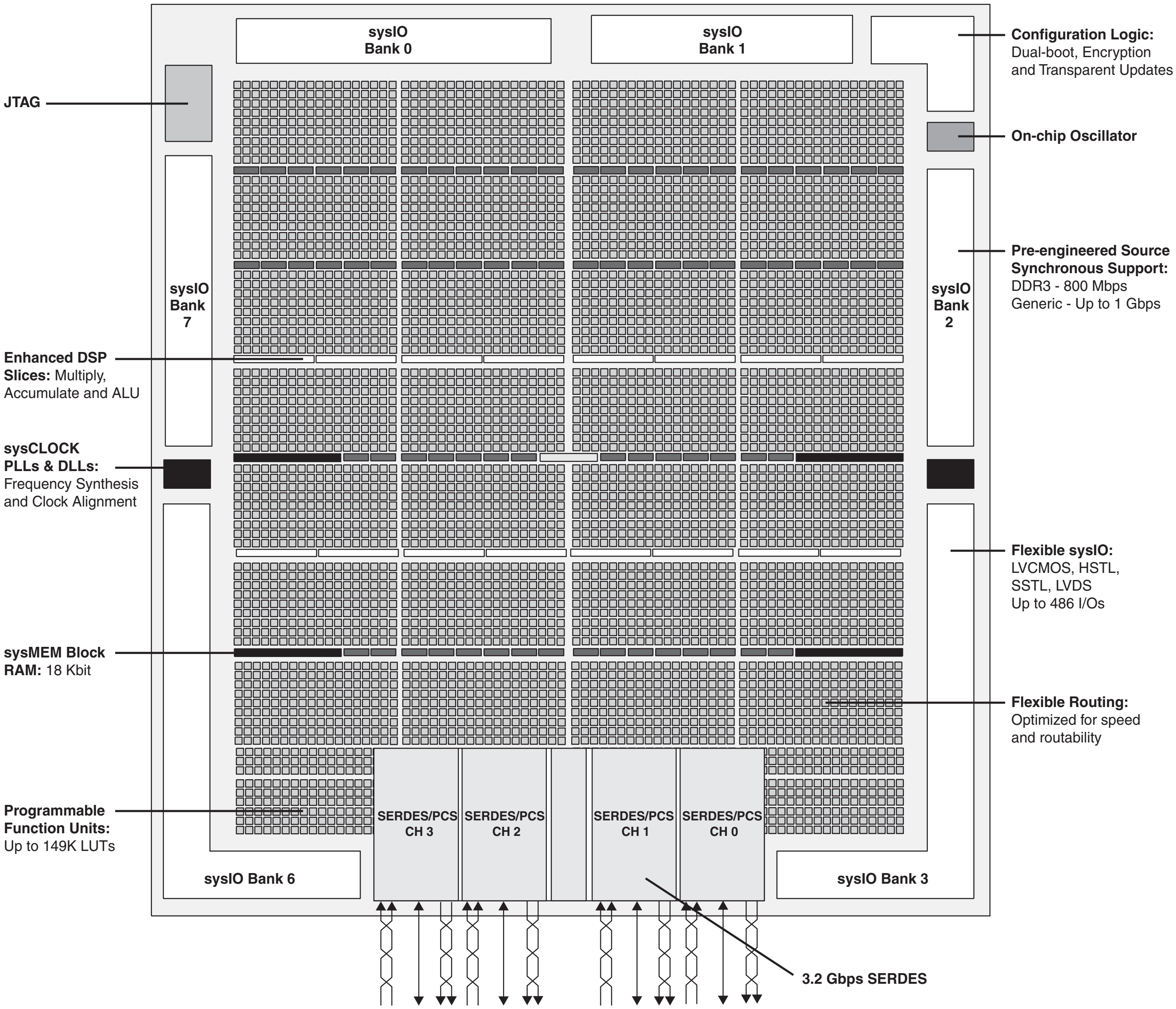
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2125 |
| Number of Logic Elements/Cells | 17000 |
| Total RAM Bits | 716800 |
| Number of I/O | 222 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-6fn484i |

*Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)*



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

## PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

***Table 2-3. Number of Slices Required to Implement Distributed RAM***

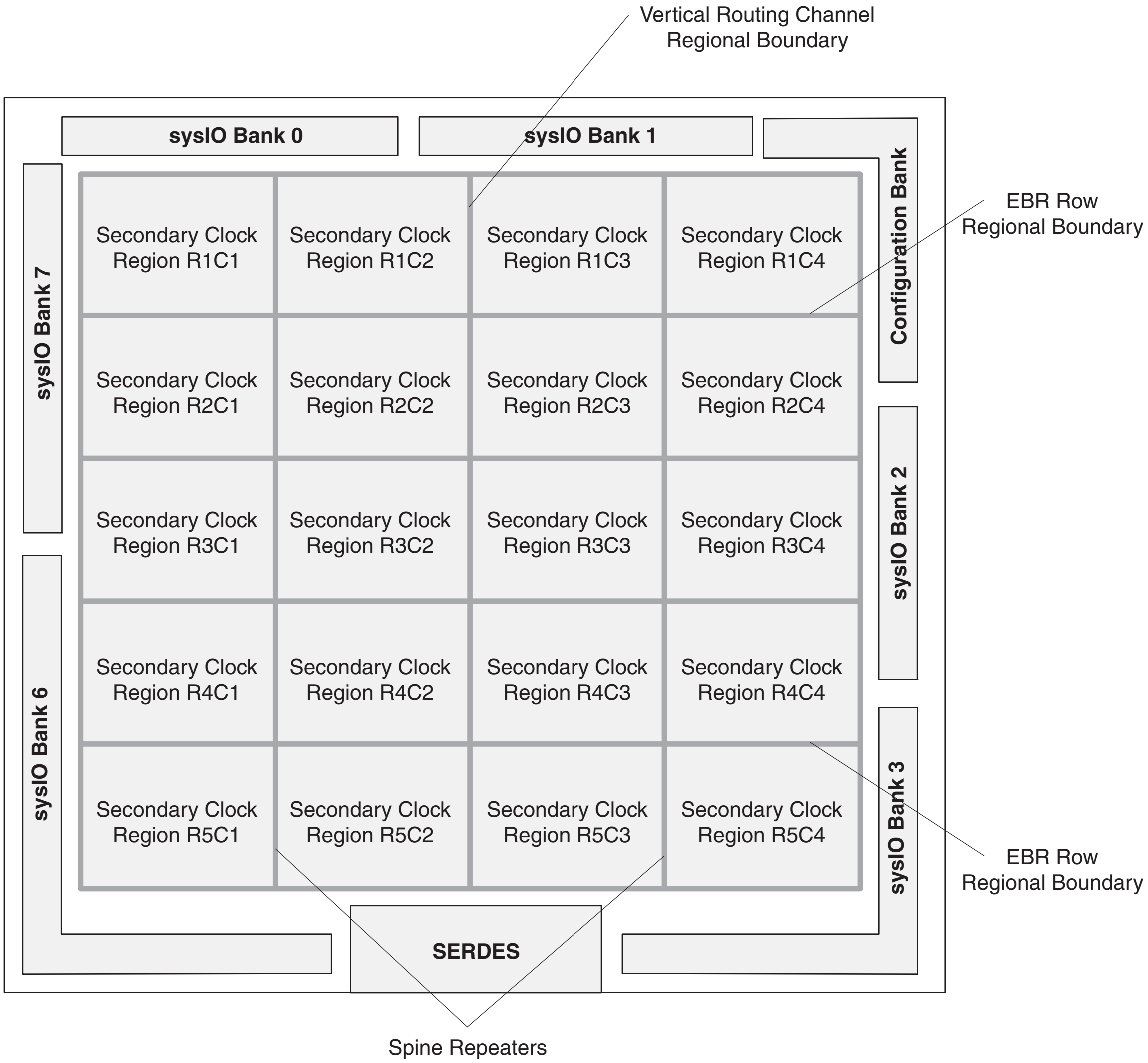
| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

*Table 2-6. Secondary Clock Regions*

| Device | Number of Secondary Clock Regions |
|---|---|
| ECP3-17 | 16 |
| ECP3-35 | 16 |
| ECP3-70 | 20 |
| ECP3-95 | 20 |
| ECP3-150 | 36 |

*Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions*



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

## MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

*Figure 2-26. MULT sysDSP Element*

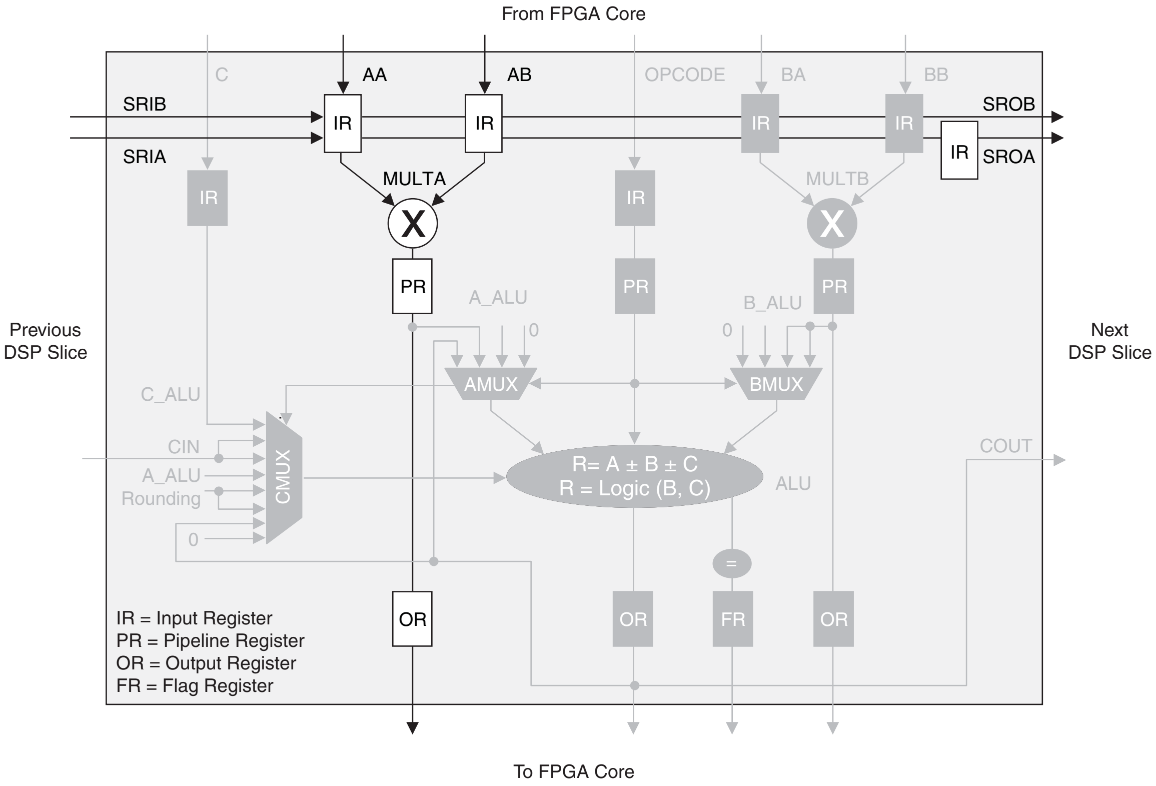
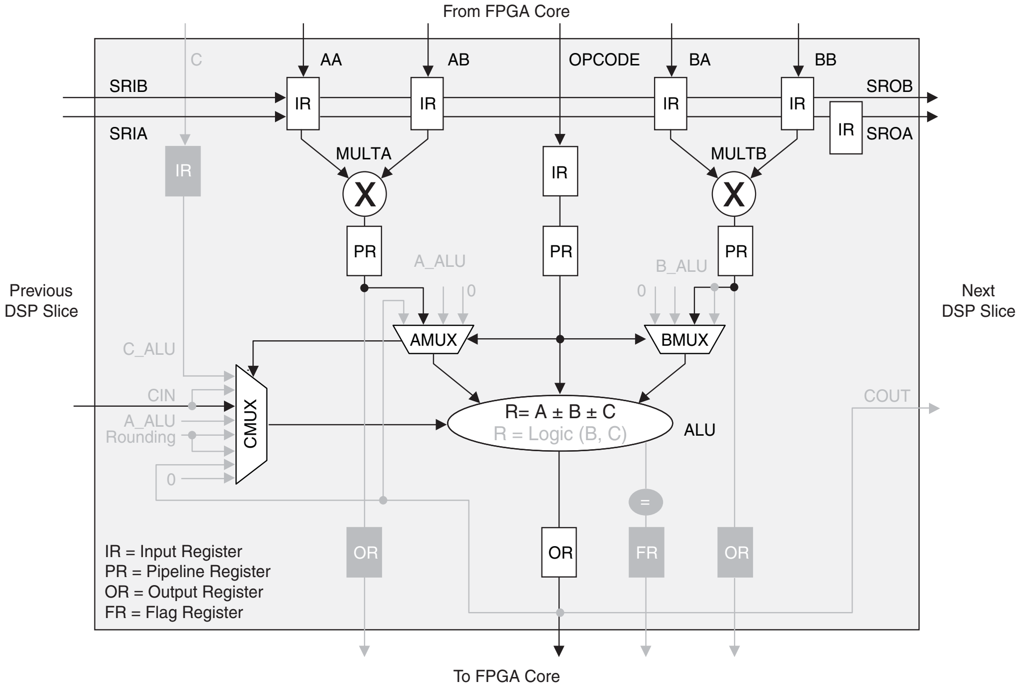


*Figure 2-31. MULTADDSUBSUM Slice 1*



# Advanced sysDSP Slice Features

## Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

## Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

## Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

## ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

## Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

***Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family***

| Device | DSP Slices | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---|---|---|---|---|
| ECP3-17 | 12 | 48 | 24 | 6 |
| ECP3-35 | 32 | 128 | 64 | 16 |
| ECP3-70 | 64 | 256 | 128 | 32 |
| ECP3-95 | 64 | 256 | 128 | 32 |
| ECP3-150 | 160 | 640 | 320 | 80 |

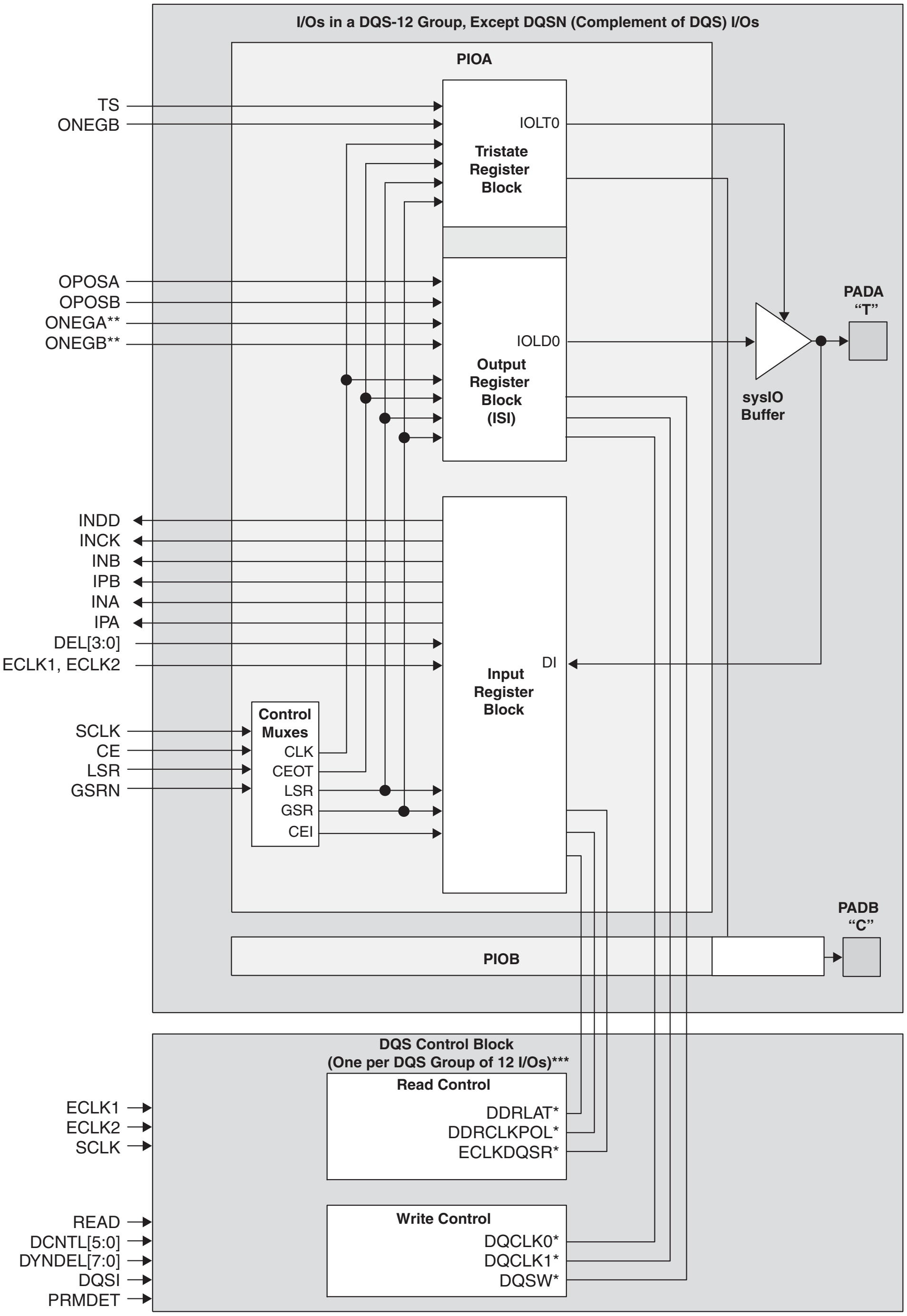
***Table 2-10. Embedded SRAM in the LatticeECP3 Family***

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) |
|---|---|---|
| ECP3-17 | 38 | 700 |
| ECP3-35 | 72 | 1327 |
| ECP3-70 | 240 | 4420 |
| ECP3-95 | 240 | 4420 |
| ECP3-150 | 372 | 6850 |

## Programmable I/O Cells (PIC)

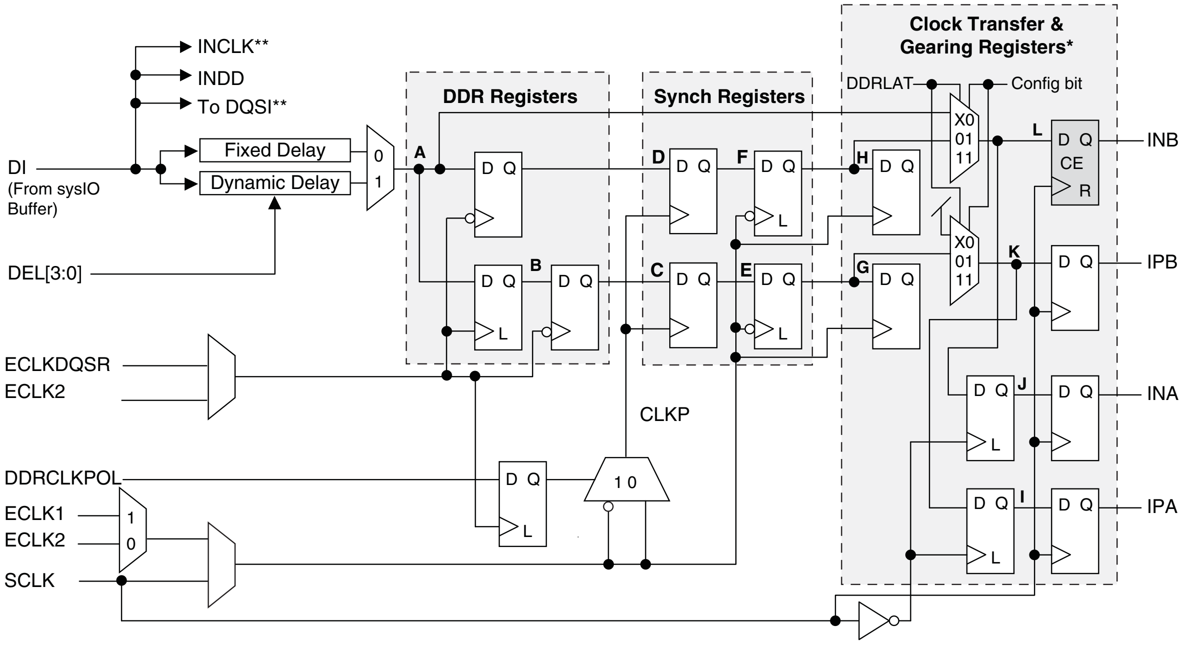
Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

***Figure 2-32. PIC Diagram***



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

*Figure 2-33. Input Register Block for Left, Right and Top Edges*



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

## Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

## External Resistor

LatticeECP3 devices require a single external, 10 kOhm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

## On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/– 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

# DC Electrical Characteristics

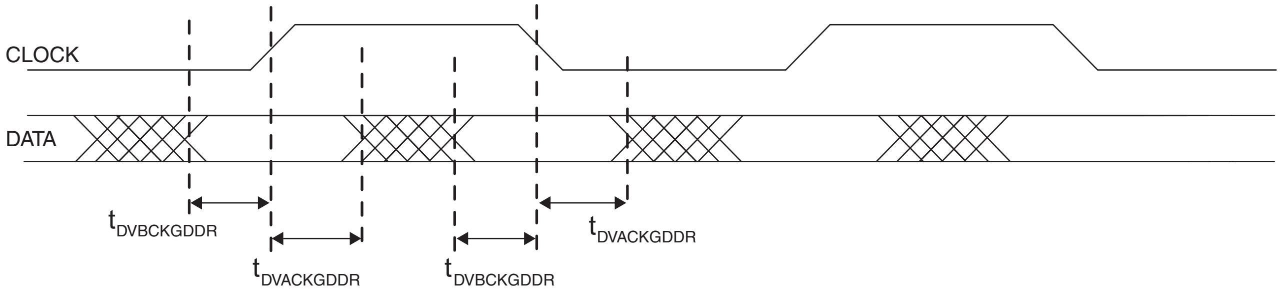
### Over Recommended Operating Conditions

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input or I/O Low Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2\text{ V})$ | — | — | 10 | µA |
| $I_{IH}$[1, 3] | Input or I/O High Leakage | $(V_{CCIO} - 0.2\text{ V}) < V_{IN} \le 3.6\text{ V}$ | — | — | 150 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | –30 | — | –210 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{CCIO}$ | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCIO}$ | –30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 210 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | –210 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V,<br>$V_{CC}$ = 1.2 V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 8 | pf |
| C2 | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V,<br>$V_{CC}$ = 1.2 V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 7 | pf |

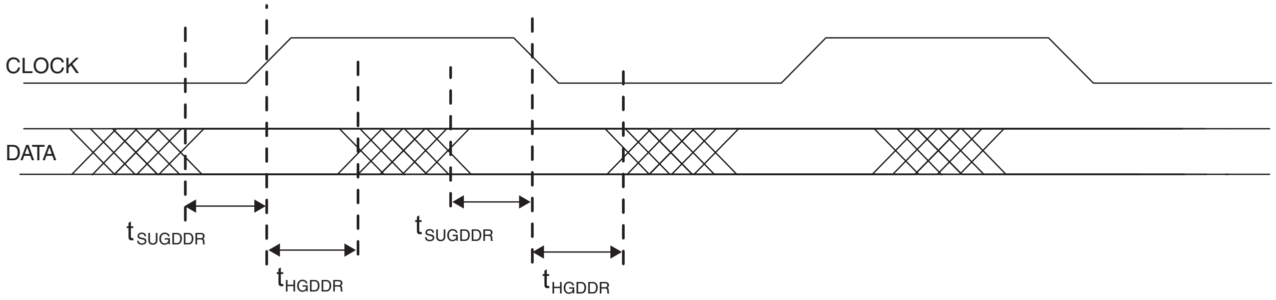
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as $V_{REF}$, maximum leakage= 25 µA.

*Figure 3-8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)*

**Transmit Parameters**



**Receive Parameters**

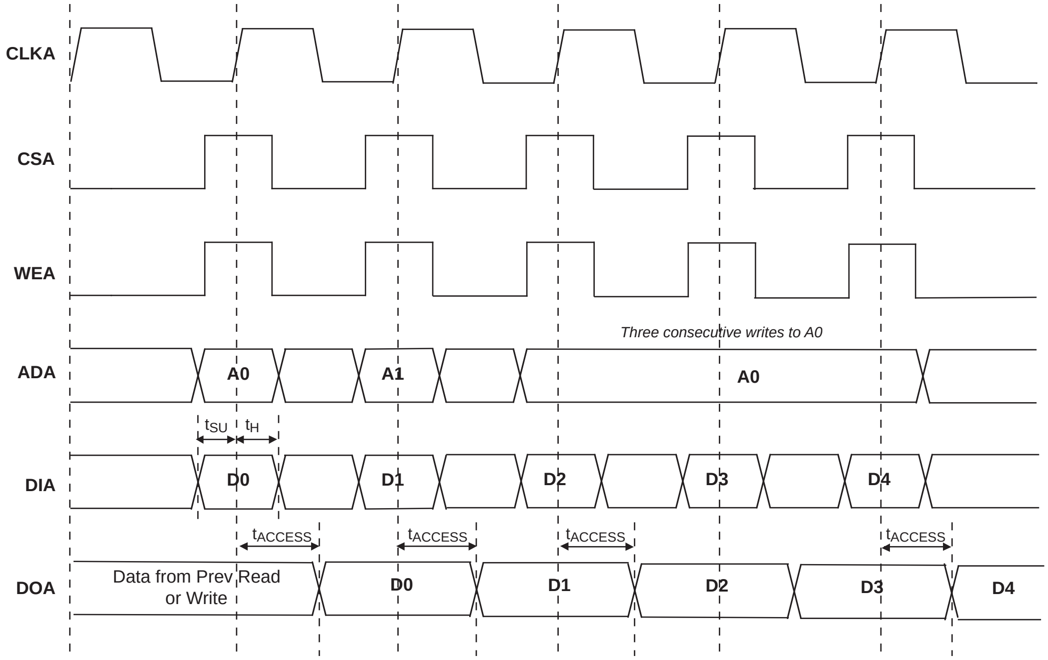


## LatticeECP3 Internal Switching Characteristics[1, 2, 5]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | –8 | | –7 | | –6 | | Units. |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.147 | — | 0.163 | — | 0.179 | ns |
| $t_{LUT6\_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.281 | — | 0.335 | — | 0.379 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to output of PFU (Asynchronous) | — | 0.593 | — | 0.674 | — | 0.756 | ns |
| $t_{LSRREC\_PFU}$ | Asynchronous Set/Reset recovery time for PFU Logic | | 0.298 | | 0.345 | | 0.391 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.134 | — | 0.144 | — | 0.153 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | –0.097 | — | –0.103 | — | –0.109 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D input setup time | 0.061 | — | 0.068 | — | 0.075 | — | ns |
| $t_{HD\_PFU}$ | Clock to D input hold time | 0.019 | — | 0.013 | — | 0.015 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q delay, (D-type Register Configuration) | — | 0.243 | — | 0.273 | — | 0.303 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output (F Port) | — | 0.710 | — | 0.803 | — | 0.897 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | –0.137 | — | –0.155 | — | –0.174 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.188 | — | 0.217 | — | 0.246 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | –0.227 | — | –0.257 | — | –0.286 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.240 | — | 0.275 | — | 0.310 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | –0.055 | — | –0.055 | — | –0.063 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.059 | — | 0.059 | — | 0.071 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay (LVCMOS25) | — | 0.423 | — | 0.466 | — | 0.508 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay (LVCMOS25) | — | 1.241 | — | 1.301 | — | 1.361 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI\_PIO}$ | Input Register Setup Time (Data Before Clock) | 0.956 | — | 1.124 | — | 1.293 | — | ns |
| $t_{HI\_PIO}$ | Input Register Hold Time (Data after Clock) | 0.225 | — | 0.184 | — | 0.240 | — | ns |
| $t_{COO\_PIO}$ | Output Register Clock to Output Delay[4] | - | 1.09 | - | 1.16 | - | 1.23 | ns |
| $t_{SUCE\_PIO}$ | Input Register Clock Enable Setup Time | 0.220 | — | 0.185 | — | 0.150 | — | ns |
| $t_{HCE\_PIO}$ | Input Register Clock Enable Hold Time | –0.085 | — | –0.072 | — | –0.058 | — | ns |
| $t_{SULSR\_PIO}$ | Set/Reset Setup Time | 0.117 | — | 0.103 | — | 0.088 | — | ns |
| $t_{HLSR\_PIO}$ | Set/Reset Hold Time | –0.107 | — | –0.094 | — | –0.081 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock (Read) to output from Address or Data | — | 2.78 | — | 2.89 | — | 2.99 | ns |
| $t_{COO\_EBR}$ | Clock (Write) to output from EBR output Register | — | 0.31 | — | 0.32 | — | 0.33 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | –0.218 | — | –0.227 | — | –0.237 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | 0.249 | — | 0.257 | — | 0.265 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | –0.071 | — | –0.070 | — | –0.068 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | 0.118 | — | 0.098 | — | 0.077 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory | –0.107 | — | –0.106 | — | –0.106 | — | ns |

*Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)*



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

# SERDES High-Speed Data Transmitter[1]

*Table 3-6. Serial Output Timing and Levels*

| Symbol | Description | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}1.44}$ | Differential swing (1.44 V setting)[1, 2] | 0.15 to 3.125 Gbps | 1150 | 1440 | 1730 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}1.35}$ | Differential swing (1.35 V setting)[1, 2] | 0.15 to 3.125 Gbps | 1080 | 1350 | 1620 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}1.26}$ | Differential swing (1.26 V setting)[1, 2] | 0.15 to 3.125 Gbps | 1000 | 1260 | 1510 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}1.13}$ | Differential swing (1.13 V setting)[1, 2] | 0.15 to 3.125 Gbps | 840 | 1130 | 1420 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}1.04}$ | Differential swing (1.04 V setting)[1, 2] | 0.15 to 3.125 Gbps | 780 | 1040 | 1300 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}0.92}$ | Differential swing (0.92 V setting)[1, 2] | 0.15 to 3.125 Gbps | 690 | 920 | 1150 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}0.87}$ | Differential swing (0.87 V setting)[1, 2] | 0.15 to 3.125 Gbps | 650 | 870 | 1090 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}0.78}$ | Differential swing (0.78 V setting)[1, 2] | 0.15 to 3.125 Gbps | 585 | 780 | 975 | mV, p-p |
| $V_{TX\text{-}DIFF\text{-}P\text{-}P\text{-}0.64}$ | Differential swing (0.64 V setting)[1, 2] | 0.15 to 3.125 Gbps | 480 | 640 | 800 | mV, p-p |
| $V_{OCM}$ | Output common mode voltage | — | $V_{CCOB}$ –0.75 | $V_{CCOB}$ –0.60 | $V_{CCOB}$ –0.45 | V |
| $T_{TX\text{-}R}$ | Rise time (20% to 80%) | — | 145 | 185 | 265 | ps |
| $T_{TX\text{-}F}$ | Fall time (80% to 20%) | — | 145 | 185 | 265 | ps |
| $Z_{TX\text{-}OI\text{-}SE}$ | Output Impedance 50/75/HiZ Ohms (single ended) | — | –20% | 50/75/ Hi Z | +20% | Ohms |
| $R_{LTX\text{-}RL}$ | Return loss (with package) | — | 10 | | | dB |
| $T_{TX\text{-}INTRASKEW}$ | Lane-to-lane TX skew within a SERDES quad block (intra-quad) | — | — | — | 200 | ps |
| $T_{TX\text{-}INTERSKEW}$[3] | Lane-to-lane skew between SERDES quad blocks (inter-quad) | — | — | — | 1UI +200 | ps |

1. All measurements are with 50 Ohm impedance.
2. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for actual binary settings and the min-max range.
3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

*Figure 3-14. Jitter Transfer – 3.125 Gbps*

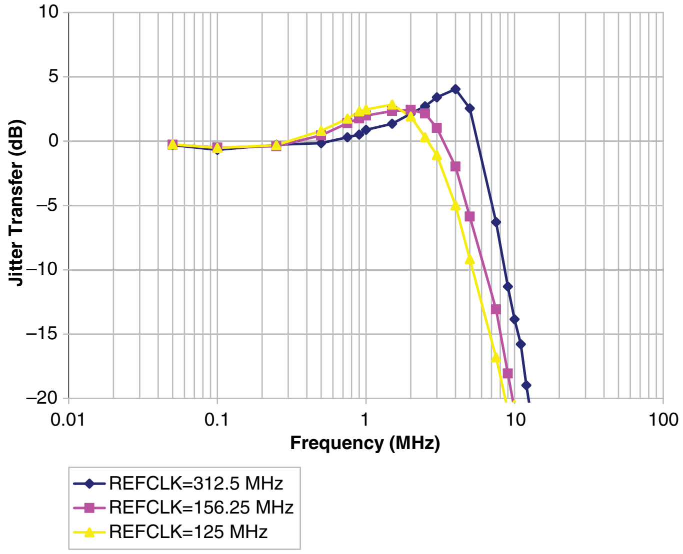
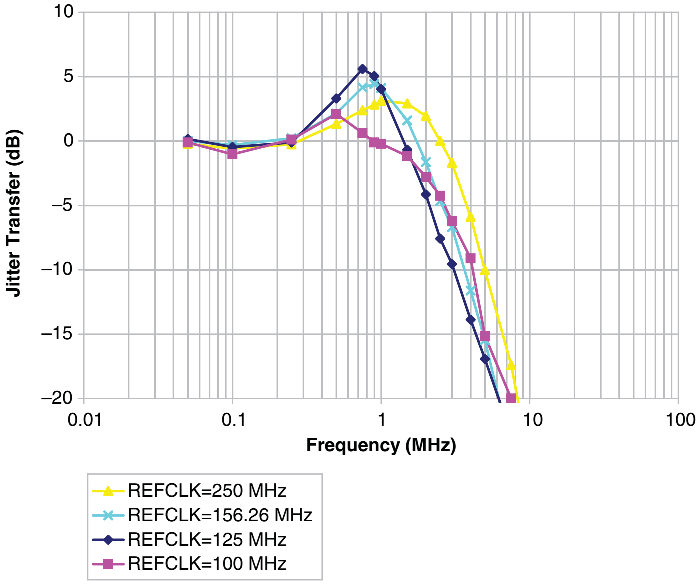
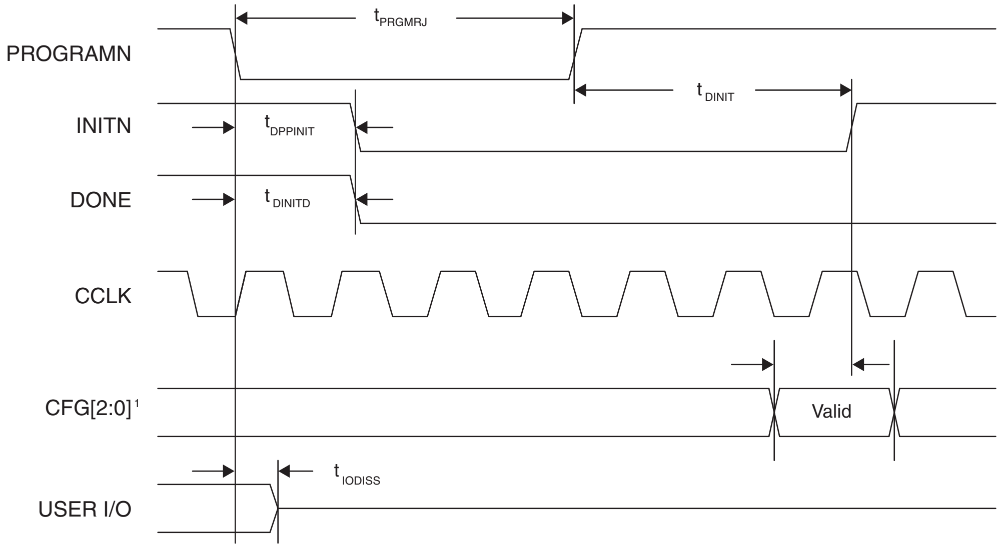


*Figure 3-15. Jitter Transfer – 2.5 Gbps*

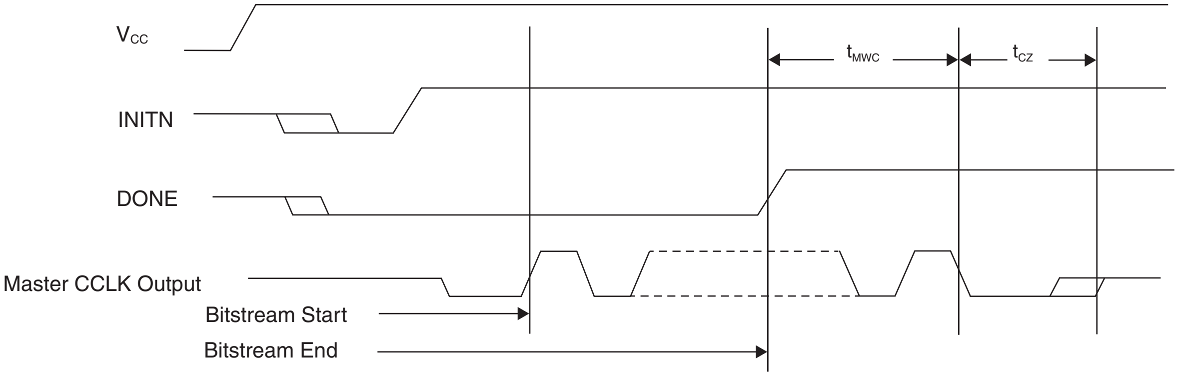


## Figure 3-26. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

## Figure 3-27. Wake-Up Timing



## Pin Information Summary (Cont.)

| Pin Information Summary | | ECP3-95EA | | | ECP3-150EA | |
|---|---|---|---|---|---|---|
| **Pin Type** | | **484 fpBGA** | **672 fpBGA** | **1156 fpBGA** | **672 fpBGA** | **1156 fpBGA** |
| General Purpose Inputs/Outputs per bank | Bank 0 | 42 | 60 | 86 | 60 | 94 |
| | Bank 1 | 36 | 48 | 78 | 48 | 86 |
| | Bank 2 | 24 | 34 | 36 | 34 | 58 |
| | Bank 3 | 54 | 59 | 86 | 59 | 104 |
| | Bank 6 | 63 | 67 | 86 | 67 | 104 |
| | Bank 7 | 36 | 48 | 54 | 48 | 76 |
| | Bank 8 | 24 | 24 | 24 | 24 | 24 |
| General Purpose Inputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 4 | 8 | 8 | 8 | 8 |
| | Bank 3 | 4 | 12 | 12 | 12 | 12 |
| | Bank 6 | 4 | 12 | 12 | 12 | 12 |
| | Bank 7 | 4 | 8 | 8 | 8 | 8 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| General Purpose Outputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 | 0 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| Total Single-Ended User I/O | | 295 | 380 | 490 | 380 | 586 |
| VCC | | 16 | 32 | 32 | 32 | 32 |
| VCCAUX | | 8 | 12 | 16 | 12 | 16 |
| VTT | | 4 | 4 | 8 | 4 | 8 |
| VCCA | | 4 | 8 | 16 | 8 | 16 |
| VCCPLL | | 4 | 4 | 4 | 4 | 4 |
| VCCIO | Bank 0 | 2 | 4 | 4 | 4 | 4 |
| | Bank 1 | 2 | 4 | 4 | 4 | 4 |
| | Bank 2 | 2 | 4 | 4 | 4 | 4 |
| | Bank 3 | 2 | 4 | 4 | 4 | 4 |
| | Bank 6 | 2 | 4 | 4 | 4 | 4 |
| | Bank 7 | 2 | 4 | 4 | 4 | 4 |
| | Bank 8 | 2 | 2 | 2 | 2 | 2 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 |
| TAP | | 4 | 4 | 4 | 4 | 4 |
| GND, GNDIO | | 98 | 139 | 233 | 139 | 233 |
| NC | | 0 | 0 | 238 | 0 | 116 |
| Reserved[1] | | 2 | 2 | 2 | 2 | 2 |
| SERDES | | 26 | 52 | 78 | 52 | 104 |
| Miscellaneous Pins | | 8 | 8 | 8 | 8 | 8 |
| Total Bonded Pins | | 484 | 672 | 1156 | 672 | 1156 |

## LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

### Commercial

| Part Number | Voltage | Grade | Power | Package[1] | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-17EA-6FTN256C | 1.2 V | –6 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-7FTN256C | 1.2 V | –7 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-8FTN256C | 1.2 V | –8 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-6LFTN256C | 1.2 V | –6 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-7LFTN256C | 1.2 V | –7 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-8LFTN256C | 1.2 V | –8 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-6MG328C | 1.2 V | –6 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-7MG328C | 1.2 V | –7 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-8MG328C | 1.2 V | –8 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-6LMG328C | 1.2 V | –6 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-7LMG328C | 1.2 V | –7 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-8LMG328C | 1.2 V | –8 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-6FN484C | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-7FN484C | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-8FN484C | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-6LFN484C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-7LFN484C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-8LFN484C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | COM | 17 |

1. Green = Halogen free and lead free.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-35EA-6FTN256C | 1.2 V | –6 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-7FTN256C | 1.2 V | –7 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-8FTN256C | 1.2 V | –8 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-6LFTN256C | 1.2 V | –6 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-7LFTN256C | 1.2 V | –7 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-8LFTN256C | 1.2 V | –8 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-6FN484C | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-7FN484C | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-8FN484C | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-6LFN484C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-7LFN484C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-8LFN484C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-6FN672C | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-7FN672C | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-8FN672C | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-6LFN672C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-7LFN672C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-8LFN672C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | COM | 33 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672C | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672C | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672C | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6LFN672C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7LFN672C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8LFN672C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156C | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156C | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156C | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-6LFN1156C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7LFN1156C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8LFN1156C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672CTW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672CTW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672CTW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156CTW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156CTW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156CTW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | COM | 149 |

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250 V.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2010 | 01.6 | Architecture | Added Read-Before-Write information. |
| | | DC and Switching Characteristics | Added footnote #6 to Maximum I/O Buffer Speed table. |
| | | | Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table. |
| | | Pinout Information | Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | Ordering Information | Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | | Removed dual mark information. |
| November 2009 | 01.5 | Introduction | Updated Embedded SERDES features. |
| | | | Added SONET/SDH to Embedded SERDES protocols. |
| | | Architecture | Updated Figure 2-4, General Purpose PLL Diagram. |
| | | | Updated SONET/SDH to SERDES and PCS protocols. |
| | | | Updated Table 2-13, SERDES Standard Support to include SONET/SDH and updated footnote 2. |
| | | DC and Switching Characterisitcs | Added footnote to ESD Performance table. |
| | | | Updated SERDES Power Supply Requirements table and footnotes. |
| | | | Updated Maximum I/O Buffer Speed table. |
| | | | Updated Pin-to-Pin Peformance table. |
| | | | Updated sysCLOCK PLL Timing table. |
| | | | Updated DLL timing table. |
| | | | Updated High-Speed Data Transmitter tables. |
| | | | Updated High-Speed Data Receiver table. |
| | | | Updated footnote for Receiver Total Jitter Tolerance Specification table. |
| | | | Updated Periodic Receiver Jitter Tolerance Specification table. |
| | | | Updated SERDES External Reference Clock Specification table. |
| | | | Updated PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Updated SMPTE AC/DC Characteristics Transmit table. |
| | | | Updated Mini LVDS table. |
| | | | Updated RSDS table. |
| | | | Added Supply Current (Standby) table for EA devices. |
| | | | Updated Internal Switching Characteristics table. |
| | | | Updated Register-to-Register Performance table. |
| | | | Added HDMI Electrical and Timing Characteristics data. |
| | | | Updated Family Timing Adders table. |
| | | | Updated sysCONFIG Port Timing Specifications table. |
| | | | Updated Recommended Operating Conditions table. |
| | | | Updated Hot Socket Specifications table. |
| | | | Updated Single-Ended DC table. |
| | | | Updated TRLVDS table and figure. |
| | | | Updated Serial Data Input Specifications table. |
| | | | Updated HDMI Transmit and Receive table. |
| | | Ordering Information | Added LFE3-150EA “TW” devices and footnotes to the Commercial and Industrial tables. |