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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

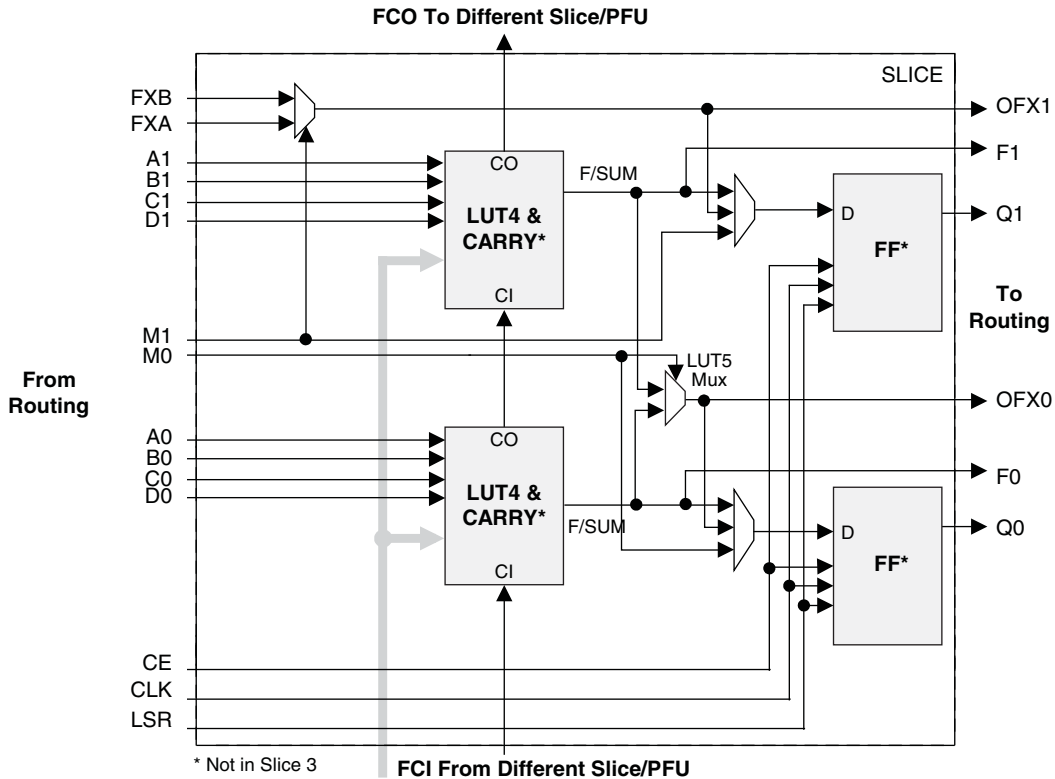
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-6ftn256c

Figure 2-3. Slice Diagram



* Not in Slice 3

For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
 WCK is CLK
 WRE is from LSR
 DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
 WAD [A:D] is a 4-bit address from slice 2 LUT input

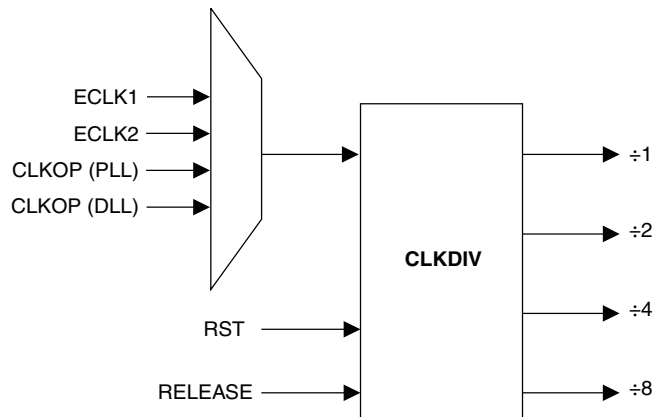
Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Figure 2-8. Clock Divider Connections



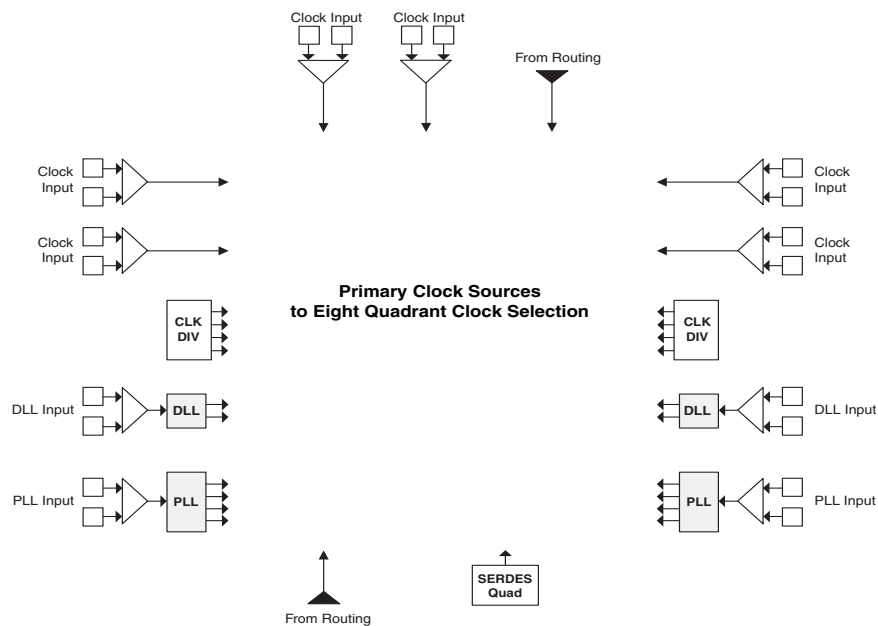
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

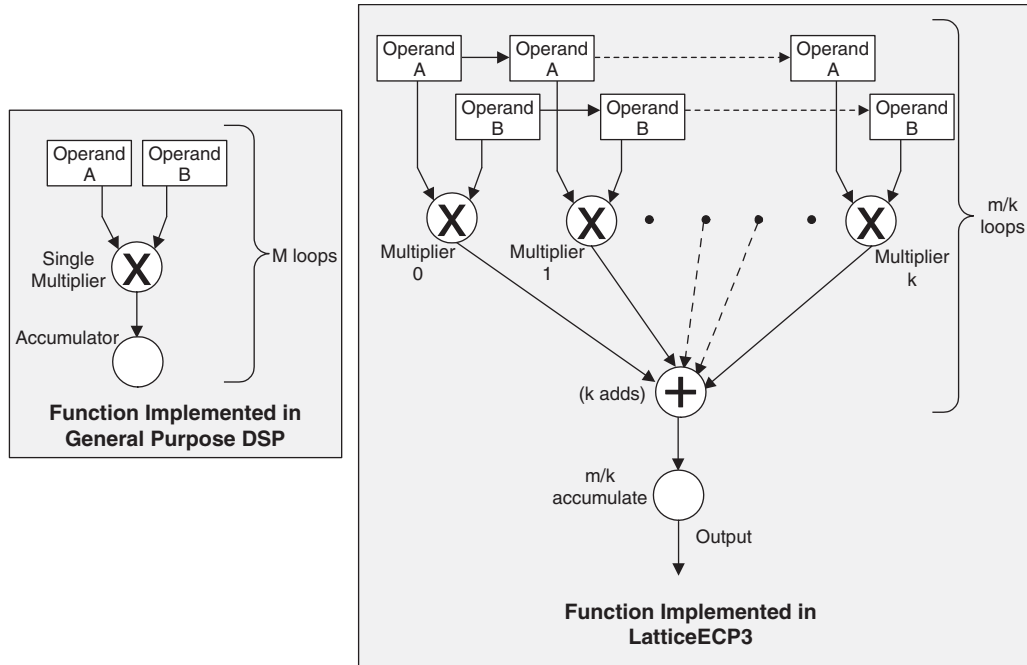
Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches



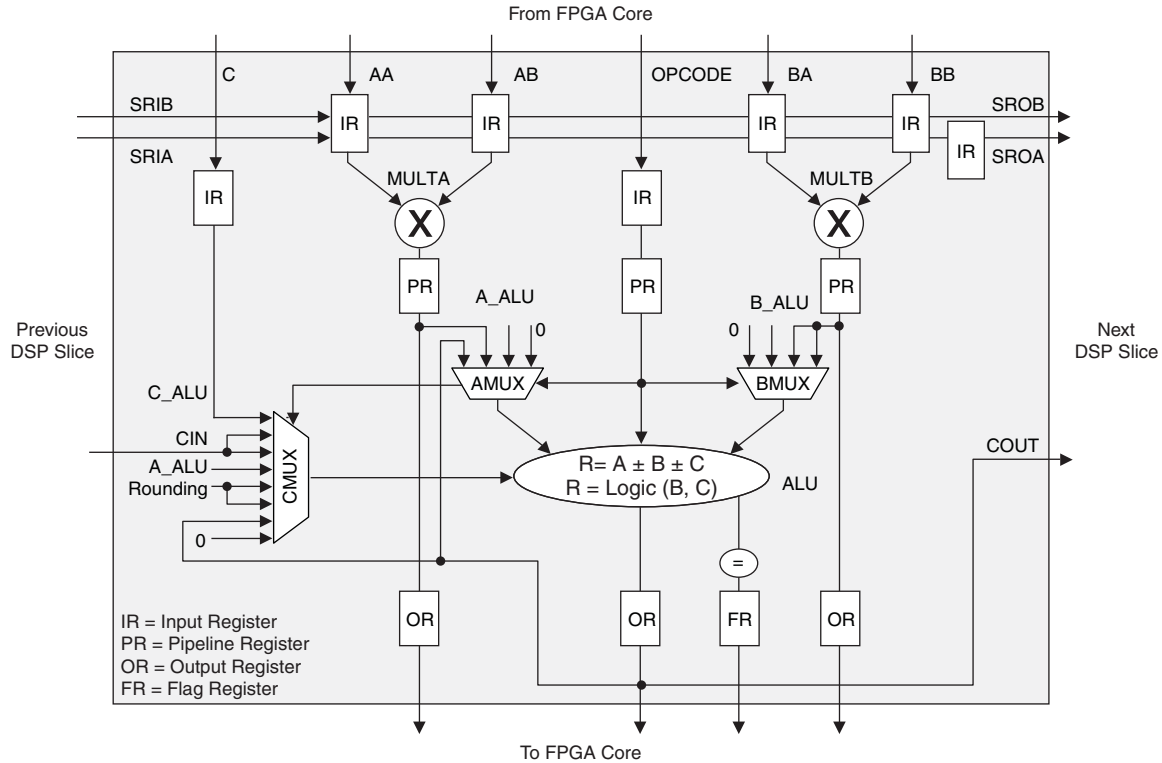
LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multipliers per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multipliers feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

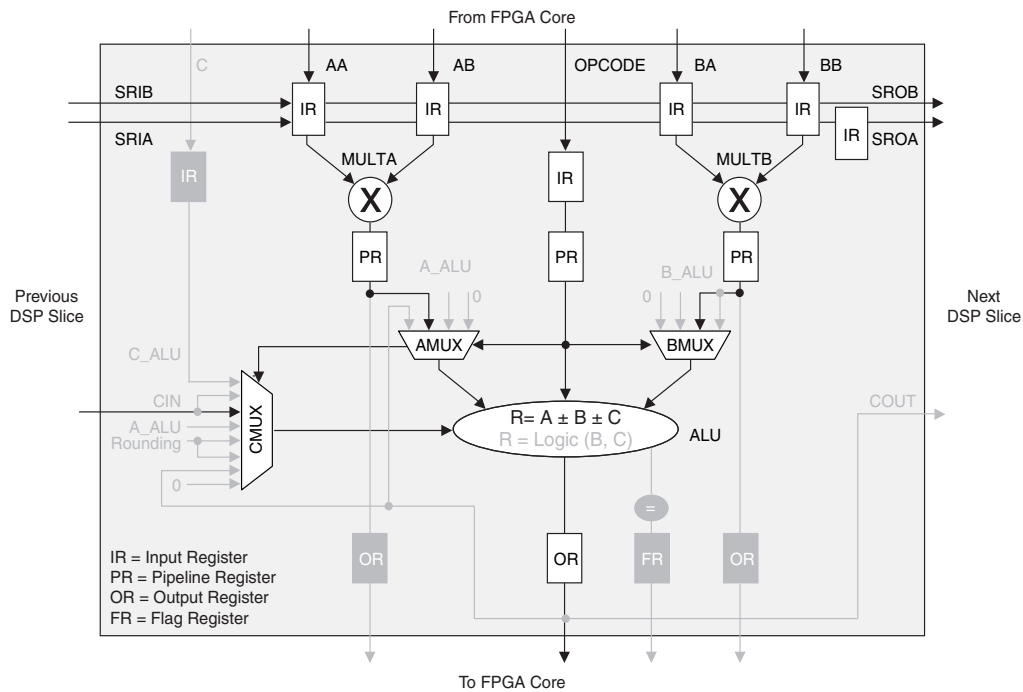
Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

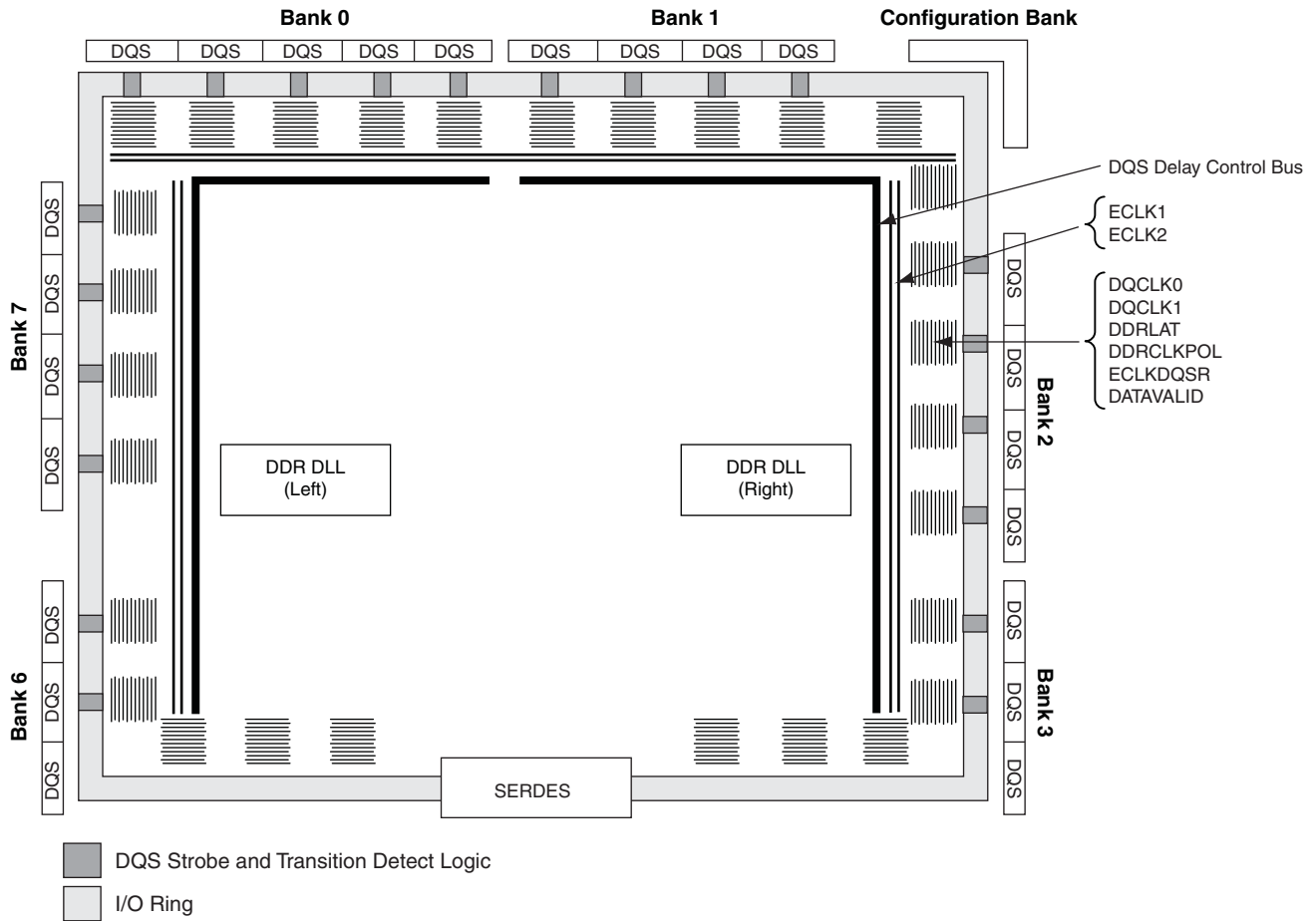
The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



*Includes shared configuration I/Os and dedicated configuration I/Os.

Please see TN1177, [LatticeECP3 sysIO Usage Guide](#) for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel $\div 1$, $\div 2$ and $\div 11$ rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS ⁴	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH} \text{ (Max.)}$	—	—	+/-1	mA
IDK ⁵	Input or I/O Leakage Current	$0 \leq V_{IN} < V_{CCIO}$	—	—	+/-1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5V$	—	18	—	mA

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .
3. LVCMOS and LVTTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements^{1, 2}

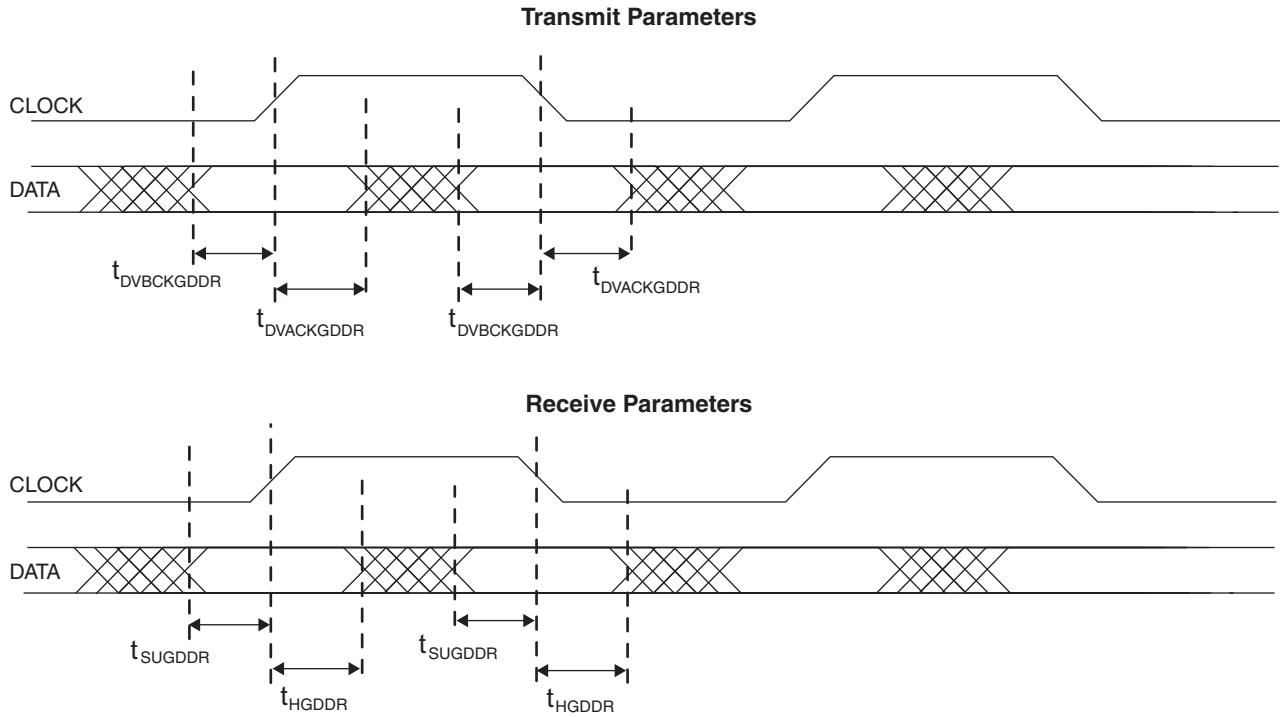
Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed V_{CCOB} (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be $8 \text{ mA} \times 16 \text{ channels} \times 2 \text{ input pins per channel} = 256 \text{ mA}$

ESD Performance

Please refer to the [LatticeECP3 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

Figure 3-8. Generic DDRX1/DDR2 (With Clock Center on Data Window)



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units	
f _{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz	
			Primary clock ⁴	2	—	420	MHz	
f _{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz	
			Primary clock ⁴	4	—	420	MHz	
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz	
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz	
f _{VCO}	PLL VCO frequency			500	—	1000	MHz	
f _{PDF} ³	Phase detector input frequency		Edge clock	2	—	500	MHz	
			Primary clock ⁴	2	—	420	MHz	
AC Characteristics								
t _{PA}	Programmable delay unit			65	130	260	ps	
t _{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%	
			f _{OUT} ≤ 250 MHz	Primary clock	45	50	55	%
			f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CFA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period	
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns	
t _{OPJIT} ¹	Output clock period jitter	f _{OUT} ≥ 420 MHz		—	—	200	ps	
		420 MHz > f _{OUT} ≥ 100 MHz		—	—	250	ps	
		f _{OUT} < 100 MHz		—	—	0.025	UIPP	
t _{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps	
t _{LOCK} ²	Lock time	2 to 25 MHz		—	—	200	us	
		25 to 500 MHz		—	—	50	us	
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns	
t _{HI}	Input clock high time	90% to 90%		0.5	—	—	ns	
t _{LO}	Input clock low time	10% to 10%		0.5	—	—	ns	
t _{IPJIT}	Input clock period jitter			—	—	400	ps	
t _{RST}	Reset signal pulse width high, RSTK			10	—	—	ns	
	Reset signal pulse width high, RST			500	—	—	ns	

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for f_{PDF} > 4 MHz. For f_{PDF} < 4 MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for f_{PDF} < 4 MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

SERDES High-Speed Data Transmitter¹

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44 V setting) ^{1,2}	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35 V setting) ^{1,2}	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26 V setting) ^{1,2}	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13 V setting) ^{1,2}	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04 V setting) ^{1,2}	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92 V setting) ^{1,2}	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87 V setting) ^{1,2}	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78 V setting) ^{1,2}	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64 V setting) ^{1,2}	0.15 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$ ³	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 Ohm impedance.

2. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for actual binary settings and the min-max range.

3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

SERDES External Reference Clock

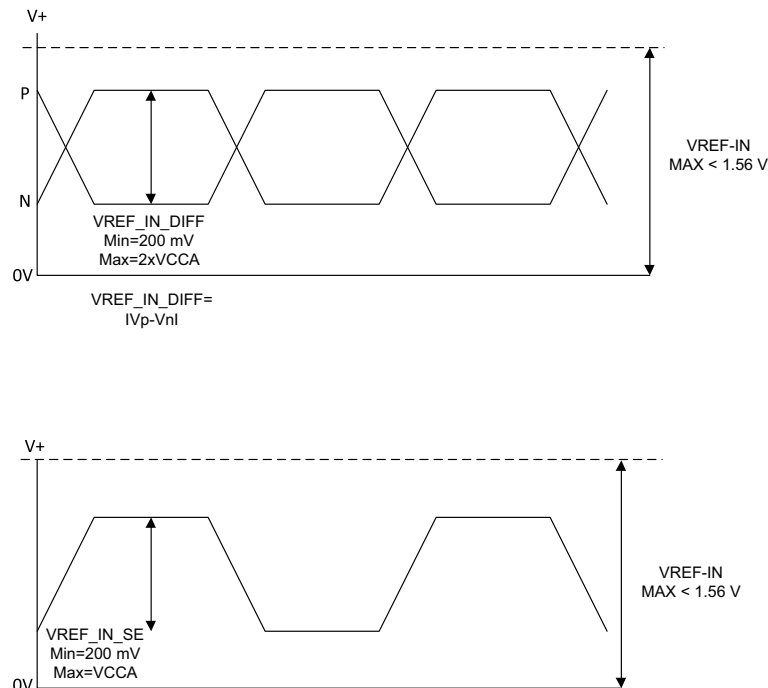
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance ¹	-1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock ²	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2 \cdot V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCA} + 0.3$	V
D_{REF}	Duty cycle ³	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	-20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms



Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential impedance		80	100	120	Ohms
$J_{TX_DDJ}^{3,4,5}$	Output data deterministic jitter		—	—	0.10	UI
$J_{TX_TJ}^{2,3,4,5}$	Total output data jitter		—	—	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pF load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
$J_{RX_DJ}^{1,2,3,4,5}$	Deterministic jitter tolerance (peak-to-peak)		—	—	0.34	UI
$J_{RX_RJ}^{1,2,3,4,5}$	Random jitter tolerance (peak-to-peak)		—	—	0.26	UI
$J_{RX_SJ}^{1,2,3,4,5}$	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.11	UI
$J_{RX_TJ}^{1,2,3,4,5}$	Total jitter tolerance (peak-to-peak)		—	—	0.71	UI
T_{RX_EYE}	Receiver eye opening		0.29	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

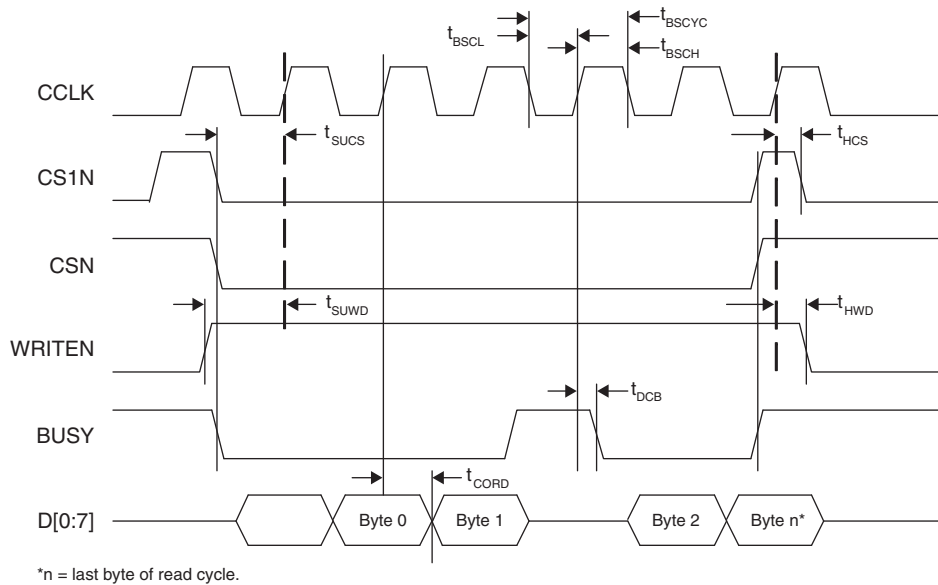
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{SSCL}	CCLK Minimum Low Pulse	5	—	ns
t_{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle

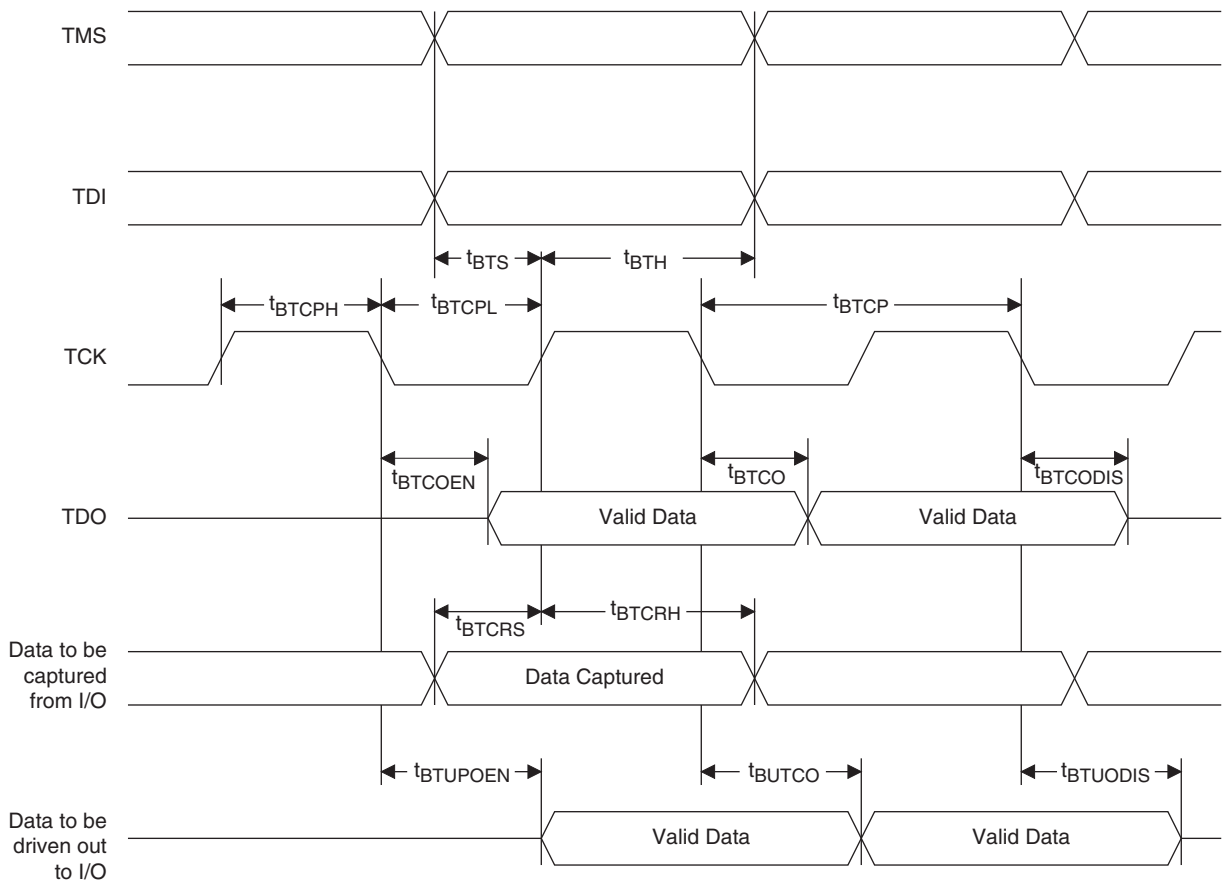


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

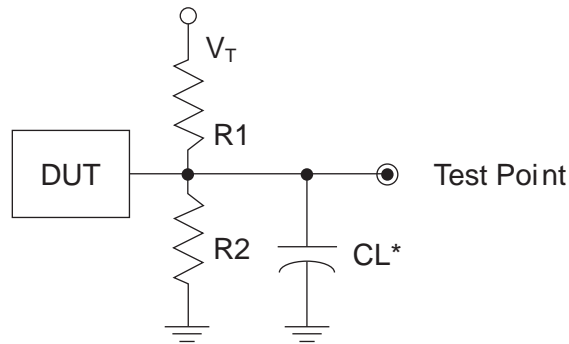
Figure 3-32. JTAG Port Timing Waveforms



Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*spFNpkgCTW* and LFE3-150EA-*spFNpkgITW* devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*spFNpkgC* and LFE3-150EA-*spFNpkgI* devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250 V.

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Date	Version	Section	Change Summary
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characteristics	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI} , t_{W_EDGE} and $t_{SKEW_EDGE_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT} .
			External Reference Clock Specification (refclkp/refclkcn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$.
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC} .
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
			Updated Mini LVDS table.
August 2009	01.3	DC and Switching Characteristics	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
July 2009	01.2	Multiple	Changed references of "multi-boot" to "dual-boot" throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characteristics	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.

Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram. Updated Device Configuration text section. Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table. Corrected footnote 2 in sysIO Recommended Operating Conditions table. Added added footnote 7 for $t_{\text{SKEW_PRIB}}$ to External Switching Characteristics table. Added 2-to-1 Gearing text section and table. Updated External Reference Clock Specification (refclkp/refclk) table. LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information. Added sysCONFIG Port Timing waveform. Serial Input Data Specifications table, delete Typ data for $V_{\text{RX-DIFF-S}}$. Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD} . Added SERDES/PCS Block Latency Breakdown table. External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF. Added SERDES External Reference Clock Waveforms. Updated Serial Output Timing and Levels table. Pin-to-pin performance table, changed "typically 3% slower" to "typically slower". Updated timing information Updated SERDES minimum frequency. Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements. Updated Serial Input Data Specifications table. Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables. Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	—	Initial release.