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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	222
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-6lfn484i

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

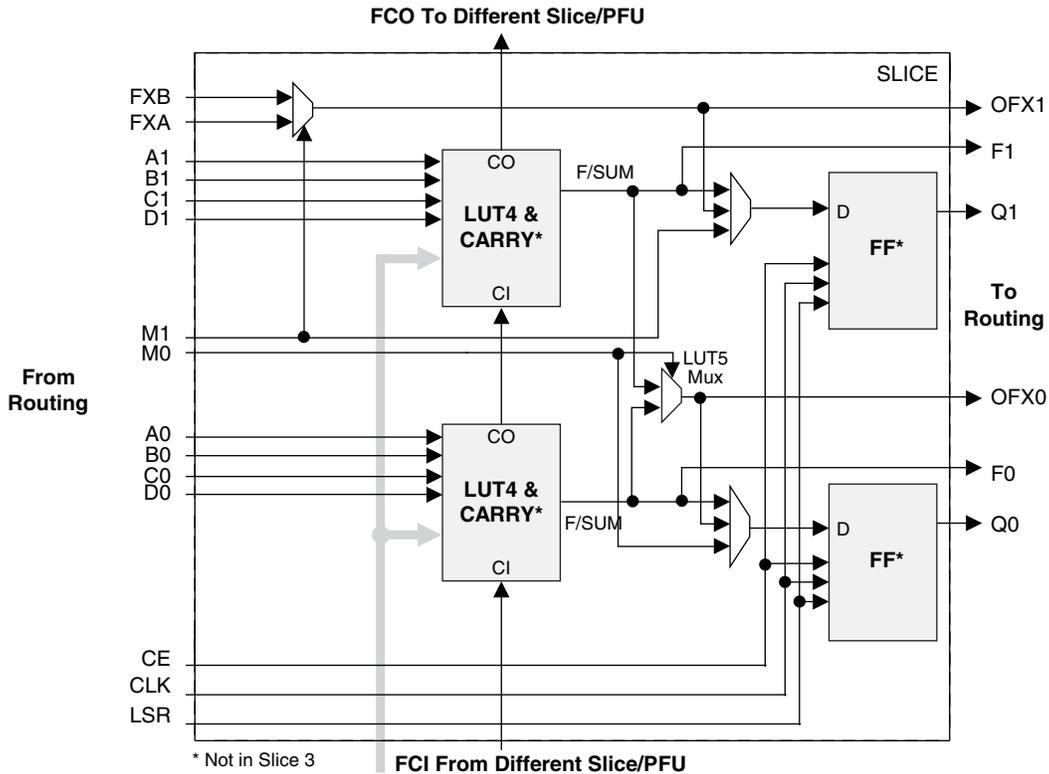
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Table 2-5. DLL Signals

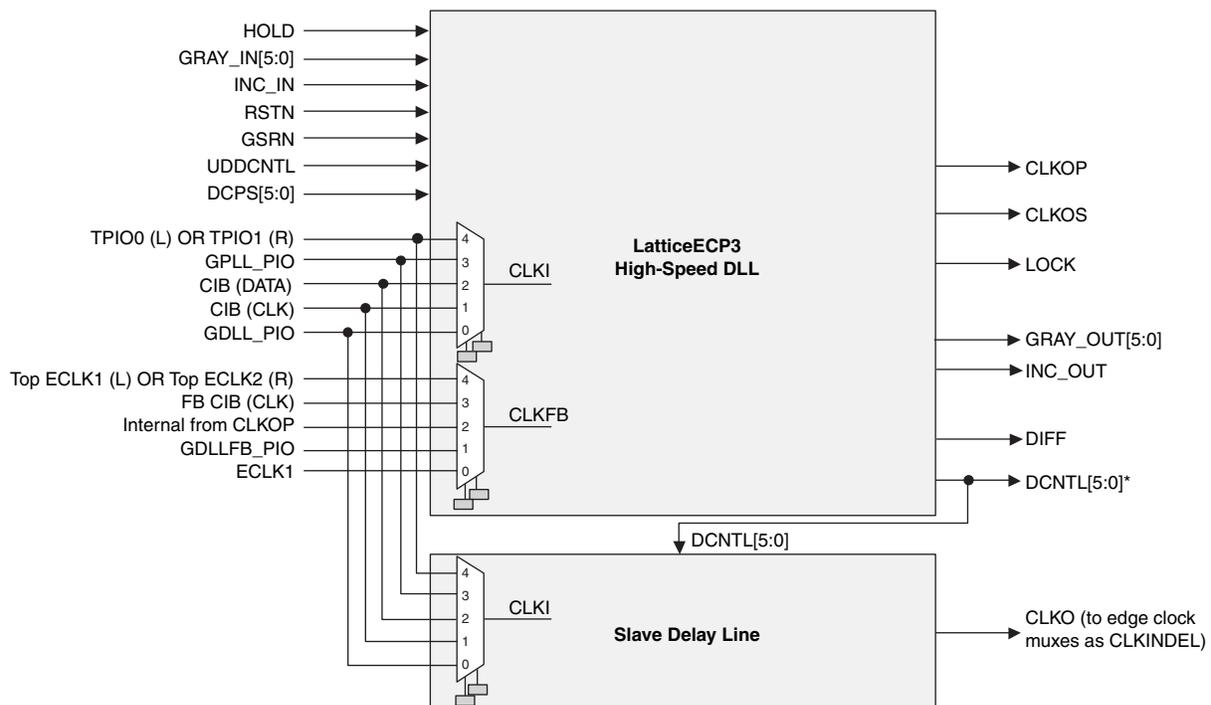
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

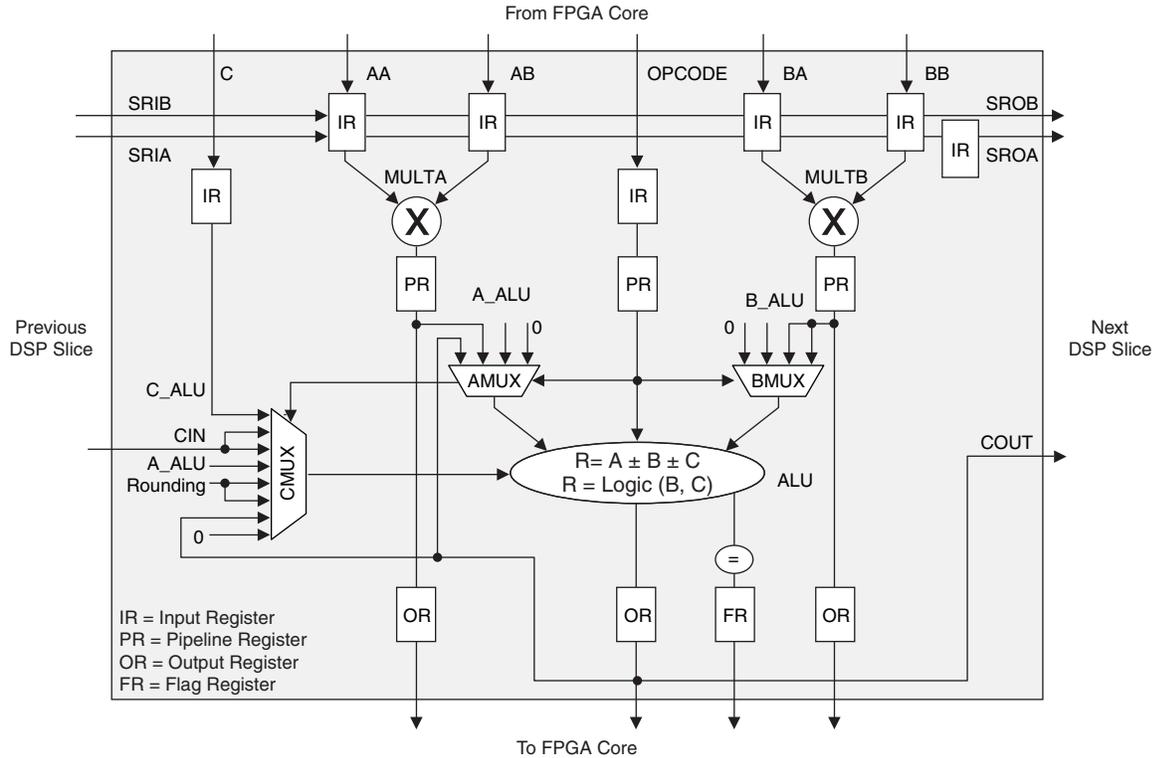
For more information, please see TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#).

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



* This signal is not user accessible. It can only be used to feed the slave delay line.

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

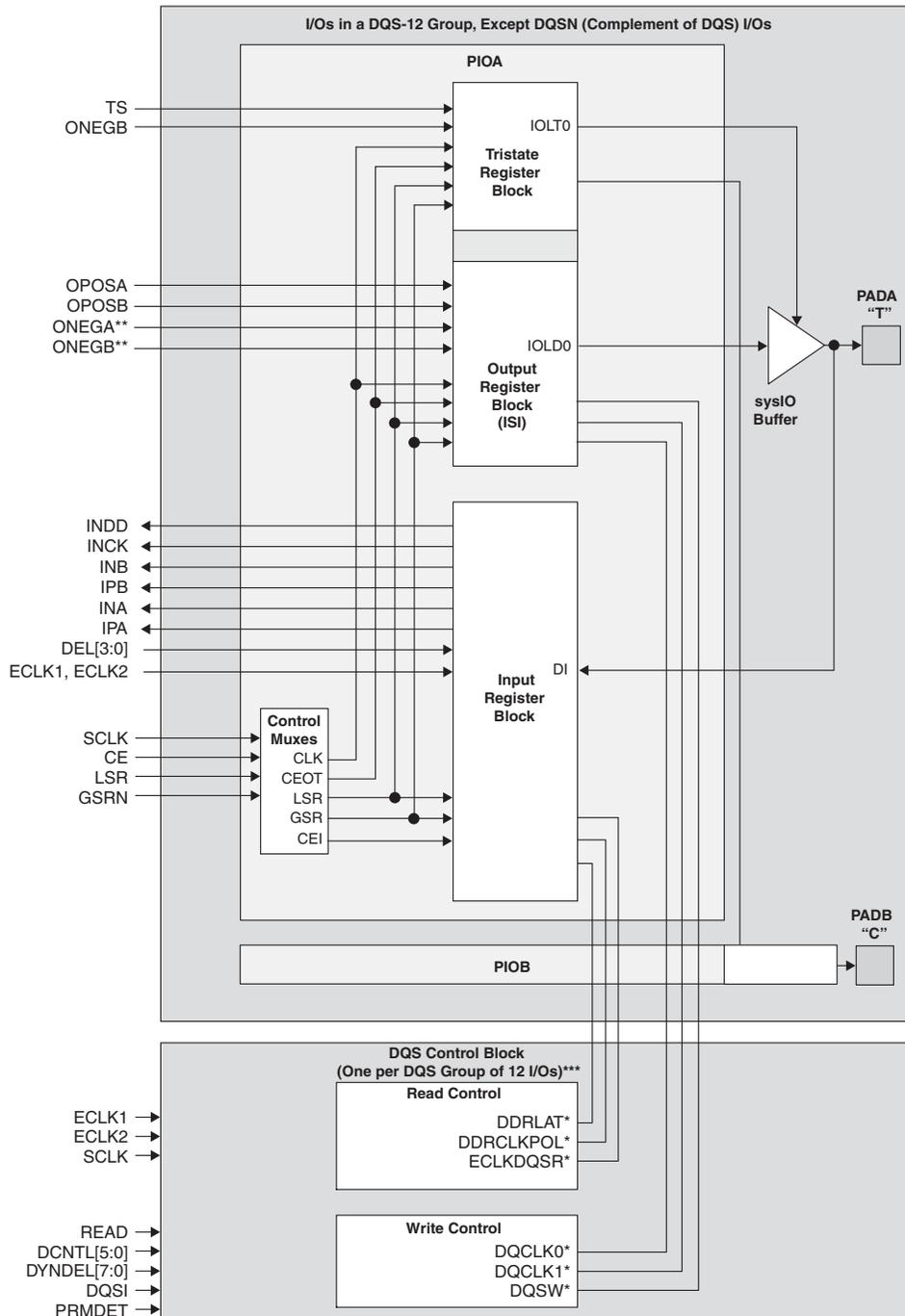
Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

Programmable I/O Cells (PIC)

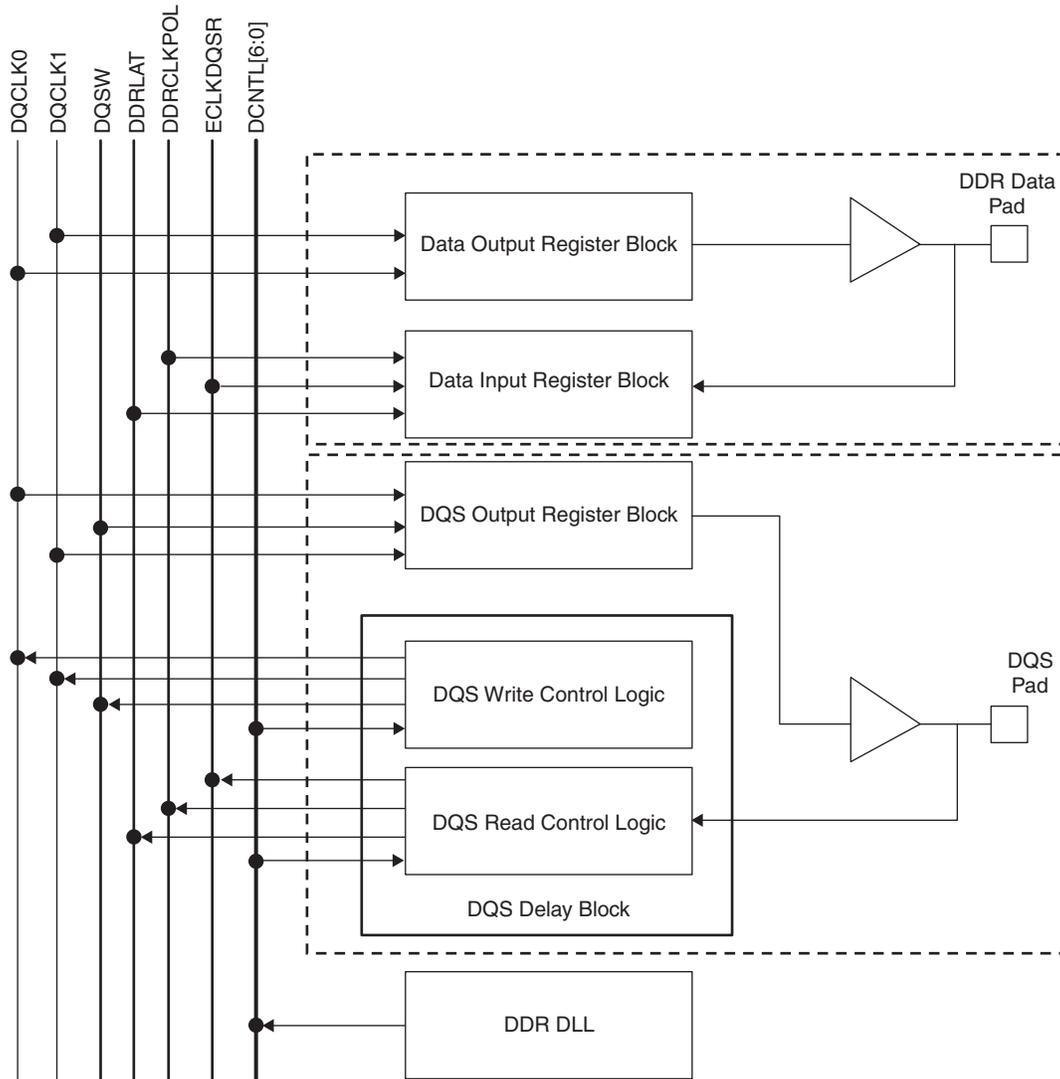
Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
 ** Signals are available on the left and right sides only
 *** Selected PIO.

Figure 2-37. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

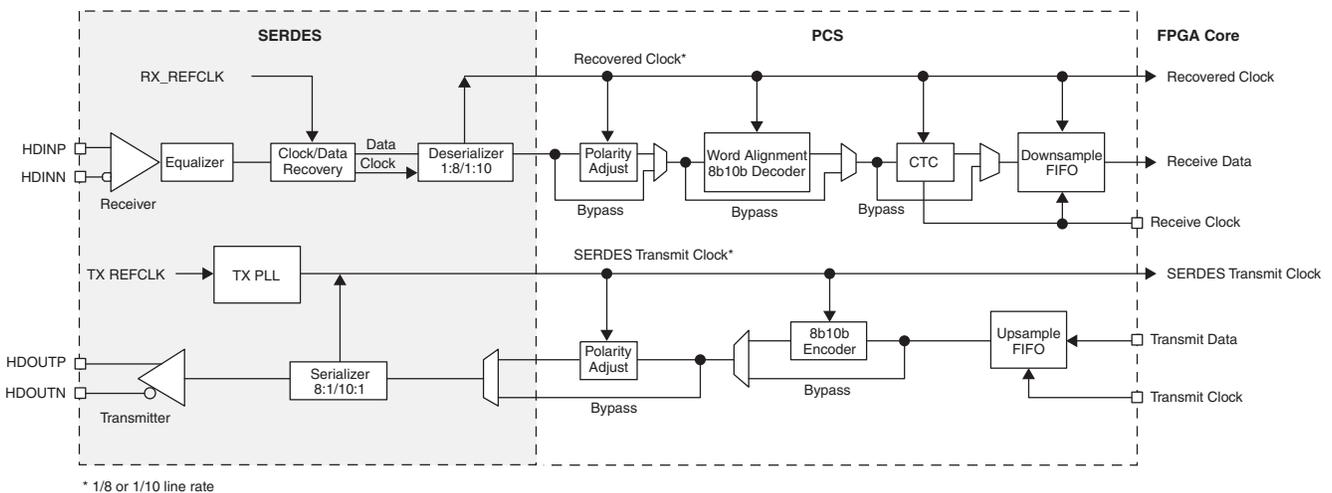
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, [LatticeECP3 sysCONFIG Usage Guide](#).

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, [LatticeECP3 sysCONFIG Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

1. JTAG
2. Standard Serial Peripheral Interface (SPI and SPI_{MEM} modes) - interface to boot PROM memory
3. System microprocessor to drive a x8 CPU port (PCM mode)
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Generic byte wide flash with a MachXO™ device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

MCCLK (MHz)	MCCLK (MHz)
	10
2.5 ¹	13
4.3	15 ²
5.4	20
6.9	26
8.1	33 ³
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the [LatticeECP3 Pin Migration Tables](#) and Diamond software for specific restrictions and limitations.

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS ⁴	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH} \text{ (Max.)}$	—	—	+/-1	mA
IDK ⁵	Input or I/O Leakage Current	$0 \leq V_{IN} < V_{CCIO}$	—	—	+/-1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5V$	—	18	—	mA

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .
3. LVCMOS and LVTTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements^{1, 2}

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed V_{CCOB} (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the [LatticeECP3 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	—	4.1	—	4.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	—	1.4	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	—	1.5	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	—	500	—	420	—	375	MHz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting²									
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.3	—	3.6	—	3.9	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SU_DELP}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
t _{H_DELP}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.3	—	3.5	—	3.8	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.8	—	0.9	—	ns

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDR2_TX.PLL.Centered)¹⁰									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f _{MAX_GDDR}	DDR2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)⁴									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing									
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	-90	90	-90	90	-90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jitter During DLL Locking Period	All ECP3 Devices	—	180	—	180	—	180	ps

- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
- General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
- Generic DDR timing numbers based on LVDS I/O.
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
- DDR3 timing numbers based on SSTL15.
- Uses LVDS I/O standard.
- The current version of software does not support per bank skew numbers; this will be supported in a future release.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- Using settings generated by IPexpress.
- These numbers are generated using best case PLL located in the center of the device.
- Uses SSTL25 Class II Differential I/O Standard.
- All numbers are generated with ispLEVER 8.1 software.
- For details on -9 speed grade devices, please contact your Lattice Sales Representative.

LatticeECP3 Internal Switching Characteristics^{1, 2, 5}
Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t _{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.097	—	-0.103	—	-0.109	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t _{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t _{SUDATA_PFU}	Data Setup Time	-0.137	—	-0.155	—	-0.174	—	ns
t _{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.227	—	-0.257	—	-0.286	—	ns
t _{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.055	—	-0.055	—	-0.063	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay ⁴	-	1.09	-	1.16	-	1.23	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.085	—	-0.072	—	-0.058	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.107	—	-0.094	—	-0.081	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.218	—	-0.227	—	-0.237	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.071	—	-0.070	—	-0.068	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.107	—	-0.106	—	-0.106	—	ns

LatticeECP3 Maximum I/O Buffer Speed ^{1, 2, 3, 4, 5, 6}
Over Recommended Operating Conditions

Buffer	Description	Max.	Units
Maximum Input Frequency			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
PPLVDS	Point-to-Point LVDS	400	MHz
TRLVDS	Transition-Reduced LVDS	612	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	400	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
HSTL15	HSTL_15 class I, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, $V_{CCIO} = 3.3\text{ V}$	400	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, $V_{CCIO} = 2.5\text{ V}$	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	166	MHz
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	166	MHz
LVC MOS15	LVC MOS 1.5, $V_{CCIO} = 1.5\text{ V}$	166	MHz
LVC MOS12	LVC MOS 1.2, $V_{CCIO} = 1.2\text{ V}$	166	MHz
PCI33	PCI, $V_{CCIO} = 3.3\text{ V}$	66	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	612	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
RS DS25	RS DS, Emulated, $V_{CCIO} = 2.5\text{ V}$	612	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
PPLVDS	Point-to-point LVDS	612	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	612	MHz
Mini-LVDS	Mini LVDS	612	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	200	MHz
HSTL15 (all supported classes)	HSTL_15 class I, $V_{CCIO} = 1.5\text{ V}$	200	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, $V_{CCIO} = 3.3\text{ V}$	233	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, $V_{CCIO} = 2.5\text{ V}$	233	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	266	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	166	MHz
LVC MOS33 (For all drives)	LVC MOS, 3.3 V	166	MHz
LVC MOS25 (For all drives)	LVC MOS, 2.5 V	166	MHz
LVC MOS18 (For all drives)	LVC MOS, 1.8 V	166	MHz
LVC MOS15 (For all drives)	LVC MOS, 1.5 V	166	MHz
LVC MOS12 (For all drives except 2 mA)	LVC MOS, $V_{CCIO} = 1.2\text{ V}$	166	MHz
LVC MOS12 (2 mA drive)	LVC MOS, $V_{CCIO} = 1.2\text{ V}$	100	MHz

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units	
f _{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz	
			Primary clock ⁴	2	—	420	MHz	
f _{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz	
			Primary clock ⁴	4	—	420	MHz	
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz	
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz	
f _{VCO}	PLL VCO frequency			500	—	1000	MHz	
f _{PDF} ³	Phase detector input frequency		Edge clock	2	—	500	MHz	
			Primary clock ⁴	2	—	420	MHz	
AC Characteristics								
t _{PA}	Programmable delay unit			65	130	260	ps	
t _{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%	
			f _{OUT} ≤ 250 MHz	Primary clock	45	50	55	%
			f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CFA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period	
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns	
t _{OPJIT} ¹	Output clock period jitter	f _{OUT} ≥ 420 MHz		—	—	200	ps	
		420 MHz > f _{OUT} ≥ 100 MHz		—	—	250	ps	
		f _{OUT} < 100 MHz		—	—	0.025	UIPP	
t _{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps	
t _{LOCK} ²	Lock time	2 to 25 MHz		—	—	200	us	
		25 to 500 MHz		—	—	50	us	
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns	
t _{HI}	Input clock high time	90% to 90%		0.5	—	—	ns	
t _{LO}	Input clock low time	10% to 10%		0.5	—	—	ns	
t _{IPJIT}	Input clock period jitter			—	—	400	ps	
t _{RST}	Reset signal pulse width high, RSTK			10	—	—	ns	
	Reset signal pulse width high, RST			500	—	—	ns	

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for f_{PDF} > 4 MHz. For f_{PDF} < 4 MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for f_{PDF} < 4 MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

SERDES High-Speed Data Transmitter¹

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44 V setting) ^{1,2}	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35 V setting) ^{1,2}	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26 V setting) ^{1,2}	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13 V setting) ^{1,2}	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04 V setting) ^{1,2}	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92 V setting) ^{1,2}	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87 V setting) ^{1,2}	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78 V setting) ^{1,2}	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64 V setting) ^{1,2}	0.15 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$ ³	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 Ohm impedance.

2. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for actual binary settings and the min-max range.

3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential impedance		80	100	120	Ohms
$J_{TX_DDJ}^{2,3,4}$	Output data deterministic jitter		—	—	0.17	UI
$J_{TX_TJ}^{1,2,3,4}$	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
$J_{RX_DJ}^{1,2,3}$	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
$J_{RX_RJ}^{1,2,3}$	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
$J_{RX_SJ}^{1,2,3}$	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
$J_{RX_TJ}^{1,2,3}$	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOU/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at <http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3> and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools > Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- [Thermal Management](#) document
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.