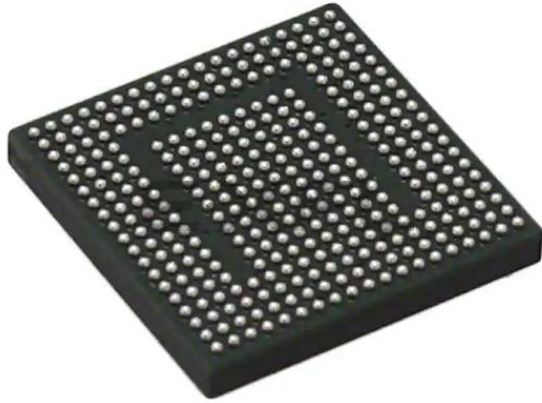




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	116
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	328-LFBGA, CSBGA
Supplier Device Package	328-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-7lmg328i

Introduction

The LatticeECP3™ (Economy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

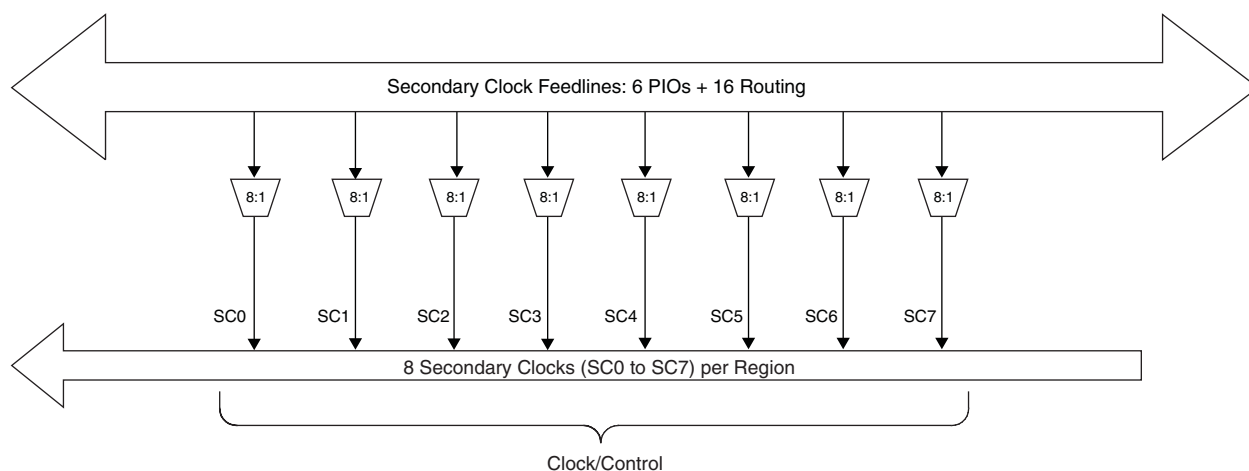
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

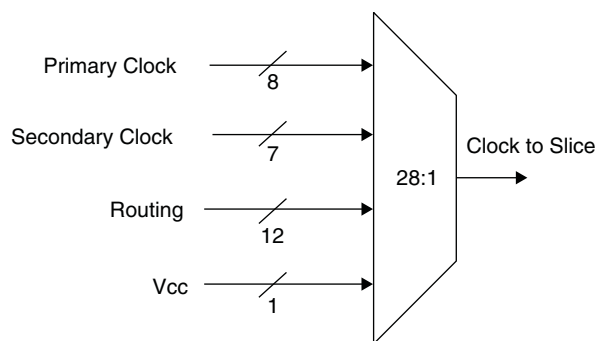
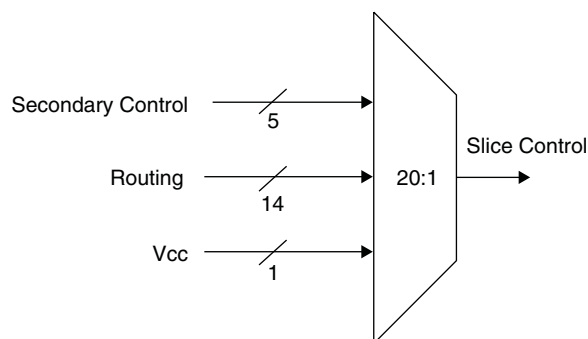


Figure 2-18. Slice0 through Slice2 Control Selection



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

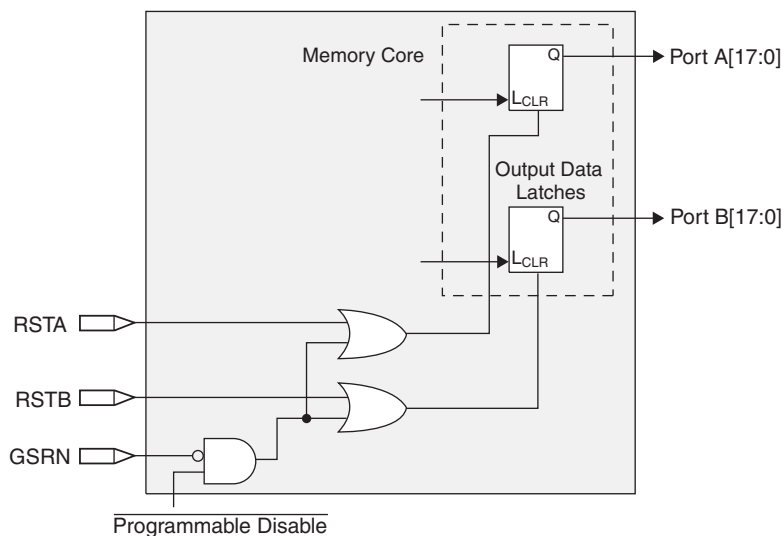
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

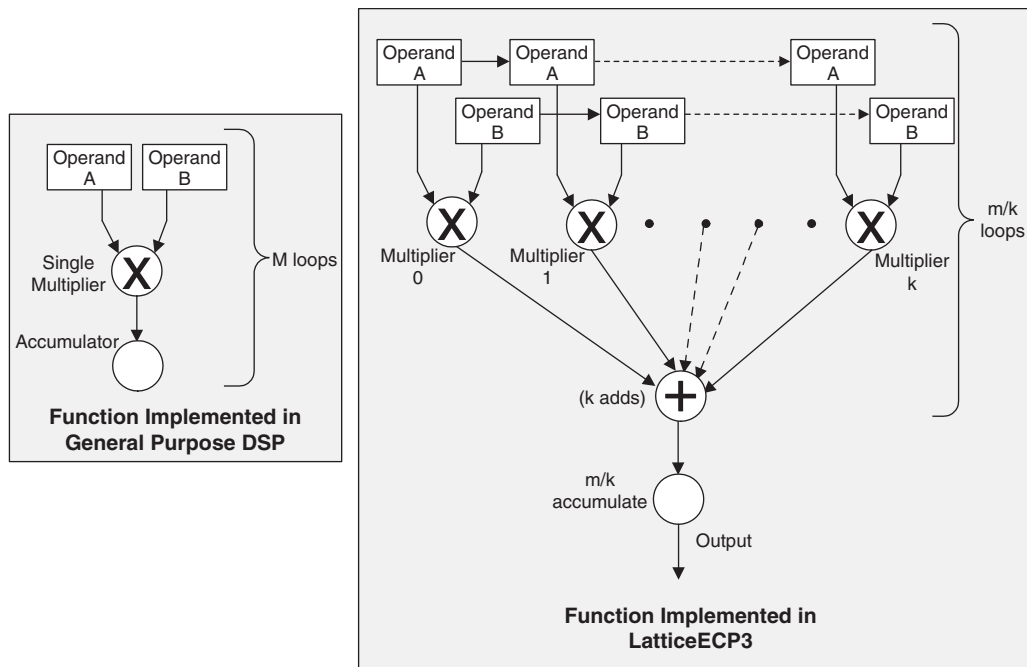
The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches



LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

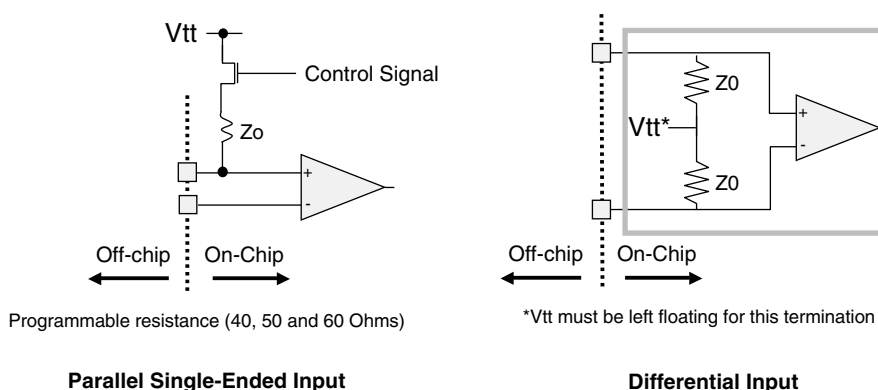
Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

Figure 2-39. On-Chip Termination



See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT ^{1,2}	DIFFERENTIAL TERMINATION RESISTOR ¹
LVDS25	p	80, 100, 120
BLVDS25	p	80, 100, 120
MLVDS	p	80, 100, 120
HSTL18_I	40, 50, 60	p
HSTL18_II	40, 50, 60	p
HSTL18D_I	40, 50, 60	p
HSTL18D_II	40, 50, 60	p
HSTL15_I	40, 50, 60	p
HSTL15D_I	40, 50, 60	p
SSTL25_I	40, 50, 60	p
SSTL25_II	40, 50, 60	p
SSTL25D_I	40, 50, 60	p
SSTL25D_II	40, 50, 60	p
SSTL18_I	40, 50, 60	p
SSTL18_II	40, 50, 60	p
SSTL18D_I	40, 50, 60	p
SSTL18D_II	40, 50, 60	p
SSTL15	40, 50, 60	p
SSTL15D	40, 50, 60	p

1. TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.
Use of TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

MCCLK (MHz)	MCCLK (MHz)
	10
2.5 ¹	13
4.3	15 ²
5.4	20
6.9	26
8.1	33 ³
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the [LatticeECP3 Pin Migration Tables](#) and Diamond software for specific restrictions and limitations.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2 \text{ V})$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2 \text{ V}) < V_{IN} \leq 3.6 \text{ V}$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-210	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (\text{MAX}) \leq V_{IN} \leq V_{CCIO}$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (\text{MAX})$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (\text{MAX})$	$V_{IL} (\text{MAX})$	—	$V_{IH} (\text{MIN})$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	7	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$.

3. Applicable to general purpose I/Os in top and bottom banks.

4. When used as V_{REF} maximum leakage = $25 \mu\text{A}$.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS18	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS15	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS12	-0.3	$0.35 V_{CC}$	$0.65 V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI33	-0.3	$0.3 V_{CCIO}$	$0.5 V_{CCIO}$	3.6	$0.1 V_{CCIO}$	$0.9 V_{CCIO}$	1.5	-0.5
SSTL18_I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
SSTL18_II (DDR2 Memory)	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.28	$V_{CCIO} - 0.28$	8	-8
							11	-11
SSTL2_I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
							12	-12
SSTL2_II (DDR Memory)	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
							20	-20
SSTL3_I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL3_II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL15 (DDR3 Memory)	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.3	$V_{CCIO} - 0.3$	7.5	-7.5
						$V_{CCIO} * 0.8$	9	-9
HSTL15_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
HSTL18_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
							12	-12
HSTL18_II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16

1. For electromigration, the average DC current drawn by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed $n * 8$ mA, where n is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Register-to-Register Performance^{1, 2, 3}

Function	-8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
3. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond and ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond and ispLEVER design tools can provide logic timing numbers at a particular temperature and voltage.

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	—	4.1	—	4.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	—	1.4	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	—	1.5	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	—	500	—	420	—	375	MHz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting²									
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.3	—	3.6	—	3.9	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SU_DELP}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
t _{H_DELP}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.3	—	3.5	—	3.8	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.8	—	0.9	—	ns

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	683	—	688	—	690	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	—	688	—	690	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	—	688	—	690	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data Aligned at Pin (GDDR1_TX.SCLK.Aligned)¹⁰									
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA	—	335	—	338	—	341	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-70EA/95EA	—	339	—	343	—	347	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-70EA/95EA	—	339	—	343	—	347	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-35EA	—	322	—	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-35EA	—	322	—	320	—	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-17EA	—	322	—	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-17EA	—	322	—	320	—	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR1_TX.DQS.Centered)¹⁰									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	670	—	675	—	676	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	—	676	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	—	250	—	250	MHz
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDR2_TX.Aligned)									
Left and Right Sides									
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDR2_TX.DQSDLL.Centered)¹¹									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400	—	400	—	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400	—	400	—	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz

LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)
Over Recommended Commercial Operating Conditions

Buffer Type	Description	–8	–7	–6	Units
RS2S25	RS2S, VCCIO = 2.5 V	–0.07	–0.04	–0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	–0.22	–0.19	–0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTTL33_4mA	LVTTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTTL33_8mA	LVTTTL 8 mA drive, VCCIO = 3.3V	–0.06	–0.06	–0.07	ns
LVTTTL33_12mA	LVTTTL 12 mA drive, VCCIO = 3.3V	–0.01	–0.02	–0.02	ns
LVTTTL33_16mA	LVTTTL 16 mA drive, VCCIO = 3.3V	–0.07	–0.07	–0.08	ns
LVTTTL33_20mA	LVTTTL 20 mA drive, VCCIO = 3.3V	–0.12	–0.13	–0.14	ns
LVC MOS33_4mA	LVC MOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVC MOS33_8mA	LVC MOS 3.3 8 mA drive, fast slew rate	–0.06	–0.06	–0.07	ns
LVC MOS33_12mA	LVC MOS 3.3 12 mA drive, fast slew rate	–0.01	–0.02	–0.02	ns
LVC MOS33_16mA	LVC MOS 3.3 16 mA drive, fast slew rate	–0.07	–0.07	–0.08	ns
LVC MOS33_20mA	LVC MOS 3.3 20 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVC MOS25_4mA	LVC MOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVC MOS25_8mA	LVC MOS 2.5 8 mA drive, fast slew rate	–0.05	–0.06	–0.07	ns
LVC MOS25_12mA	LVC MOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVC MOS25_20mA	LVC MOS 2.5 20 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVC MOS18_4mA	LVC MOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVC MOS18_8mA	LVC MOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVC MOS18_12mA	LVC MOS 1.8 12 mA drive, fast slew rate	–0.04	–0.03	–0.03	ns
LVC MOS18_16mA	LVC MOS 1.8 16 mA drive, fast slew rate	–0.04	–0.03	–0.03	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f _{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock ⁴	2	—	420	MHz
f _{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock ⁴	4	—	420	MHz
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f _{VCO}	PLL VCO frequency			500	—	1000	MHz
f _{PFD} ³	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock ⁴	2	—	420	MHz
AC Characteristics							
t _{PA}	Programmable delay unit			65	130	260	ps
t _{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		f _{OUT} ≤ 250 MHz	Primary clock	45	50	55	%
		f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t _{OPJIT} ¹	Output clock period jitter	f _{OUT} ≥ 420 MHz		—	—	200	ps
		420 MHz > f _{OUT} ≥ 100 MHz		—	—	250	ps
		f _{OUT} < 100 MHz		—	—	0.025	UIPP
t _{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps
t _{LOCK} ²	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t _{HI}	Input clock high time	90% to 90%		0.5	—	—	ns
t _{LO}	Input clock low time	10% to 10%		0.5	—	—	ns
t _{IPJIT}	Input clock period jitter			—	—	400	ps
t _{RST}	Reset signal pulse width high, RSTK			10	—	—	ns
	Reset signal pulse width high, RST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ^{1,2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

- Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
- Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
- All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
- The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F _{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC _V	Duty cycle, video clock		45	50	55	%

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW ¹	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW ¹	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW ¹	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW ¹	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW ¹	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW ¹	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*lTW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*l devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250 V.



LatticeECP3 Family Data Sheet

Revision History

March 2015

Data Sheet DS1021

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information All	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 . Minor style/formatting changes.
April 2014	02.7EA	DC and Switching Characteristics	Updated LatticeECP3 Supply Current (Standby) table power numbers. Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed I_{PW} to I_{PD} in footnote 3. Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching Characteristics	Updated the Wake-Up Timing Diagram Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysI/O Buffer Banks text section – Updated description of “Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)” for hot socketing information. sysI/O Buffer Banks text section – Updated description of “Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)” for PCI clamp information. On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard. sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1. Added Oscillator Output Frequency table. LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t_{CODO} parameter. LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.

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Date	Version	Section	Change Summary
March 2010	01.6	Architecture	Added Read-Before-Write information.
		DC and Switching Characteristics	Added footnote #6 to Maximum I/O Buffer Speed table. Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table.
		Pinout Information	Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices.
		Ordering Information	Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices.
			Removed dual mark information.
November 2009	01.5	Introduction	Updated Embedded SERDES features. Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram. Updated SONET/SDH to SERDES and PCS protocols.
			Updated Table 2-13, SERDES Standard Support to include SONET/SDH and updated footnote 2.
		DC and Switching Characteristics	Added footnote to ESD Performance table.
			Updated SERDES Power Supply Requirements table and footnotes.
			Updated Maximum I/O Buffer Speed table.
			Updated Pin-to-Pin Performance table.
			Updated sysCLOCK PLL Timing table.
			Updated DLL timing table.
			Updated High-Speed Data Transmitter tables.
			Updated High-Speed Data Receiver table.
			Updated footnote for Receiver Total Jitter Tolerance Specification table.
			Updated Periodic Receiver Jitter Tolerance Specification table.
			Updated SERDES External Reference Clock Specification table.
			Updated PCI Express Electrical and Timing AC and DC Characteristics.
			Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics.
			Updated SMPTE AC/DC Characteristics Transmit table.
			Updated Mini LVDS table.
			Updated RSDS table.
			Added Supply Current (Standby) table for EA devices.
			Updated Internal Switching Characteristics table.
			Updated Register-to-Register Performance table.
			Added HDMI Electrical and Timing Characteristics data.
			Updated Family Timing Adders table.
			Updated sysCONFIG Port Timing Specifications table.
			Updated Recommended Operating Conditions table.
			Updated Hot Socket Specifications table.
			Updated Single-Ended DC table.
			Updated TRLVDS table and figure.
			Updated Serial Data Input Specifications table.
			Updated HDMI Transmit and Receive table.
		Ordering Information	Added LFE3-150EA "TW" devices and footnotes to the Commercial and Industrial tables.