



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

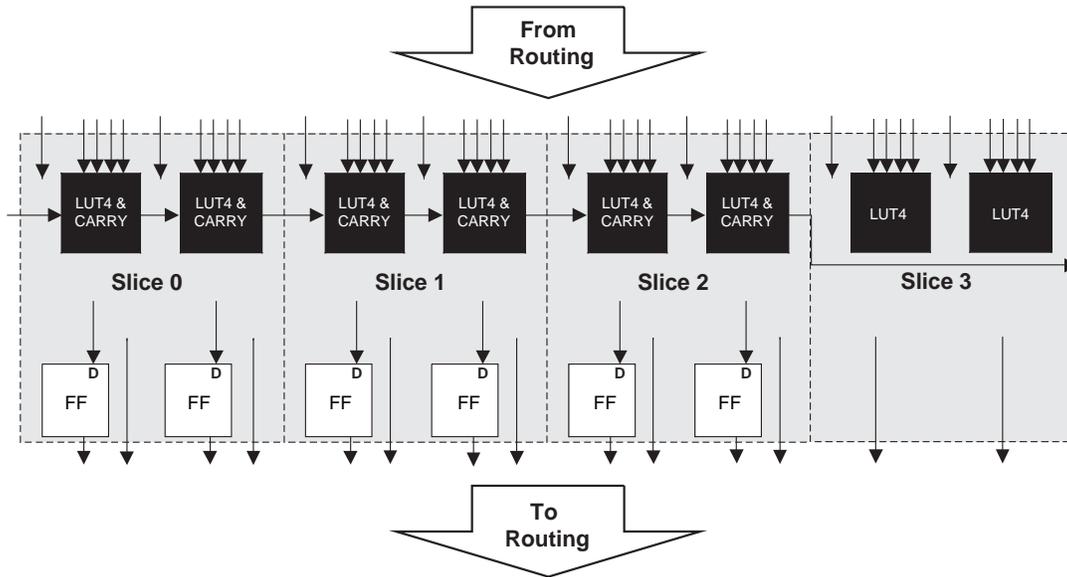
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	222
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-8fn484c

Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, [LatticeECP3 Memory Usage Guide](#).

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

Figure 2-4. General Purpose PLL Diagram

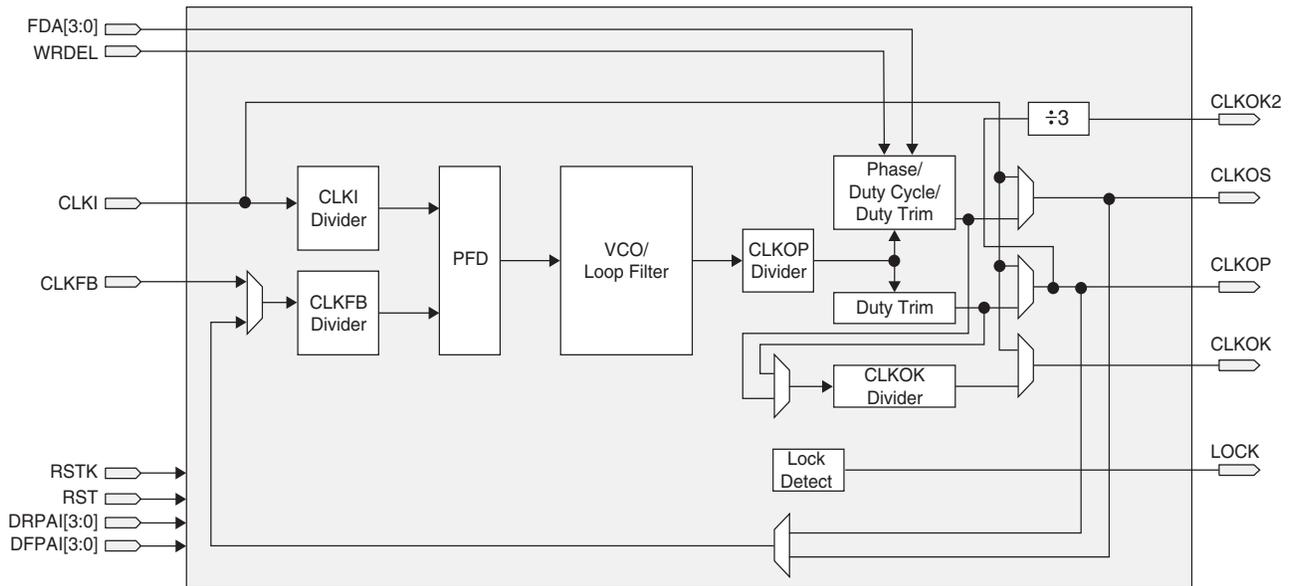


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKKOK	O	PLL output to clock tree through secondary clock divider
CLKKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

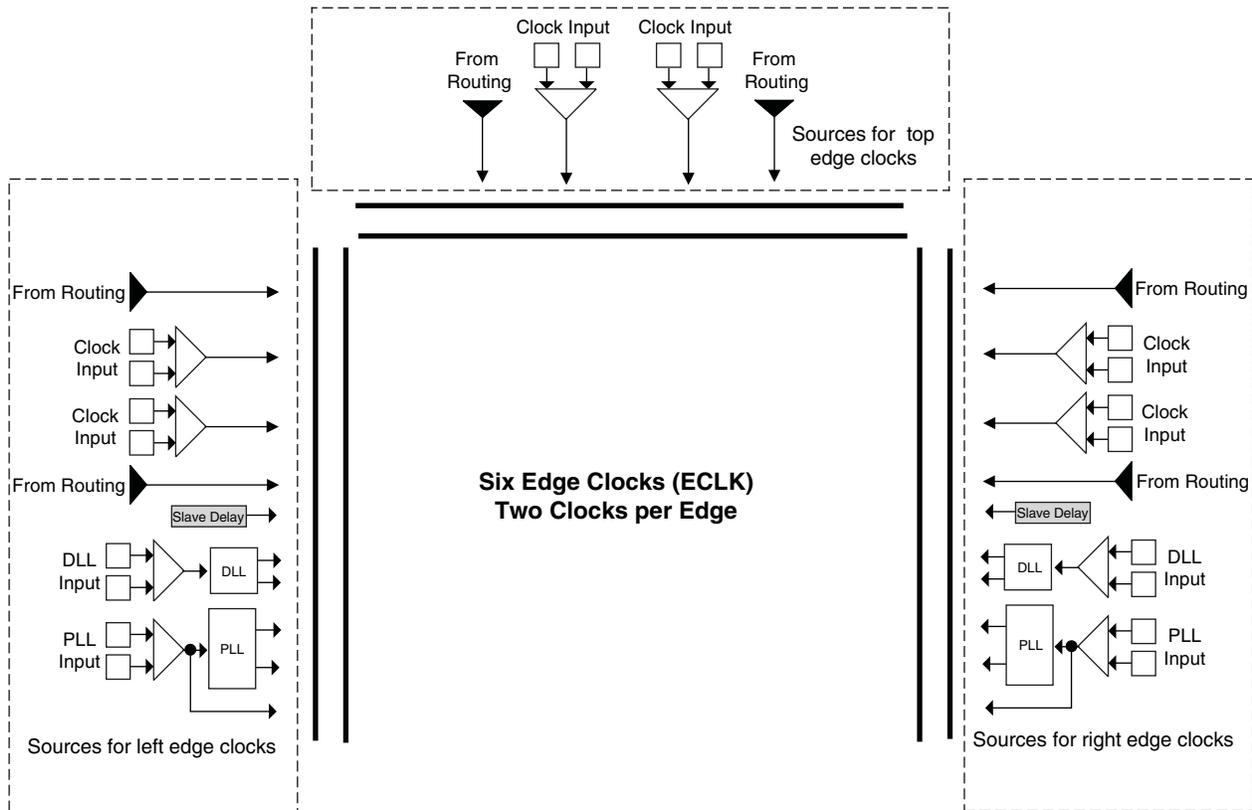
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

Figure 2-19. Edge Clock Sources



Notes:

1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, please see TN1179, [LatticeECP3 Memory Usage Guide](#).

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

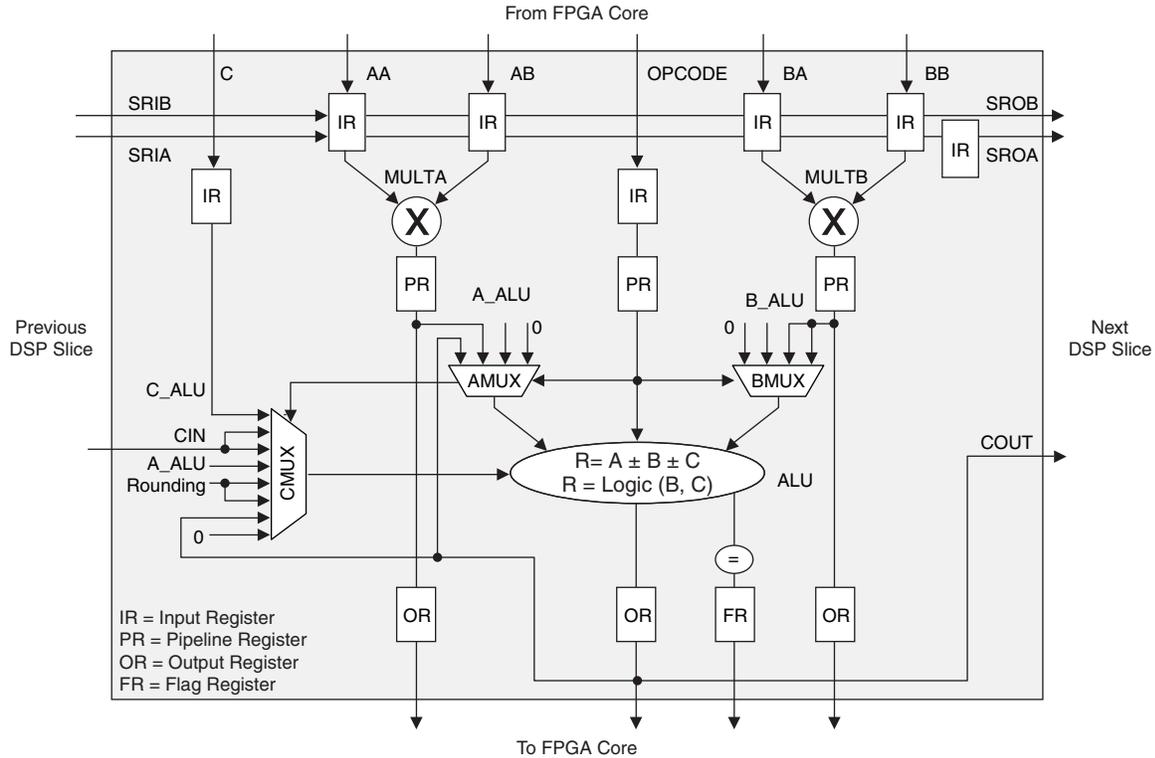
RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0

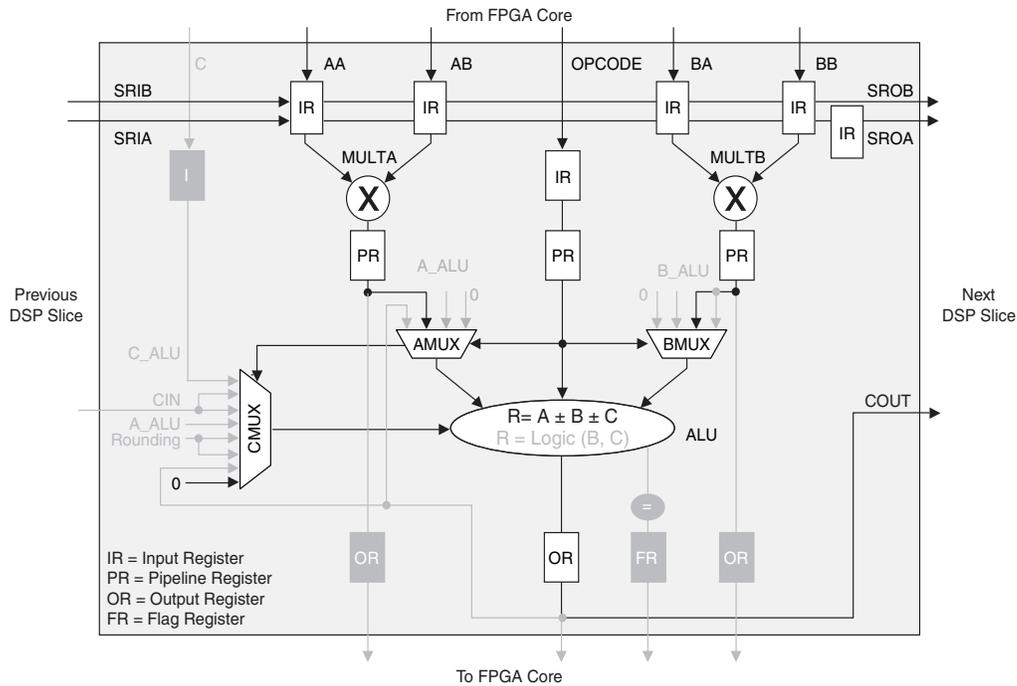
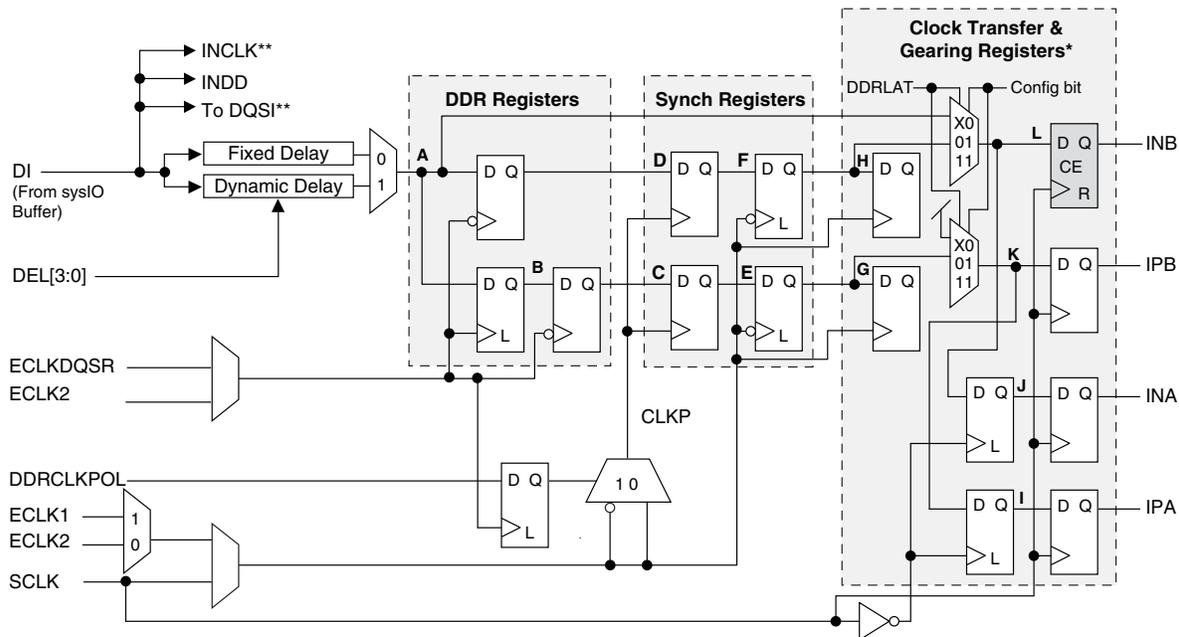


Figure 2-33. Input Register Block for Left, Right and Top Edges



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDR2 gearing of output logic. ODDR2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

MCCLK (MHz)	MCCLK (MHz)
	10
2.5 ¹	13
4.3	15 ²
5.4	20
6.9	26
8.1	33 ³
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the [LatticeECP3 Pin Migration Tables](#) and Diamond software for specific restrictions and limitations.



LatticeECP3 Family Data Sheet

DC and Switching Characteristics

April 2014

Data Sheet DS1021

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.32 V
Supply Voltage V_{CCAUX}	-0.5 V to 3.75 V
Supply Voltage V_{CCJ}	-0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied ⁴	-0.5 V to 3.75 V
Storage Temperature (Ambient)	-65 V to 150 °C
Junction Temperature (T_J)	+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^2	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^{2,4}$	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
$V_{CCIO}^{2,3}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^2	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}^5	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply⁶				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/ μ s during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.

© 2014 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2 \text{ V})$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2 \text{ V}) < V_{IN} \leq 3.6 \text{ V}$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-210	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (\text{MAX}) \leq V_{IN} \leq V_{CCIO}$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (\text{MAX})$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (\text{MAX})$	$V_{IL} (\text{MAX})$	—	$V_{IH} (\text{MIN})$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V},$ $V_{CC} = 1.2 \text{ V}, V_{IO} = 0 \text{ to } V_{IH} (\text{MAX})$	—	5	7	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25 °C, $f = 1.0 \text{ MHz}$.

3. Applicable to general purpose I/Os in top and bottom banks.

4. When used as V_{REF} maximum leakage = 25 μA .

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}^1, V_{INM}^1	Input Voltage		0	—	2.4	V
V_{CM}^1	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	μ A
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100$ Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

1, On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LatticeECP3 Internal Switching Characteristics^{1, 2, 5}
Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t _{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.097	—	-0.103	—	-0.109	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t _{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t _{SUDATA_PFU}	Data Setup Time	-0.137	—	-0.155	—	-0.174	—	ns
t _{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.227	—	-0.257	—	-0.286	—	ns
t _{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.055	—	-0.055	—	-0.063	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay ⁴	-	1.09	-	1.16	-	1.23	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.085	—	-0.072	—	-0.058	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.107	—	-0.094	—	-0.081	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.218	—	-0.227	—	-0.237	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.071	—	-0.070	—	-0.068	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.107	—	-0.106	—	-0.106	—	ns

SERDES High-Speed Data Transmitter¹

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44 V setting) ^{1,2}	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35 V setting) ^{1,2}	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26 V setting) ^{1,2}	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13 V setting) ^{1,2}	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04 V setting) ^{1,2}	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92 V setting) ^{1,2}	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87 V setting) ^{1,2}	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78 V setting) ^{1,2}	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64 V setting) ^{1,2}	0.15 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$ ³	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 Ohm impedance.

2. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for actual binary settings and the min-max range.

3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

Figure 3-16. Jitter Transfer – 1.25 Gbps

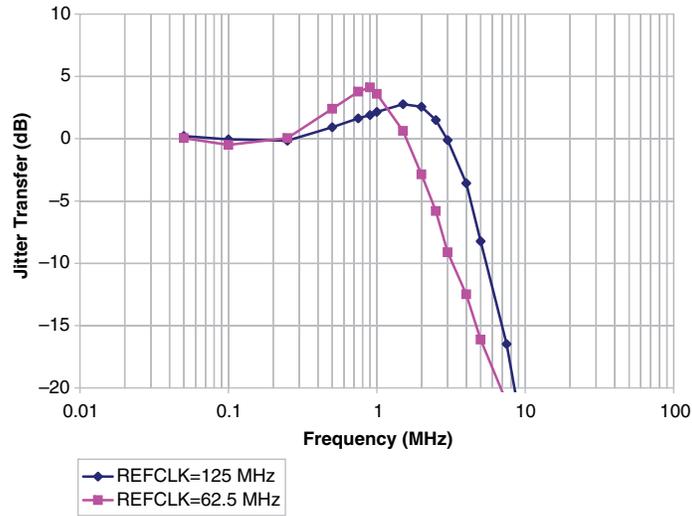


Figure 3-17. Jitter Transfer – 622 Mbps

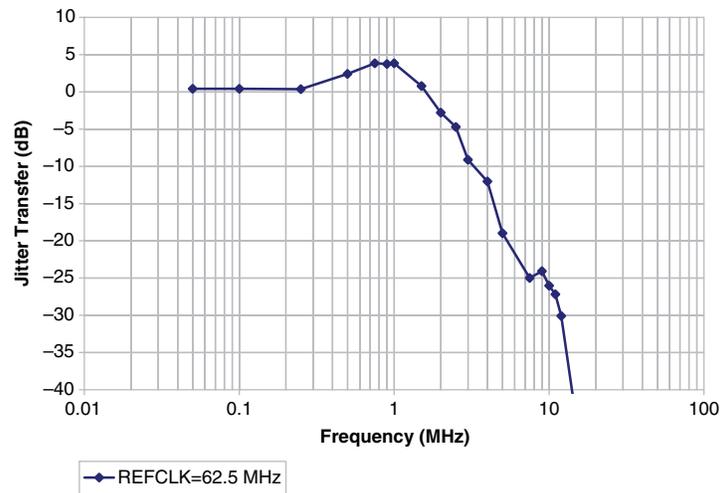
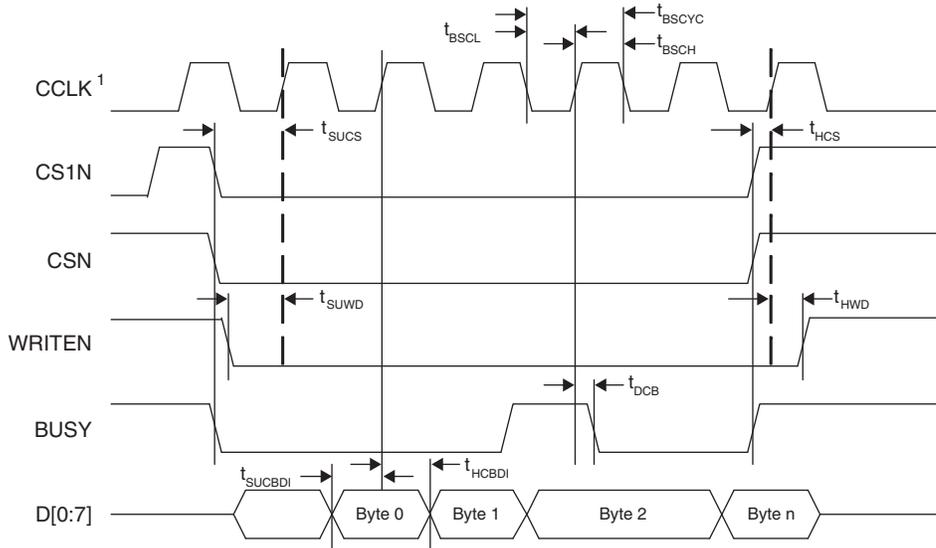


Figure 3-21. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3-22. sysCONFIG Master Serial Port Timing

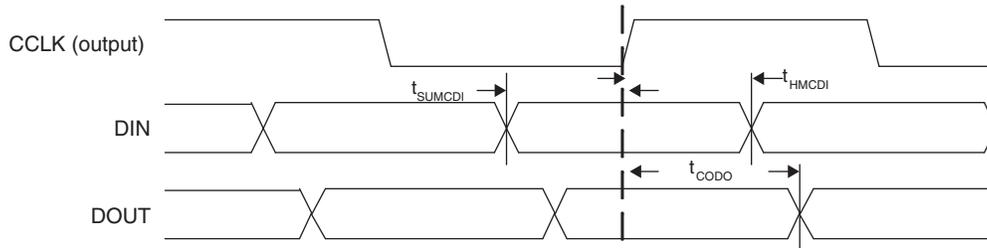
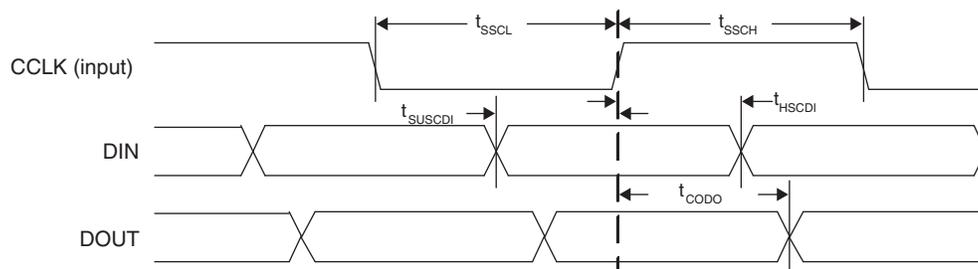


Figure 3-23. sysCONFIG Slave Serial Port Timing



Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43
	Bank 1	18	24	39
	Bank 2	8	12	13
	Bank 3	20	23	33
	Bank 6	22	25	33
	Bank 7	11	16	18
	Bank 8	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0
	Bank 1	0	0	0
	Bank 2	6	9	9
	Bank 3	9	12	16
	Bank 6	11	14	16
	Bank 7	9	12	13
	Bank 8	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49
	Bank 6	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12
DDR Groups Bonded per Bank ¹	Bank 0	3	5	7
	Bank 1	3	4	7
	Bank 2	2	3	3
	Bank 3	3	4	5
	Bank 6	4	4	5
	Bank 7	3	4	4
	Configuration Bank 8	0	0	0
SERDES Quads		1	2	3

1. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per bank	Bank 0	42	60	86	60	94
	Bank 1	36	48	78	48	86
	Bank 2	24	34	36	34	58
	Bank 3	54	59	86	59	104
	Bank 6	63	67	86	67	104
	Bank 7	36	48	54	48	76
	Bank 8	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	4	8	8	8	8
	Bank 3	4	12	12	12	12
	Bank 6	4	12	12	12	12
	Bank 7	4	8	8	8	8
	Bank 8	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	0	0	0	0	0
	Bank 3	0	0	0	0	0
	Bank 6	0	0	0	0	0
	Bank 7	0	0	0	0	0
	Bank 8	0	0	0	0	0
Total Single-Ended User I/O		295	380	490	380	586
VCC		16	32	32	32	32
VCCAUX		8	12	16	12	16
VTT		4	4	8	4	8
VCCA		4	8	16	8	16
VCCPLL		4	4	4	4	4
VCCIO	Bank 0	2	4	4	4	4
	Bank 1	2	4	4	4	4
	Bank 2	2	4	4	4	4
	Bank 3	2	4	4	4	4
	Bank 6	2	4	4	4	4
	Bank 7	2	4	4	4	4
	Bank 8	2	2	2	2	2
VCCJ		1	1	1	1	1
TAP		4	4	4	4	4
GND, GNDIO		98	139	233	139	233
NC		0	0	238	0	116
Reserved ¹		2	2	2	2	2
SERDES		26	52	78	52	104
Miscellaneous Pins		8	8	8	8	8
Total Bonded Pins		484	672	1156	672	1156

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*spFNpkgCTW* and LFE3-150EA-*spFNpkgITW* devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*spFNpkgC* and LFE3-150EA-*spFNpkgI* devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250V.