E. Lattice Semiconductor Corporation - LFE3-17EA-8LFTN256I Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-8lftn256i

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LatticeECP3 Family Data Sheet Introduction

February 2012

Features

- Higher Logic Density for Increased System Integration
 - 17K to 149K LUTs
 - 116 to 586 I/Os
- Embedded SERDES
 - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
 - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
 - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

■ sysDSP[™]

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
 - -Half 36x36, two 18x18 or four 9x9 multipliers
 - Advanced 18x36 MAC and 18x18 Multiply-
 - Multiply-Accumulate (MMAC) operations

■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM[™] Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
 Two DLLs and up to ten PLLs per device
- Pre-Engineered Source Synchronous I/O
 - DDR registers in I/O cells

Table 1-1. LatticeECP3™ Family Selection Guide

• Dedicated read/write levelling functionality

Data Sheet DS1021

- Dedicated gearing logic
- Source synchronous standards support
 ADC/DAC, 7:1 LVDS, XGMII
 Link Speed ADC/DAC devices
 - -High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- Programmable sysl/O[™] Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - Optional equalization filter on inputs
 - LVTTL and LVCMOS 33/25/18/15/12
 - SSTL 33/25/18/15 I, II
 - HSTL15 I and HSTL18 I, II
 - PCI and Differential HSTL, SSTL
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- · On-chip oscillator for initialization & general use
- 1.2 V core power supply

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2/2	4/2	10/2	10 / 2	10/2
Packages and SERDES Channels	/ I/O Combinatio	ns		•	
328 csBGA (10 x 10 mm)	2/116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

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Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM



Figure 2-4. General Purpose PLL Diagram



Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	0	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	0	PLL output to clock tree (no phase shift)
CLKOK	0	PLL output to clock tree through secondary clock divider
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)
LOCK	0	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay



Figure 2-8. Clock Divider Connections



Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.



Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.



Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)



Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143 ¹ , 177 ¹ , 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3 ²	155.52	x1	N/A
SONET-STS-12 ²	622.08	x1	N/A
SONET-STS-48 ²	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.

2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.



Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
IDK_HS⁴	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)		_	+/—1	mA
IDK⁵	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$		_	+/—1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5V$	_	18		mA

1. $V_{CC},\,V_{CCAUX}$ and V_{CCIO} should rise/fall monotonically.

2. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

3. LVCMOS and LVTTL only.

4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.

5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements^{1, 2}

Description	Min.	Тур.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	_	-	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.

2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the LatticeECP3 Product Family Qualification Summary for complete qualification data, including ESD performance.



sysl/O Recommended Operating Conditions

		V _{CCIO}		V _{REF} (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS33 ²	3.135	3.3	3.465	—	—	—
LVCMOS33D	3.135	3.3	3.465	—	—	—
LVCMOS25 ²	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12 ²	1.14	1.2	1.26	—	—	—
LVTTL33 ²	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15 ³	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ²	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ²	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_l ²	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II ²	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 ²	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 2}	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25 ^{1, 2}	2.375	2.5	2.625		—	—
RSDS ²	2.375	2.5	2.625	—	—	—
RSDSE ^{1, 2}	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D ³	1.43	1.5	1.57		—	—
SSTL18D_I ^{2, 3} , II ^{2, 3}	1.71	1.8	1.89		—	—
SSTL25D_ I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_ I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_ I ²	1.425	1.5	1.575	_	—	—
HSTL18D_ I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. For input voltage compatibility, see TN1177, LatticeECP3 sysIO Usage Guide.

3. VREF is required when using Differential SSTL to interface to DDR memory.



LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL33



Table 3-3. LVPECL33 DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z _{OUT}	Driver Impedance	10	Ω
R _S	Driver Series Resistor (+/-1%)	93	Ω
R _P	Driver Parallel Resistor (+/-1%)	196	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	2.05	V
V _{OL}	Output Low Voltage	1.25	V
V _{OD}	Output Differential Voltage	0.80	V
V _{CM}	Output Common Mode Voltage	1.65	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



Figure 3-8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)





LatticeECP3 Maximum I/O Buffer Speed ^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
Maximum Input Frequency		·	
LVDS25	LVDS, $V_{CCIO} = 2.5 V$	400	MHz
MLVDS25	MLVDS, Emulated, V _{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V _{CCIO} = 2.5 V	400	MHz
PPLVDS	Point-to-Point LVDS	400	MHz
TRLVDS	Transition-Reduced LVDS	612	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V _{CCIO} = 3.3 V	400	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, V _{CCIO} = 1.8 V	400	MHz
HSTL15	HSTL_15 class I, V _{CCIO} = 1.5 V	400	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, V _{CCIO} = 3.3 V	400	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, V _{CCIO} = 2.5 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V _{CCIO} = 1.8 V	400	MHz
LVTTL33	LVTTL, V _{CCIO} = 3.3 V	166	MHz
LVCMOS33	LVCMOS, V _{CCIO} = 3.3 V	166	MHz
LVCMOS25	LVCMOS, V _{CCIO} = 2.5 V	166	MHz
LVCMOS18	LVCMOS, V _{CCIO} = 1.8 V	166	MHz
LVCMOS15	LVCMOS 1.5, V _{CCIO} = 1.5 V	166	MHz
LVCMOS12	LVCMOS 1.2, V _{CCIO} = 1.2 V	166	MHz
PCI33	PCI, V _{CCIO} = 3.3 V	66	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz
LVDS25	LVDS, $V_{CCIO} = 2.5 V$	612	MHz
MLVDS25	MLVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz
RSDS25	RSDS, Emulated, V _{CCIO} = 2.5 V	612	MHz
BLVDS25	BLVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz
PPLVDS	Point-to-point LVDS	612	MHz
LVPECL33	LVPECL, Emulated, V _{CCIO} = 3.3 V	612	MHz
Mini-LVDS	Mini LVDS	612	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, V _{CCIO} = 1.8 V	200	MHz
HSTL15 (all supported classes)	HSTL_15 class I, V _{CCIO} = 1.5 V	200	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, V _{CCIO} = 3.3 V	233	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, V _{CCIO} = 2.5 V	233	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V _{CCIO} = 1.8 V	266	MHz
LVTTL33	LVTTL, V _{CCIO} = 3.3 V	166	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	166	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	166	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	166	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	166	MHz
LVCMOS12 (For all drives except 2 mA)	LVCMOS, V _{CCIO} = 1.2 V	166	MHz
LVCMOS12 (2 mA drive)	LVCMOS, V _{CCIO} = 1.2 V	100	MHz



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2		500	MHz
'IN	CLKFB)		Primary clock ⁴	2		420	MHz
f	Output clock frequency (CLKOP,		Edge clock	4	_	500	MHz
OUT	CLKOS)		Primary clock ⁴	4	_	420	MHz
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125	_	250	MHz
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	_	166	MHz
f _{VCO}	PLL VCO frequency			500	_	1000	MHz
f _{PFD} ³	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock ⁴	2	_	420	MHz
AC Charac	teristics					-	
t _{PA}	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t _{DT}	Output clock duty cycle (CLKOS, at 50% setting)	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
	Output clock period jitter	$f_{OUT} \ge 420 \text{ MHz}$		—	_	200	ps
t _{OPJIT} 1		420 MHz > $f_{OUT} \ge 100$ MHz		_	_	250	ps
		f _{OUT} < 100 MHz		—	_	0.025	UIPP
t _{SK}	Input clock to output clock skew when N/M = integer			_		500	ps
+ 2	Look time	2 to 25 MHz		—	_	200	us
LOCK		25 to 500 MHz		—		50	us
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			_		50	ns
t _{HI}	Input clock high time	90% to 90%		0.5	_	—	ns
t _{LO}	Input clock low time	10% to 10%		0.5	_	—	ns
t _{IPJIT}	Input clock period jitter			—	_	400	ps
+	Reset signal pulse width high, RSTK			10	_	_	ns
'RST	Reset signal pulse width high, RST			500	_	_	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.

4. When using internal feedback, maximum can be up to 500 MHz.



Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F _{REF}	Frequency range	15	_	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	_	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ²	200	_	V _{CCA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	_	mV, p-p differential	
V _{REF-IN}	Input levels	0	_	V _{CCA} + 0.3	V
D _{REF}	Duty cycle ³	40	_	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)		500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-20%	100/2K	+20%	Ohms
C _{REF-IN-CAP}	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms





Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF} ¹	Differential rise/fall time	20%-80%	—	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{3, 4, 5}	Output data deterministic jitter			_	0.17	UI
J _{TX_TJ} ^{2, 3, 4, 5}	Total output data jitter			_	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	_	_	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—		dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{2, 3, 4, 5}	Deterministic jitter tolerance (peak-to-peak)		_	—	0.37	UI
J _{RX_RJ} ^{2, 3, 4, 5}	Random jitter tolerance (peak-to-peak)		_	—	0.18	UI
J _{RX_SJ} ^{2, 3, 4, 5}	Sinusoidal jitter tolerance (peak-to-peak)		_	—	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4, 5}	Total jitter tolerance (peak-to-peak)		_	—	0.65	UI
T _{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.



Signal Descriptions (Cont.)

Signal Name	I/O	Description						
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.						
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.						
Test and Programming (Dedicated Pins)								
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.						
тск	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.						
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.						
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.						
VCCJ	—	Power supply pin for JTAG Test Access Port.						
Configuration Pads (Used During sys	CONFIG	G)						
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.						
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.						
PROGRAMN	Ι	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.						
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.						
ССГК	Ι	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.						
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.						
BUSY/SISPI	0	Parallel configuration mode busy indicator. SPI/SPIm mode data output.						
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.						
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.						
WRITEN	Ι	Write enable for parallel configuration modes.						
DOUT/CSON/CSSPI1N	0	Serial data output. Chip select output. SPI/SPIm mode chip select.						
		sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration.						
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.						
D1	I/O	Parallel configuration I/O. Open drain during configuration.						
D2	I/O	Parallel configuration I/O. Open drain during configuration.						
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configura- tion.						
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configura- tion.						
D5	I/O	Parallel configuration I/O. Open drain during configuration.						
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.						



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW1	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.



Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t _{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t _{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t _{PFD} .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Out- put Jitter, Typical Building Block Function Performance, Register-to- Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	_	Initial release.