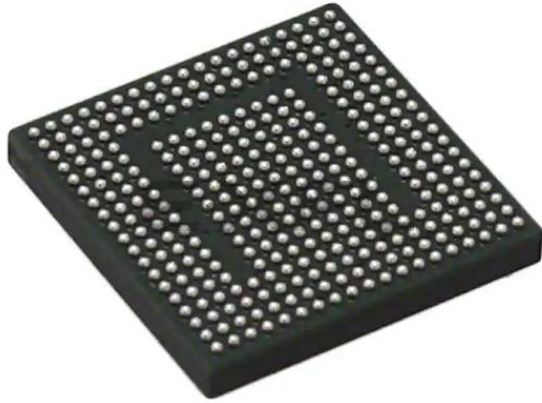




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	116
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	328-LFBGA, CSBGA
Supplier Device Package	328-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-17ea-8mg328i

Features

■ Higher Logic Density for Increased System Integration

- 17K to 149K LUTs
- 116 to 586 I/Os

■ Embedded SERDES

- 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
- Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
- Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

■ sysDSP™

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
 - Half 36x36, two 18x18 or four 9x9 multipliers
 - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations

■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM

■ sysCLOCK Analog PLLs and DLLs

- Two DLLs and up to ten PLLs per device

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells

- Dedicated read/write levelling functionality
- Dedicated gearing logic
- Source synchronous standards support
 - ADC/DAC, 7:1 LVDS, XGMII
 - High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs

■ Programmable sysI/O™ Buffer Supports Wide Range of Interfaces

- On-chip termination
- Optional equalization filter on inputs
- LVTTL and LVCMOS 33/25/18/15/12
- SSTL 33/25/18/15 I, II
- HSTL15 I and HSTL18 I, II
- PCI and Differential HSTL, SSTL
- LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

■ Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

■ System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- On-chip oscillator for initialization & general use
- 1.2 V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

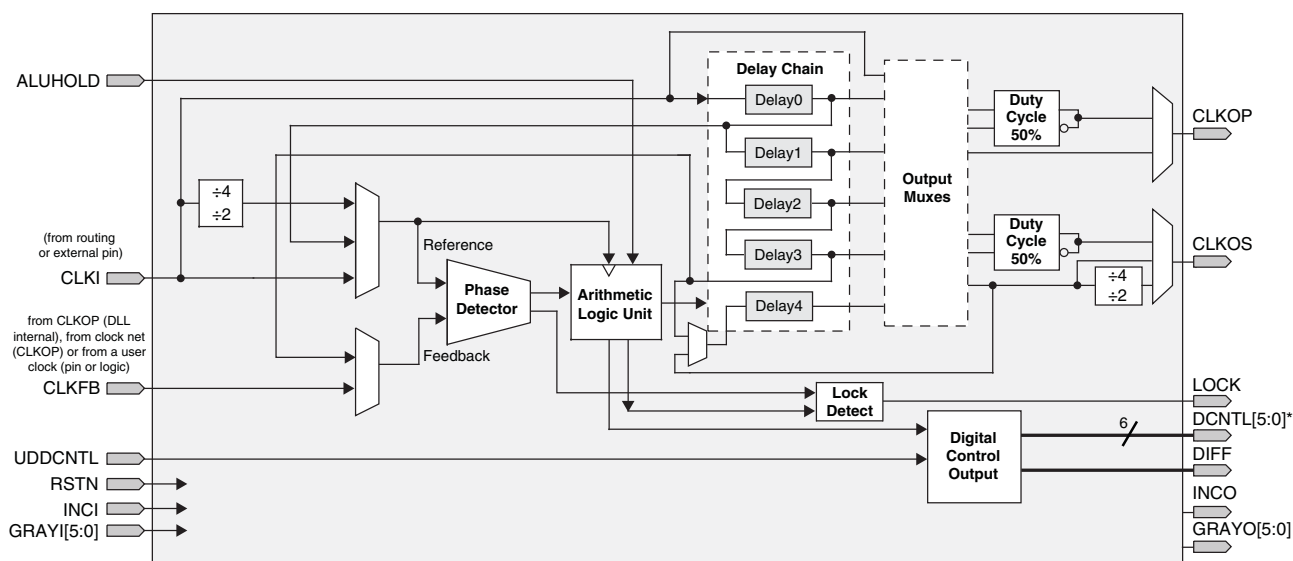
Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)



* This signal is not user accessible. This can only be used to feed the slave delay line.

The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, please see TN1179, [LatticeECP3 Memory Usage Guide](#).

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

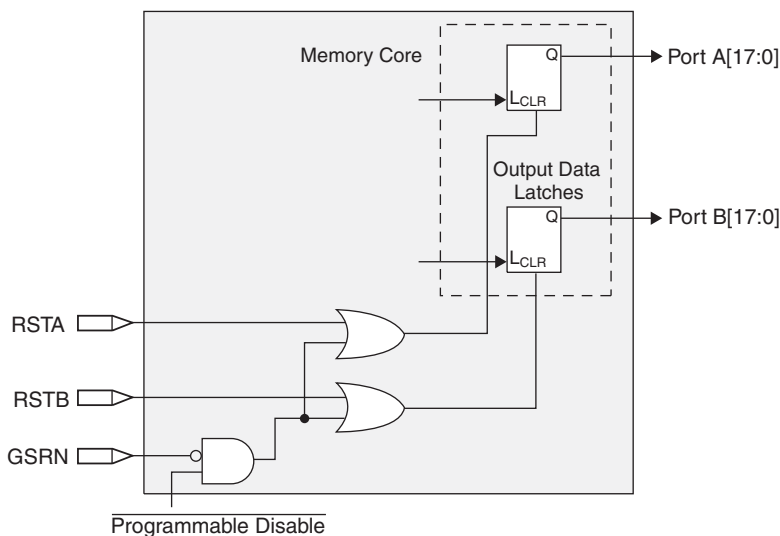
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-30 provides further information on the use of the gearbox function.

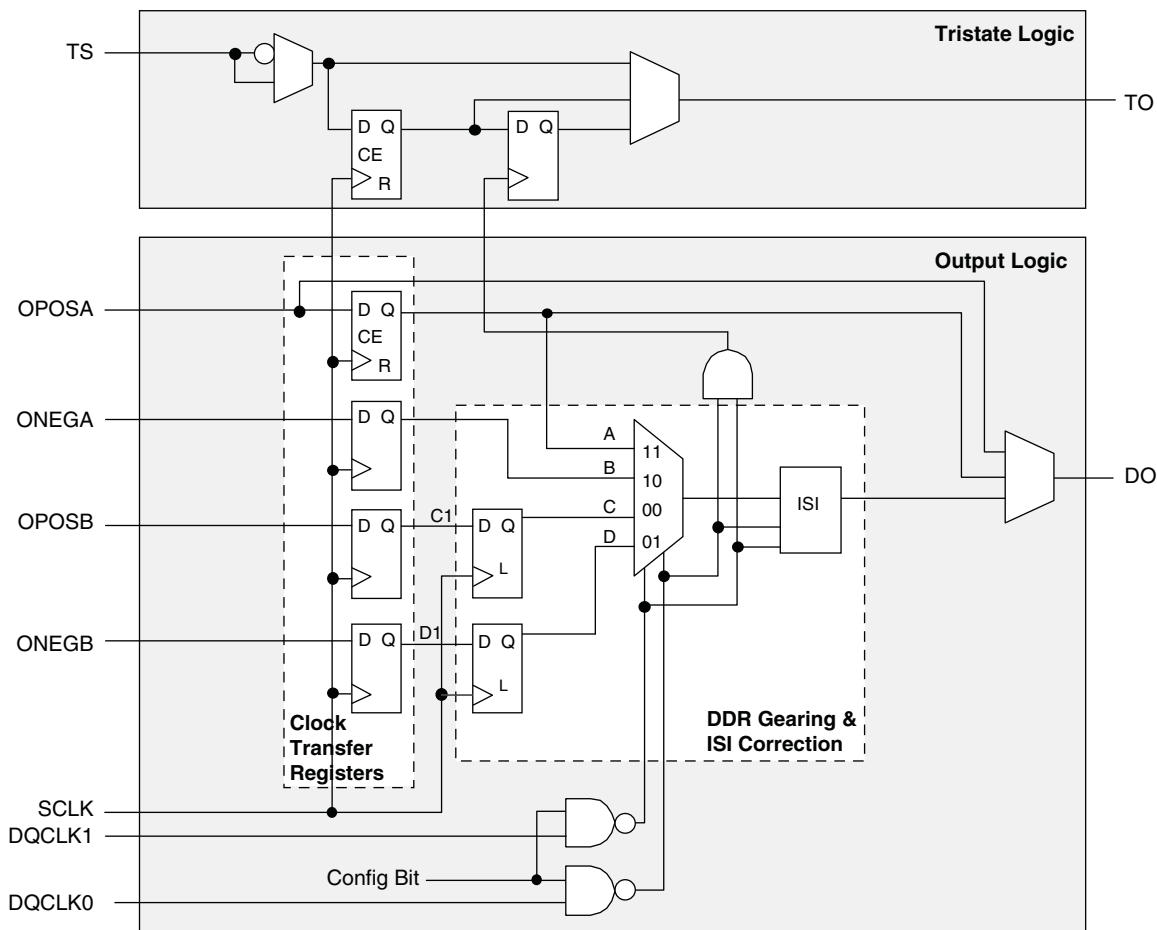
The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-37 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, [LatticeECP3 High-Speed I/O Interface](#) for more information on this topic.

Figure 2-34. Output and Tristate Block for Left and Right Edges



Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

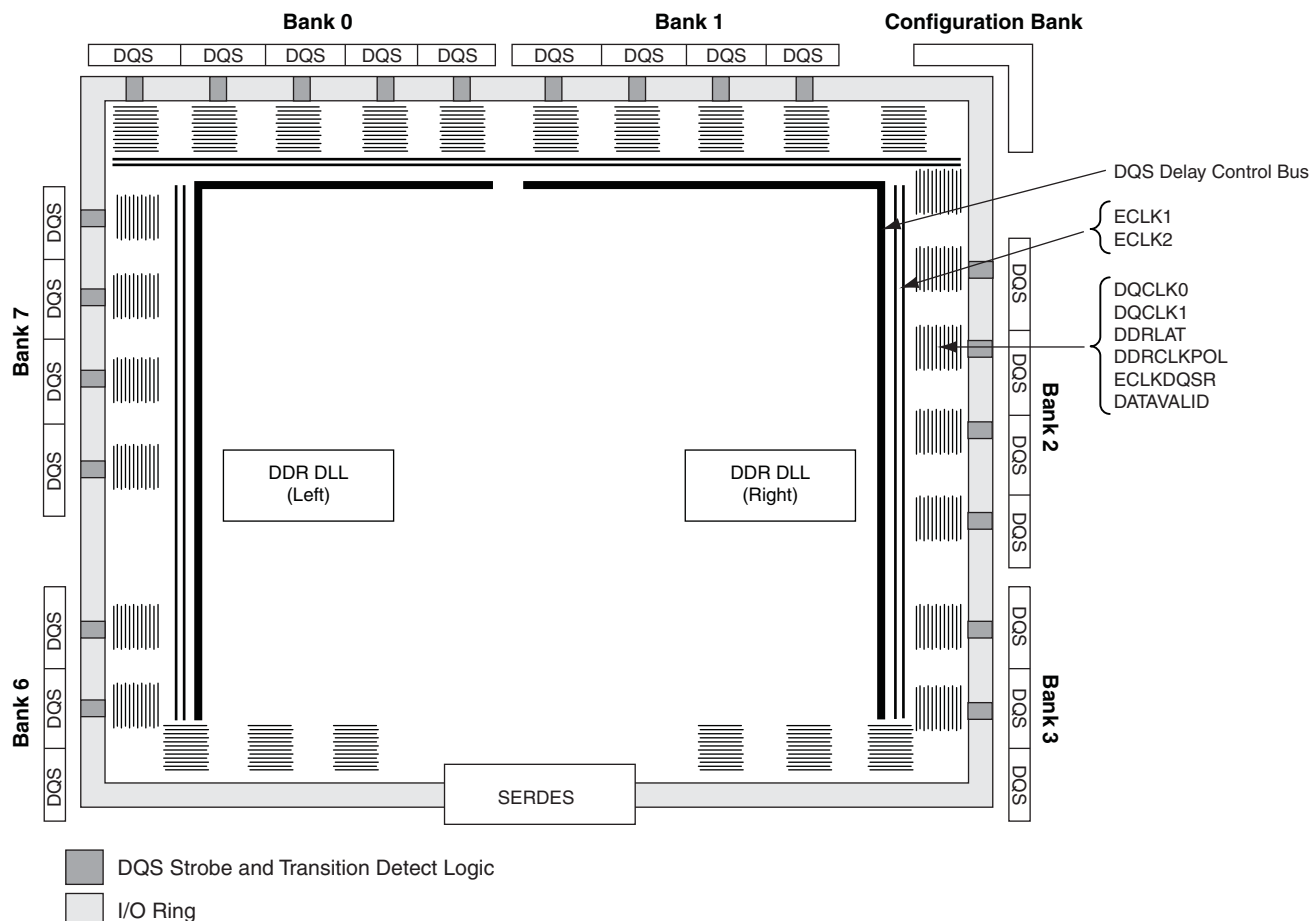
ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



*Includes shared configuration I/Os and dedicated configuration I/Os.

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, [LatticeECP3 sysCONFIG Usage Guide](#).

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, [LatticeECP3 sysCONFIG Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

1. JTAG
2. Standard Serial Peripheral Interface (SPI and SPI_{MEM} modes) - interface to boot PROM memory
3. System microprocessor to drive a x8 CPU port (PCM mode)
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Generic byte wide flash with a MachXO™ device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC}	-0.5 V to 1.32 V
Supply Voltage V_{CCAUX}	-0.5 V to 3.75 V
Supply Voltage V_{CCJ}	-0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	-0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied ⁴ . . .	-0.5 V to 3.75 V
Storage Temperature (Ambient)	-65 V to 150 °C
Junction Temperature (T_J)	+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^2	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^{2, 4}$	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
$V_{CCIO}^{2, 3}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^2	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}^5	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply⁶				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/ μ s during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.

sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS33 ²	3.135	3.3	3.465	—	—	—
LVC MOS33D	3.135	3.3	3.465	—	—	—
LVC MOS25 ²	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ²	1.14	1.2	1.26	—	—	—
LV TTL33 ²	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15 ³	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ²	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ²	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I ²	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II ²	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 ²	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 2}	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
RSDS ²	2.375	2.5	2.625	—	—	—
RSDSE ^{1, 2}	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D ³	1.43	1.5	1.57	—	—	—
SSTL18D_I ^{2, 3} , II ^{2, 3}	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. For input voltage compatibility, see TN1177, [LatticeECP3 sysIO Usage Guide](#).

3. VREF is required when using Differential SSTL to interface to DDR memory.

LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL33

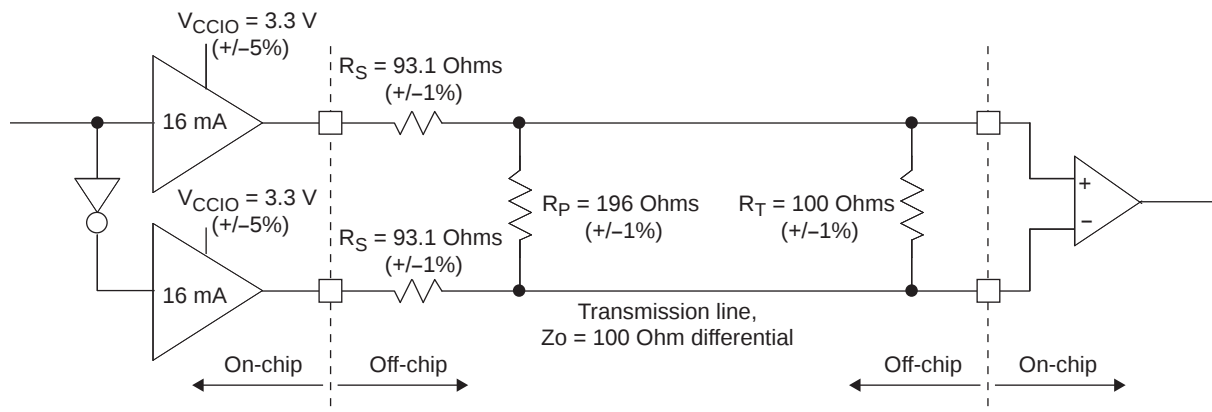


Table 3-3. LVPECL33 DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDR2_RX.ECLK.Aligned) (No CLKDIV)									
Left and Right Sides Using DLLCLKPIN for Clock Input									
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
t _{DVACLGDDR}	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
t _{DVACLGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR2_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left and Right Sides									
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f _{MAX_GDDR}	DDR2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDR2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
t _{DVACLGDDR}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDR2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDR1_TX.SCLK.Centered) ¹⁰									
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDR1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—	—	0.24	UI, p-p

Note: Values are measured with PRBS 2^7-1 , all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance ¹	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock ²	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2 \cdot V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCA} + 0.3$	V
D_{REF}	Duty cycle ³	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms

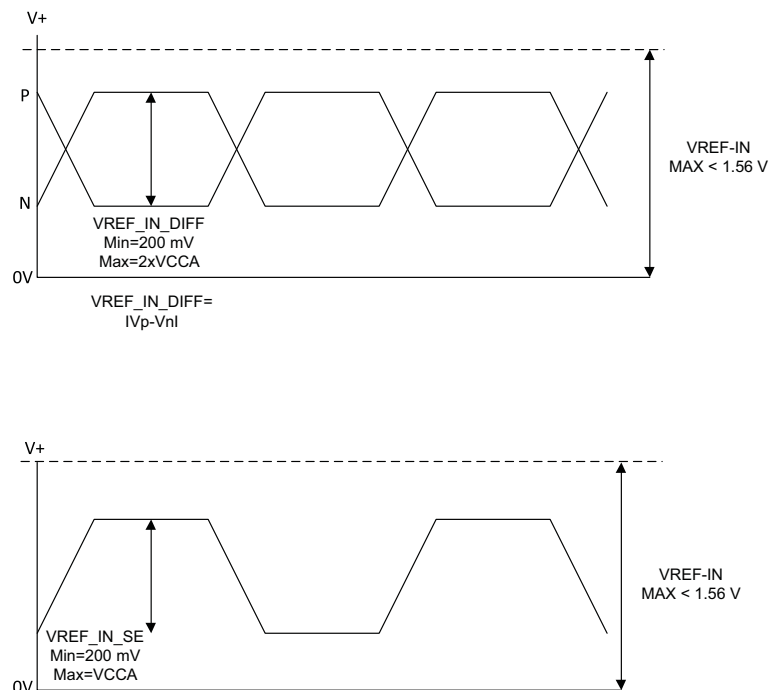
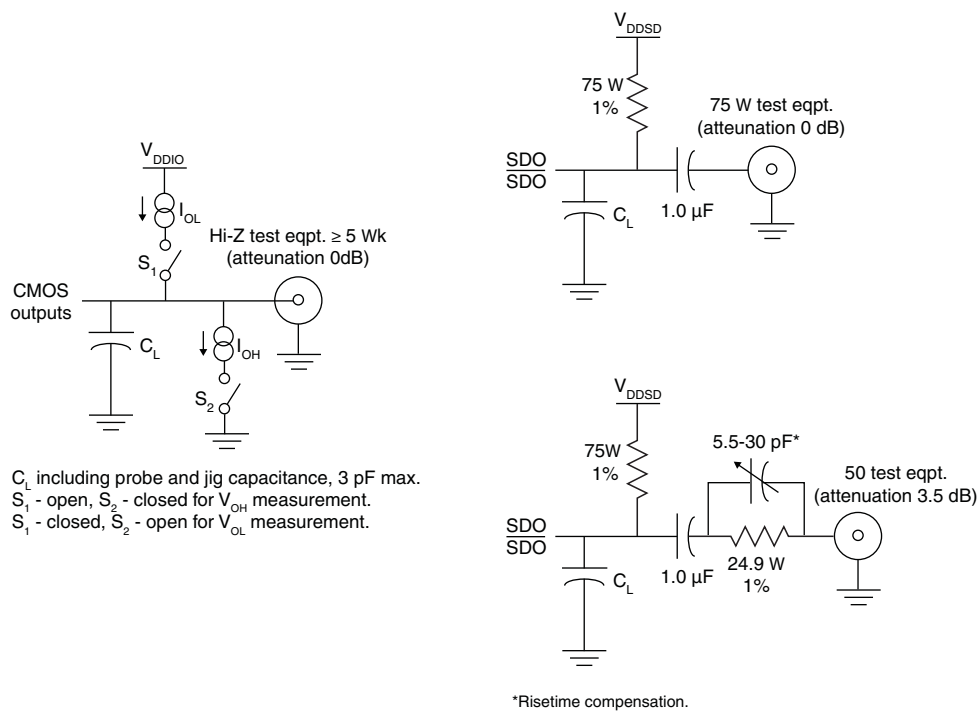
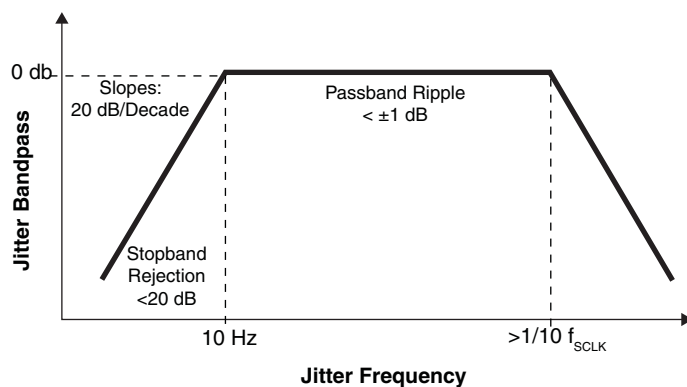


Figure 3-19. Test Loads

Test Loads



Timing Jitter Bandpass



LatticeECP3 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description		Min.	Max.	Units
POR, Configuration Initialization, and Wakeup					
t _{ICFG}	Time from the Application of V _{CC} , V _{CCAUX} or V _{CCIO8} * (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Master mode	—	23	ms
		Slave mode	—	6	ms
t _{VMC}	Time from t _{ICFG} to the Valid Master MCLK		—	5	μs
t _{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low		—	37	ns
t _{DINIT} ¹	PROGRAMN High to INITN High Delay		—	1	ms
t _{MWC}	Additional Wake Master Clock Signals After DONE Pin is High		100	500	cycles
t _{CZ}	MCLK From Active To Low To High-Z		—	300	ns
t _{IODISS}	User I/O Disable from PROGRAMN Low		—	100	ns
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence		—	100	ns
All Configuration Modes					
t _{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t _{HCDI}	Data Hold Time to CCLK/MCLK		1	—	ns
t _{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Serial					
t _{SSCH}	CCLK Minimum High Pulse		5	—	ns
t _{SSCL}	CCLK Minimum Low Pulse		5	—	ns
f _{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave Parallel					
t _{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t _{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t _{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	—	ns
t _{HWD}	WRITEN Hold Time to CCLK/MCLK		1	—	ns
t _{DCB}	CCLK/MCLK to BUSY Delay Time		—	12	ns
t _{CORD}	CCLK to Out for Read Data		—	12	ns
t _{BSCH}	CCLK Minimum High Pulse		6	—	ns
t _{BSCL}	CCLK Minimum Low Pulse		6	—	ns
t _{BSCYC}	Byte Slave Cycle Time		30	—	ns
f _{CCLK}	CCLK/MCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave SPI					
t _{CFGX}	INITN High to MCLK Low		—	80	ns
t _{CSSPI}	INITN High to CSSPIN Low		0.2	2	μs
t _{SOCDO}	MCLK Low to Output Valid		—	15	ns
t _{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		μs
f _{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
t _{SSCH}	CCLK Minimum High Pulse		5	—	ns

Figure 3-28. Master SPI Configuration Waveforms

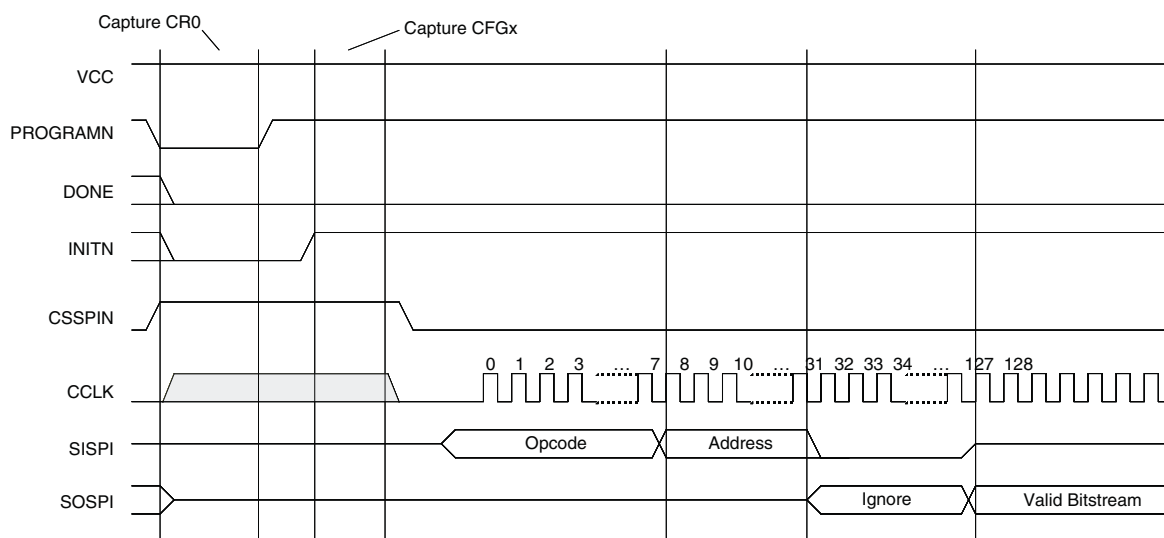
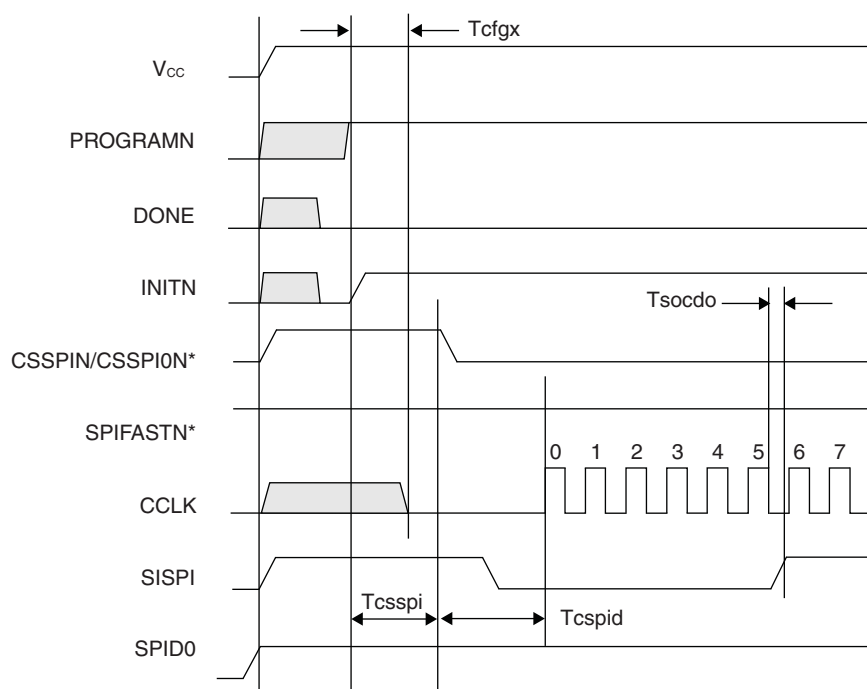


Figure 3-29. Master SPI POR Waveforms



Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per bank	Bank 0	42	60	86	60	94
	Bank 1	36	48	78	48	86
	Bank 2	24	34	36	34	58
	Bank 3	54	59	86	59	104
	Bank 6	63	67	86	67	104
	Bank 7	36	48	54	48	76
	Bank 8	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	4	8	8	8	8
	Bank 3	4	12	12	12	12
	Bank 6	4	12	12	12	12
	Bank 7	4	8	8	8	8
	Bank 8	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	0	0	0	0	0
	Bank 3	0	0	0	0	0
	Bank 6	0	0	0	0	0
	Bank 7	0	0	0	0	0
	Bank 8	0	0	0	0	0
Total Single-Ended User I/O		295	380	490	380	586
VCC		16	32	32	32	32
VCCAUX		8	12	16	12	16
VTT		4	4	8	4	8
VCCA		4	8	16	8	16
VCCPLL		4	4	4	4	4
VCCIO	Bank 0	2	4	4	4	4
	Bank 1	2	4	4	4	4
	Bank 2	2	4	4	4	4
	Bank 3	2	4	4	4	4
	Bank 6	2	4	4	4	4
	Bank 7	2	4	4	4	4
	Bank 8	2	2	2	2	2
VCCJ		1	1	1	1	1
TAP		4	4	4	4	4
GND, GNDIO		98	139	233	139	233
NC		0	0	238	0	116
Reserved ¹		2	2	2	2	2
SERDES		26	52	78	52	104
Miscellaneous Pins		8	8	8	8	8
Total Bonded Pins		484	672	1156	672	1156



LatticeECP3 Family Data Sheet

Revision History

March 2015

Data Sheet DS1021

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information All	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 . Minor style/formatting changes.
April 2014	02.7EA	DC and Switching Characteristics	Updated LatticeECP3 Supply Current (Standby) table power numbers. Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed I_{PW} to I_{PD} in footnote 3. Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching Characteristics	Updated the Wake-Up Timing Diagram Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysI/O Buffer Banks text section – Updated description of “Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)” for hot socketing information. sysI/O Buffer Banks text section – Updated description of “Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)” for PCI clamp information. On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard. sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1. Added Oscillator Output Frequency table. LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t_{CODO} parameter. LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.

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