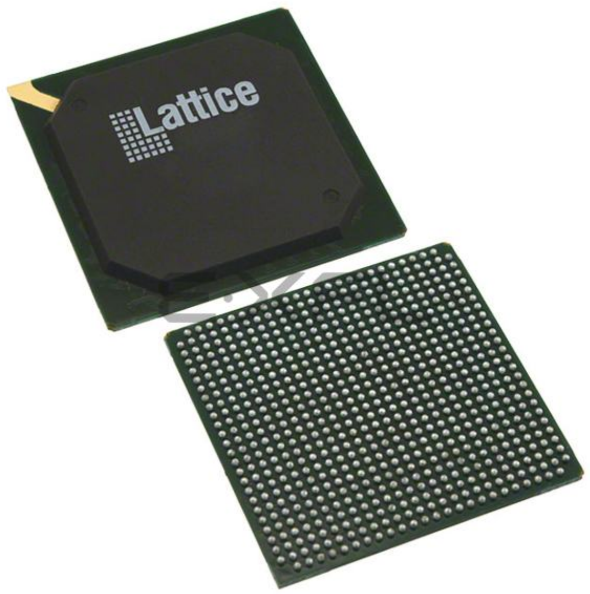
Lattice Semiconductor Corporation - LFE3-35EA-6LFN672C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	33000
Total RAM Bits	1358848
Number of I/O	310
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-6lfn672c

Figure 2-4. General Purpose PLL Diagram

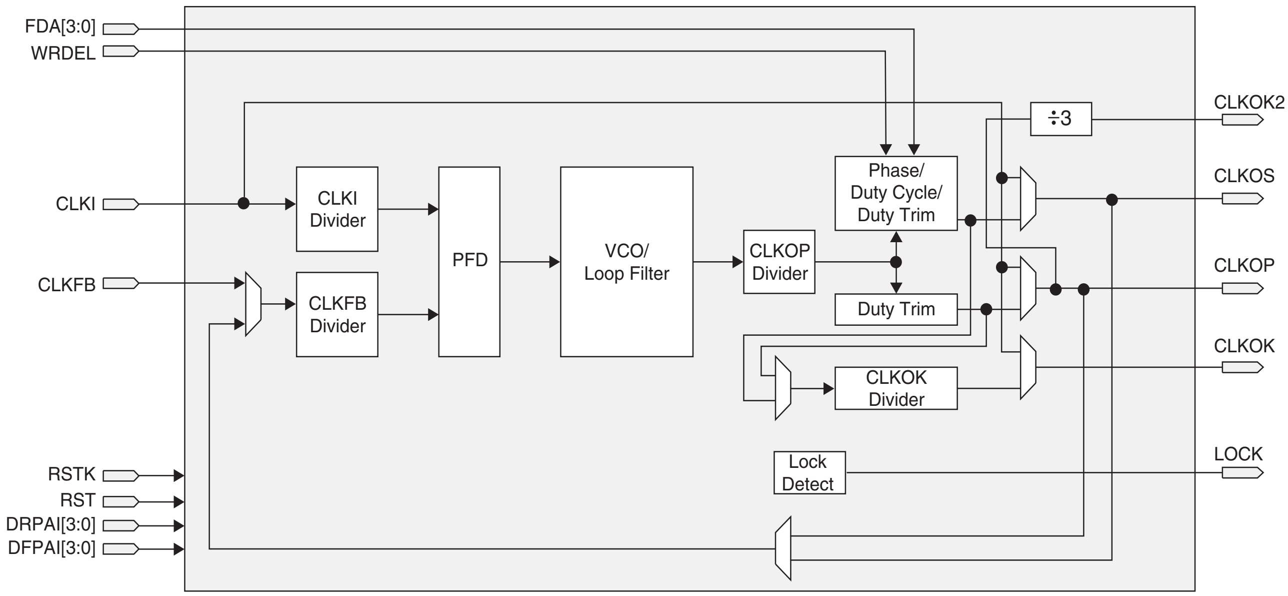


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	“1” to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	“1” to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	“1” indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

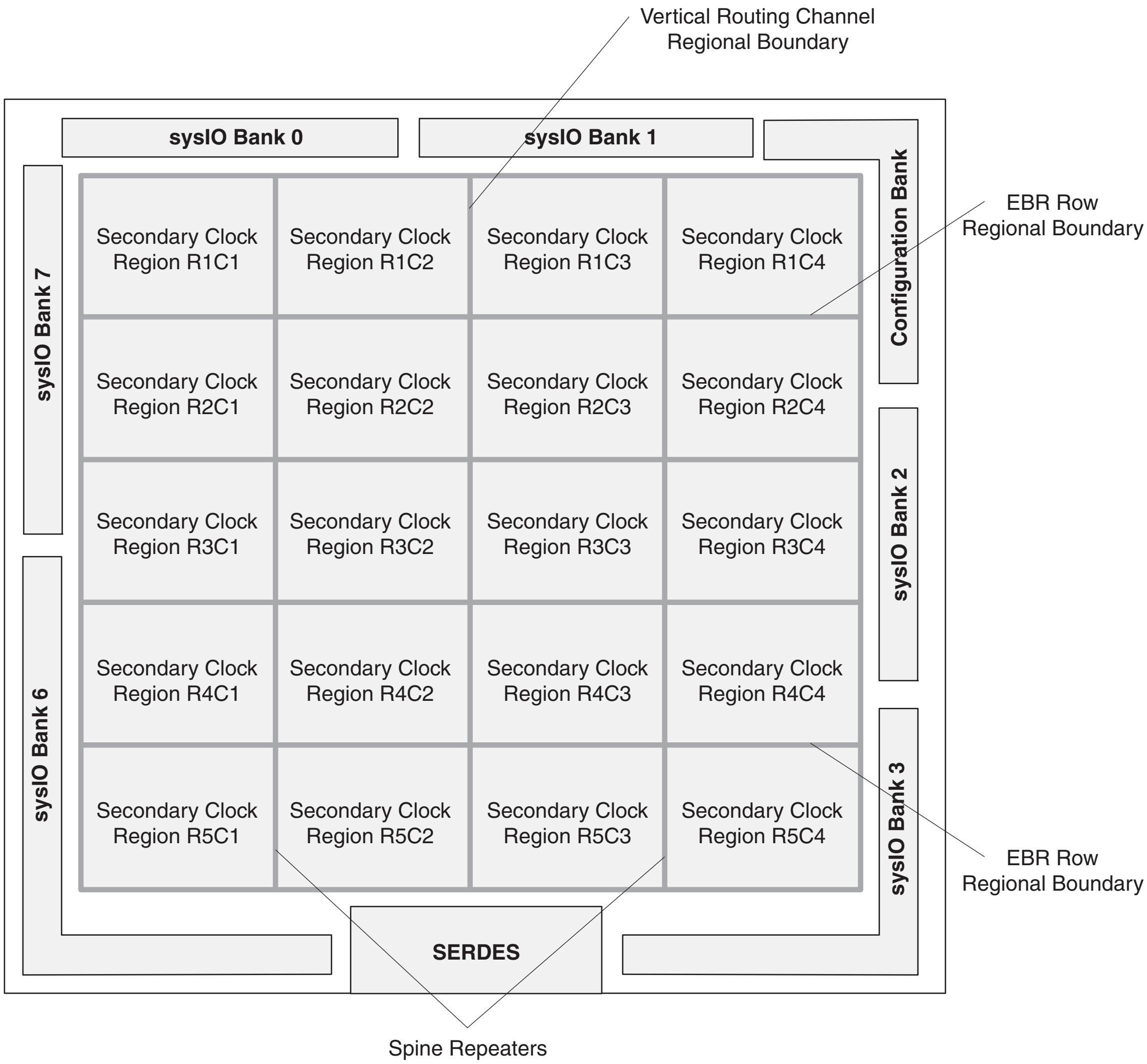
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

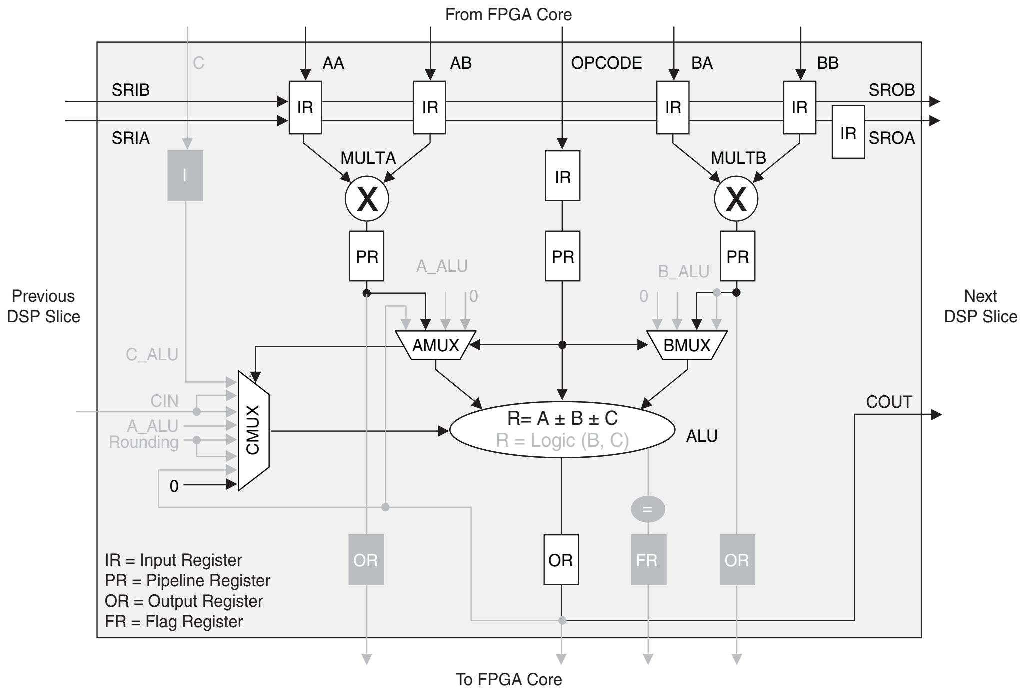
Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0



Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel ÷1, ÷2 and ÷11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.

LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical		Units
			–6L, –7L, –8L	–6, –7, –8	
I_{CC}	Core Power Supply Current	ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
		ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
		ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
I_{CCPLL}	PLL Power Supply Current (Per PLL)	ECP-17EA	0.0	0.0	mA
		ECP3-35EA	0.1	0.1	mA
		ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
		ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I_{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
I_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
		ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}[1], V_{INM}[1]	Input Voltage		0	—	2.4	V
V_{CM}[1]	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/–100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/–10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

1, On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

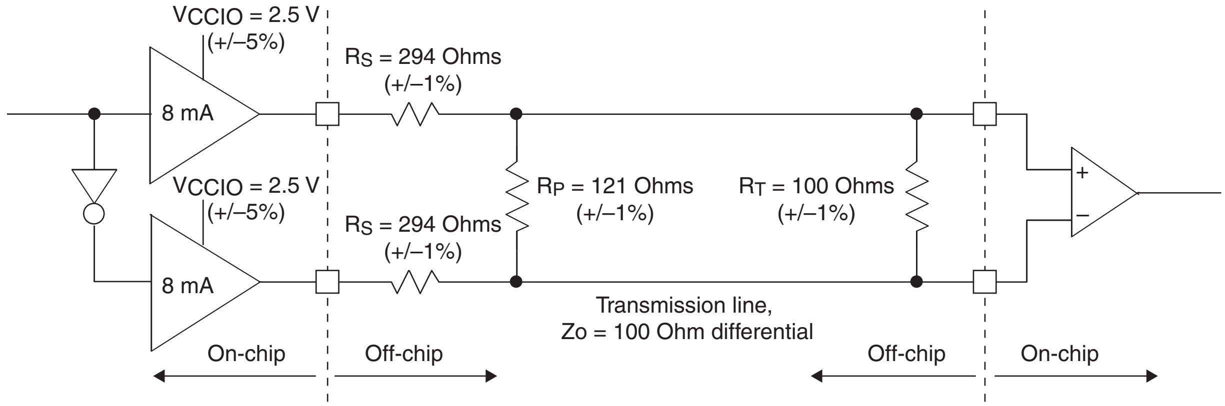


Table 3-4. RSDS25E DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	294	Ω
R_P	Driver Parallel Resistor (+/–1%)	121	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)[1, 2, 3]

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

Register-to-Register Performance[1, 2, 3]

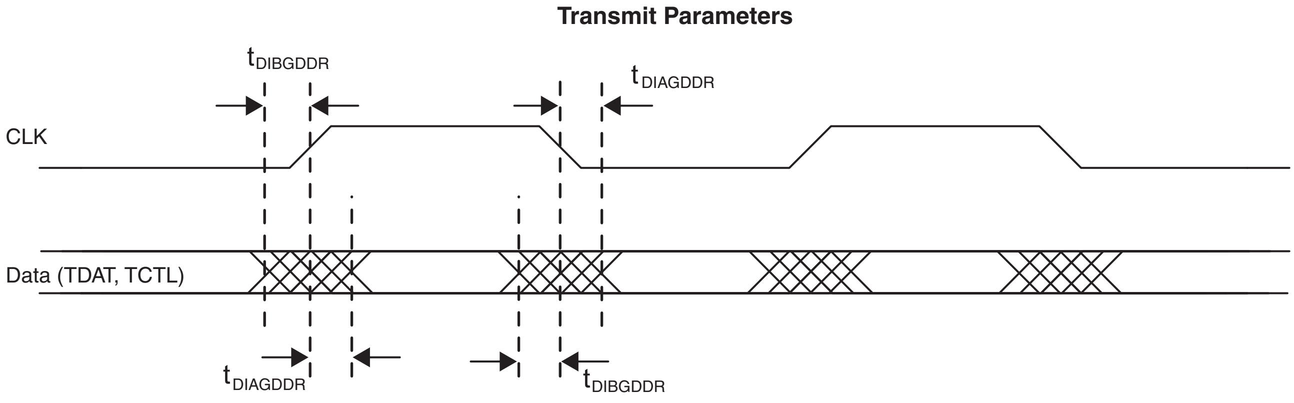
Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	500	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	400	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	260	MHz

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DVECLKGDDR}$	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA	321	—	403	—	471	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-150EA	321	—	403	—	471	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	405	—	325	—	280	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	321	—	403	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-70EA/95EA	321	—	403	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	405	—	325	—	250	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-35EA	335	—	425	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-35EA	335	—	425	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	405	—	325	—	250	MHz
t_{SUGDDR}	Data Setup Before CLK	ECP3-17EA	335	—	425	—	535	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-17EA	335	—	425	—	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	405	—	325	—	250	MHz
Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_RX.ECLK.Aligned)									
Left and Right Side Using DLLCLKIN Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz

Figure 3-6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)



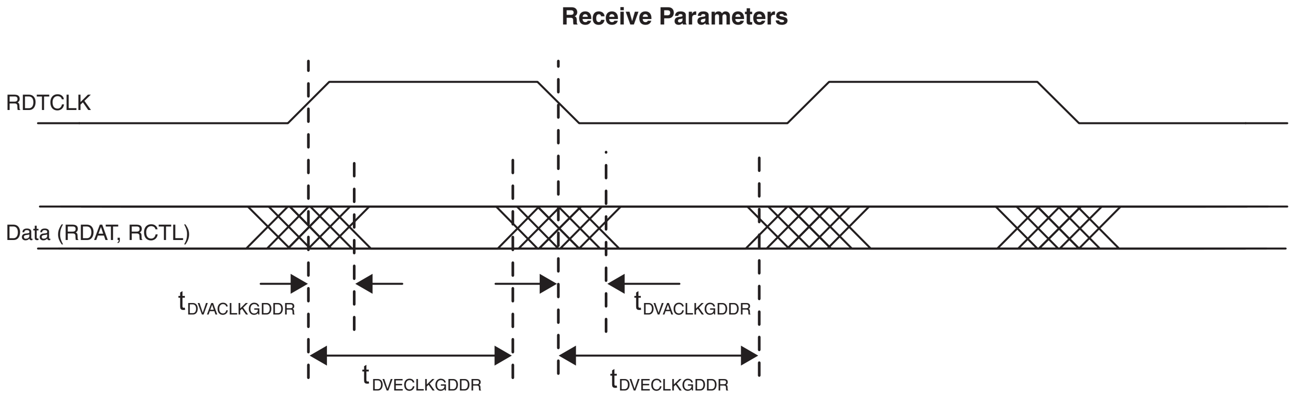
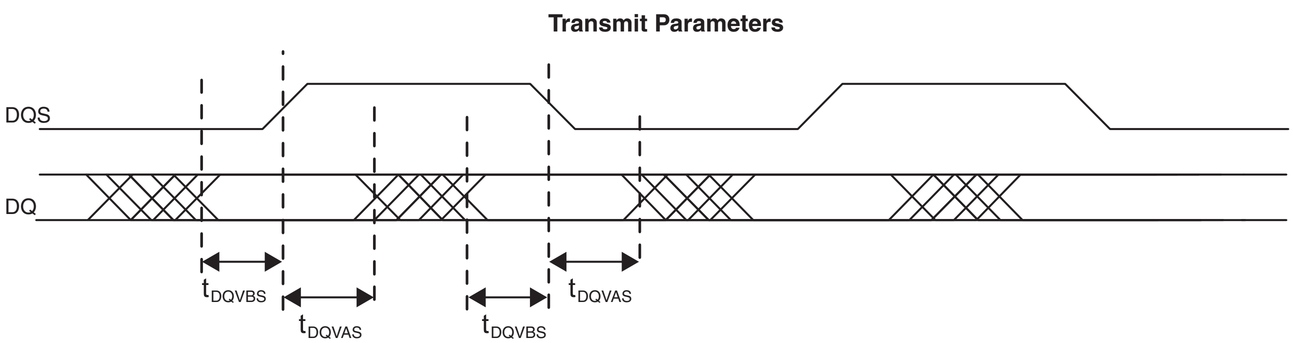
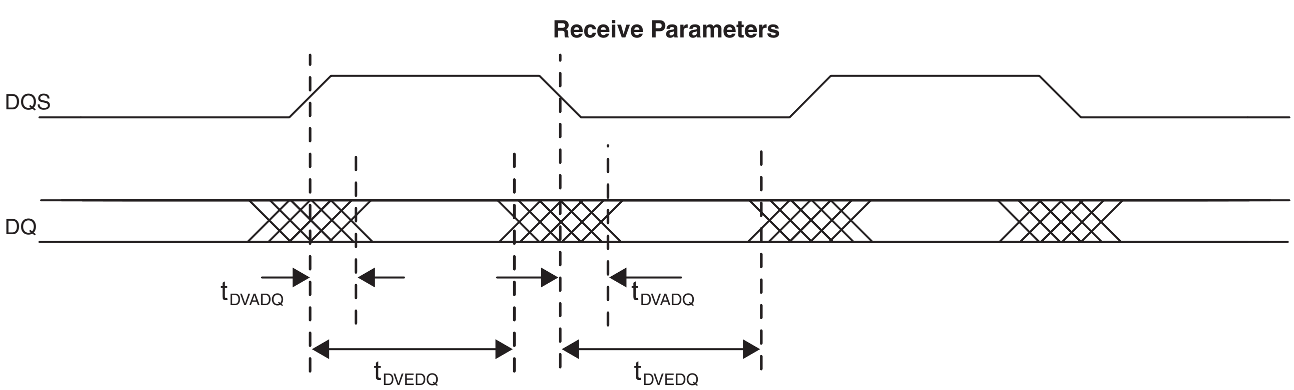


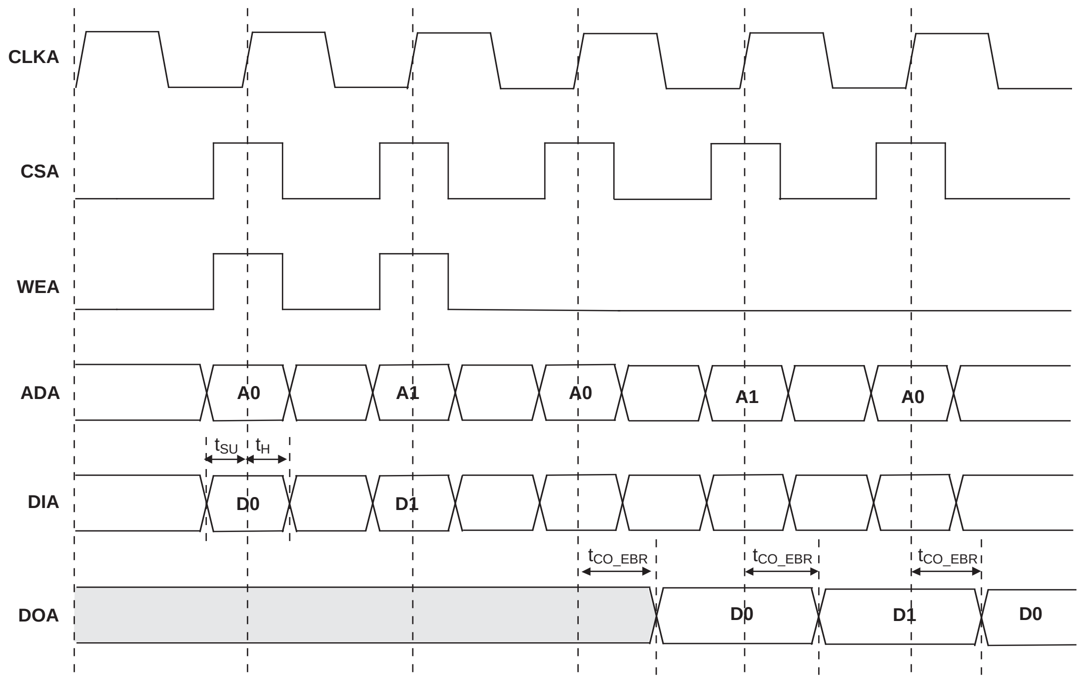
Figure 3-7. DDR/DDR2/DDR3 Parameters





Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

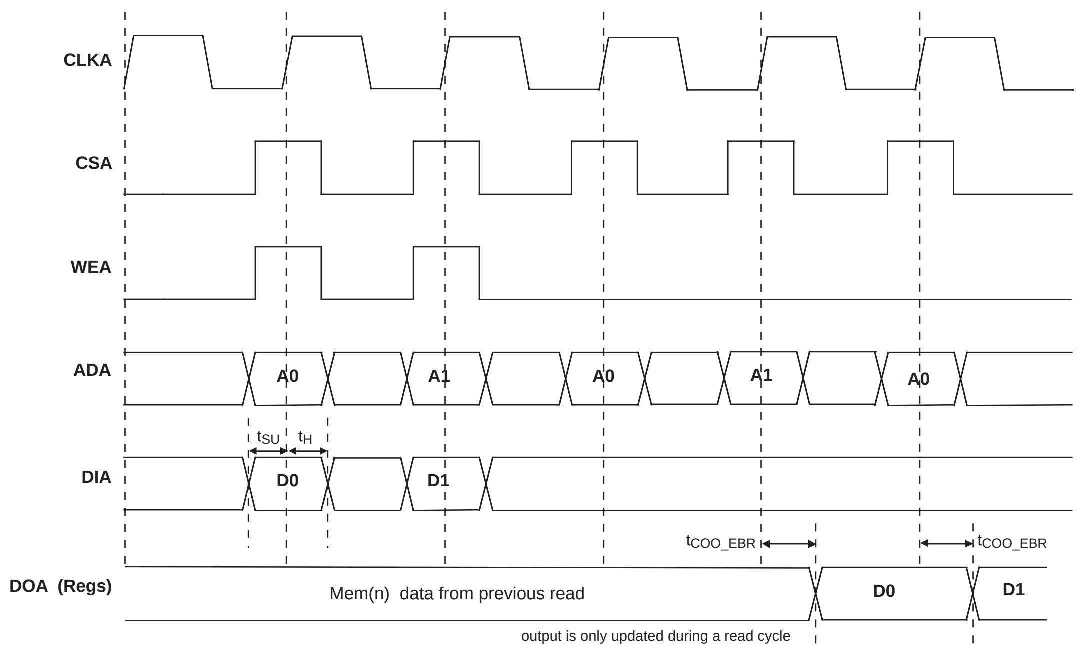


Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2^7–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-14. Jitter Transfer – 3.125 Gbps

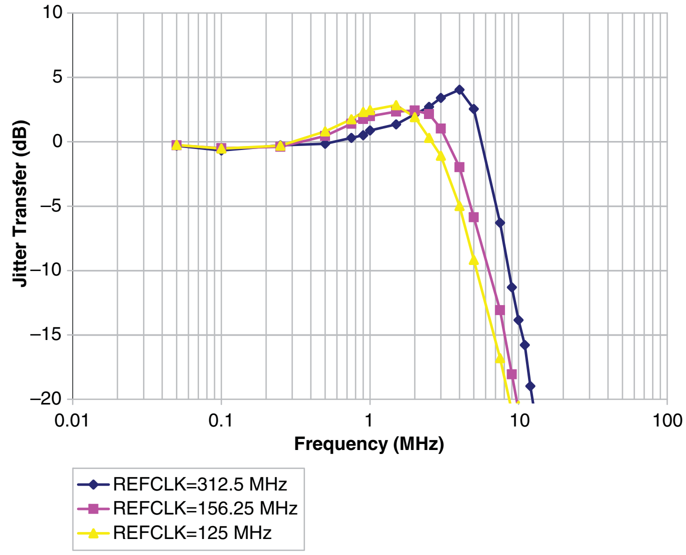
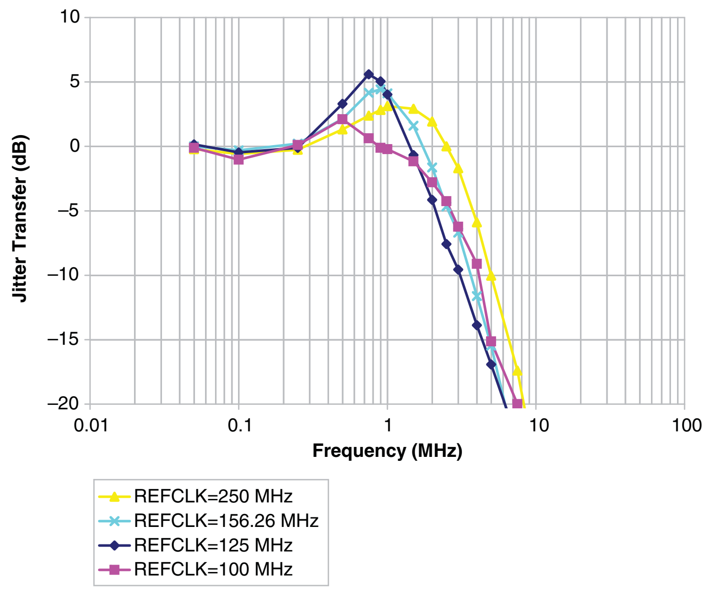


Figure 3-15. Jitter Transfer – 2.5 Gbps



XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[2, 3, 4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[1, 2, 3, 4]	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

LatticeECP3 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description		Min.	Max.	Units
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8}* (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Master mode	—	23	ms
		Slave mode	—	6	ms
t_{VMC}	Time from t_{ICFG} to the Valid Master MCLK		—	5	µs
t_{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low		—	37	ns
t_{DINIT}[1]	PROGRAMN High to INITN High Delay		—	1	ms
t_{MWC}	Additional Wake Master Clock Signals After DONE Pin is High		100	500	cycles
t_{CZ}	MCLK From Active To Low To High-Z		—	300	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low		—	100	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence		—	100	ns
All Configuration Modes					
t_{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t_{HCDI}	Data Hold Time to CCLK/MCLK		1	—	ns
t_{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Serial					
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns
t_{SSCL}	CCLK Minimum Low Pulse		5	—	ns
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave Parallel					
t_{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t_{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	—	ns
t_{HWD}	WRITEN Hold Time to CCLK/MCLK		1	—	ns
t_{DCB}	CCLK/MCLK to BUSY Delay Time		—	12	ns
t_{CORD}	CCLK to Out for Read Data		—	12	ns
t_{BSCH}	CCLK Minimum High Pulse		6	—	ns
t_{BSCL}	CCLK Minimum Low Pulse		6	—	ns
t_{BSCYC}	Byte Slave Cycle Time		30	—	ns
f_{CCLK}	CCLK/MCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave SPI					
t_{CFGX}	INITN High to MCLK Low		—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low		0.2	2	µs
t_{SOCDO}	MCLK Low to Output Valid		—	15	ns
t_{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		µs
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns

LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

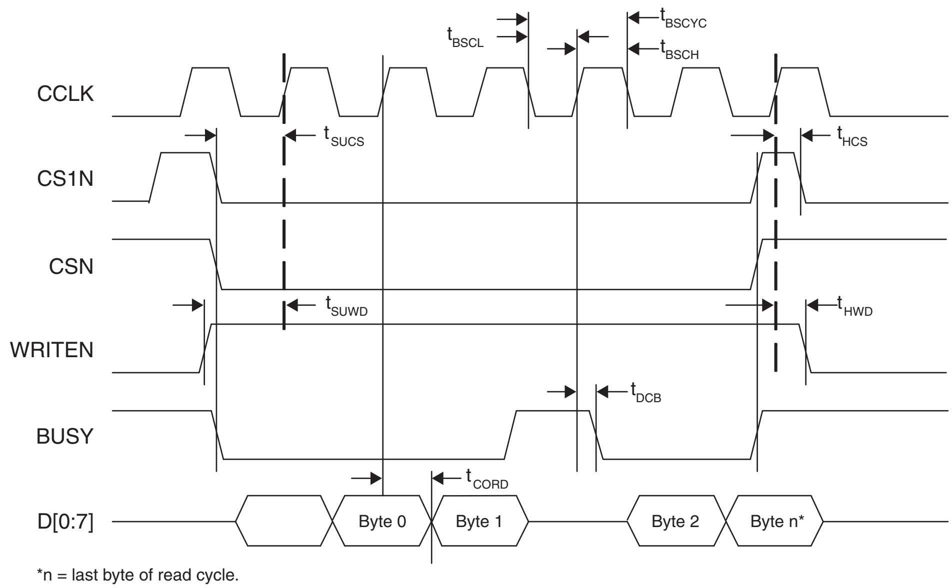
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{SSCL}	CCLK Minimum Low Pulse	5	—	ns
t_{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

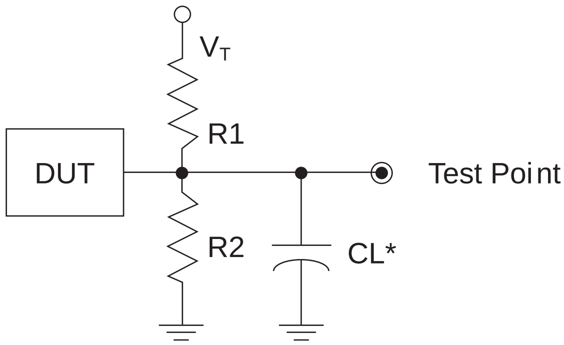
Figure 3-20. sysCONFIG Parallel Port Read Cycle



Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank[2]	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43
	Bank 1	18	24	39
	Bank 2	8	12	13
	Bank 3	20	23	33
	Bank 6	22	25	33
	Bank 7	11	16	18
	Bank 8	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0
	Bank 1	0	0	0
	Bank 2	6	9	9
	Bank 3	9	12	16
	Bank 6	11	14	16
	Bank 7	9	12	13
	Bank 8	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49
	Bank 6	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12
DDR Groups Bonded per Bank[1]	Bank 0	3	5	7
	Bank 1	3	4	7
	Bank 2	2	3	3
	Bank 3	3	4	5
	Bank 6	4	4	5
	Bank 7	3	4	4
	Configuration Bank 8	0	0	0
SERDES Quads		1	2	3

1. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

LatticeECP3 Family Data Sheet Revision History

March 2015 | Data Sheet DS1021

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3.
		All	Minor style/formatting changes.
April 2014	02.7EA	DC and Switching Characteristics	Updated LatticeECP3 Supply Current (Standby) table power numbers.
			Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed I_{PW} to I_{PD} in footnote 3.
			Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching Characteristics	Updated the Wake-Up Timing Diagram
			Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms
			Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysI/O Buffer Banks text section – Updated description of “Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)” for hot socketing information.
			sysI/O Buffer Banks text section – Updated description of “Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)” for PCI clamp information.
			On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard.
			sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1.
			Added Oscillator Output Frequency table.
			LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t_{CODO} parameter.
			LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.