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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	33000
Total RAM Bits	1358848
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-7ftn256c

LatticeECP3 Family Data Sheet Introduction

February 2012 | Data Sheet DS1021

Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

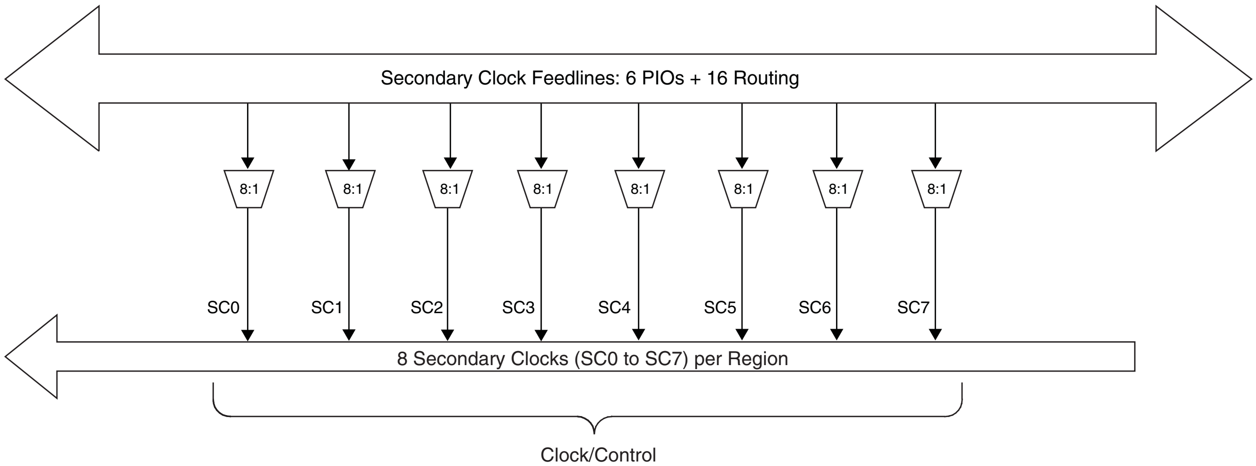
Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

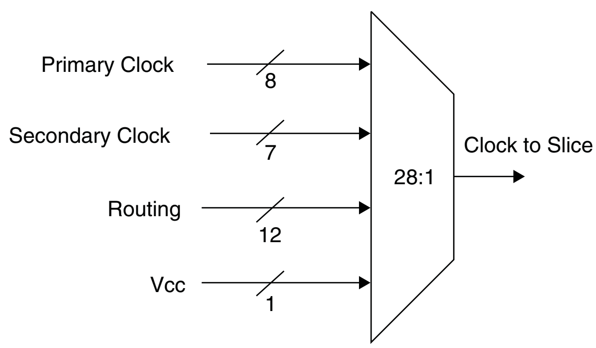
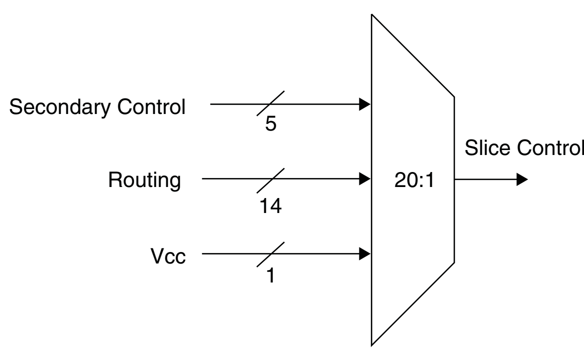
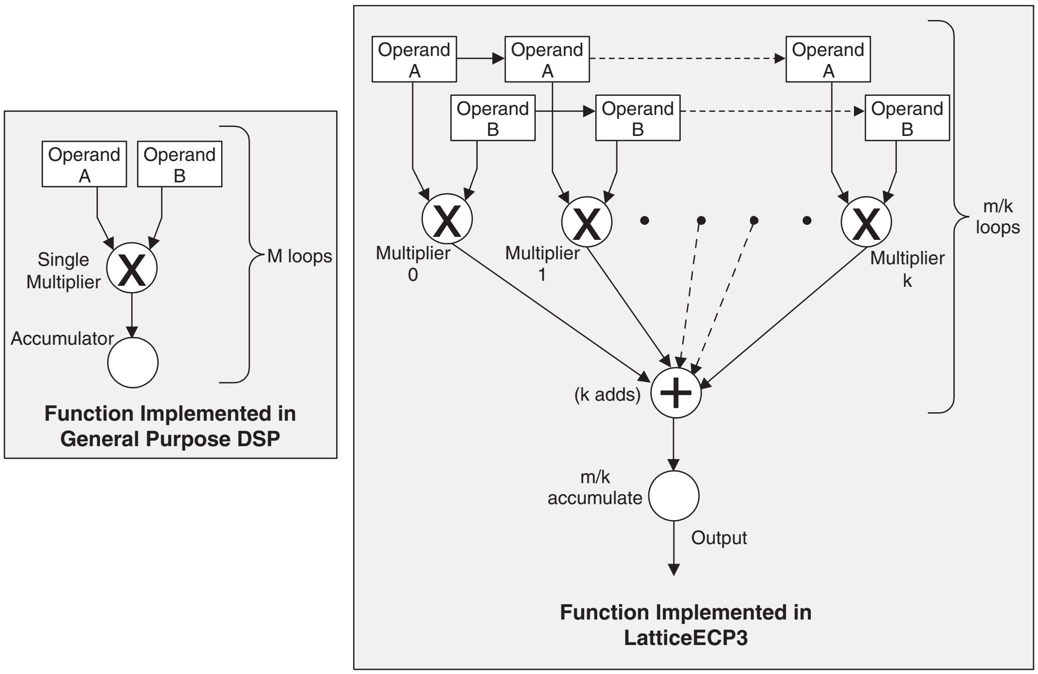


Figure 2-18. Slice0 through Slice2 Control Selection



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches



LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  — Minimizes fabric use for common DSP and ALU functions
  — Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  — Provides matching pipeline registers
  — Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  — Dynamically selectable ALU OPCODE
  — Ternary arithmetic (addition/subtraction of three inputs)
  — Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  — Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

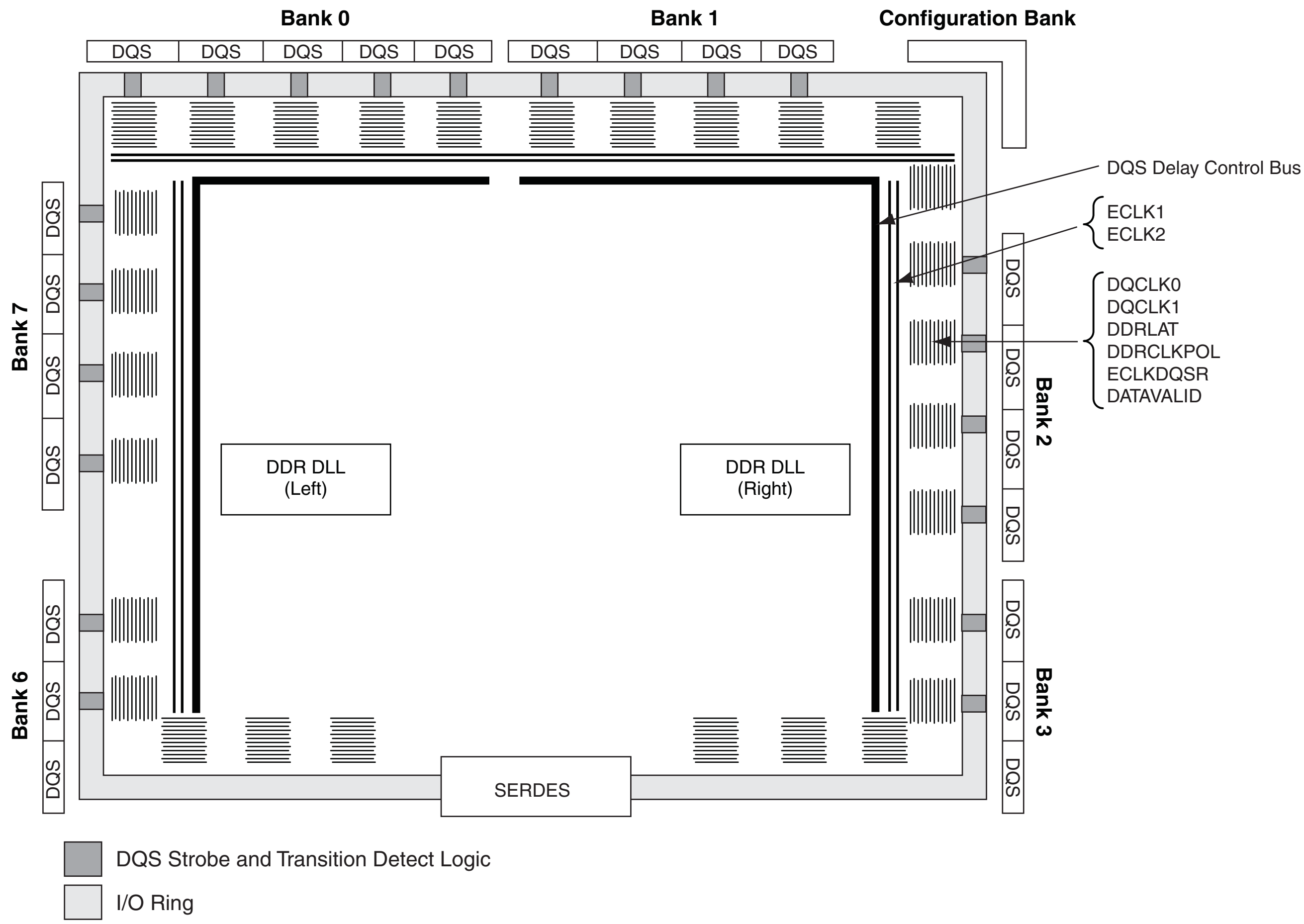
The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

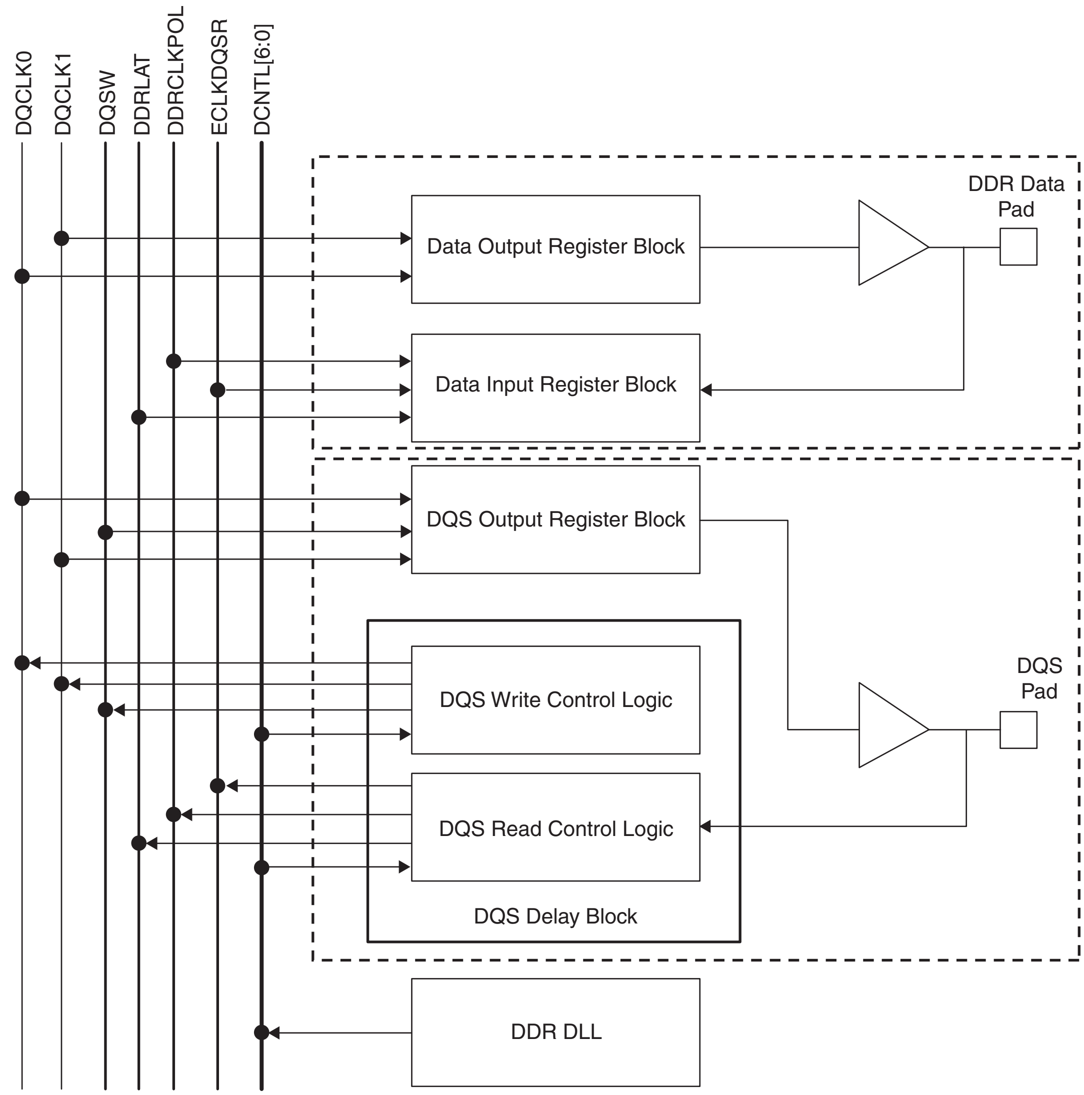
Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



*Includes shared configuration I/Os and dedicated configuration I/Os.

Figure 2-37. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

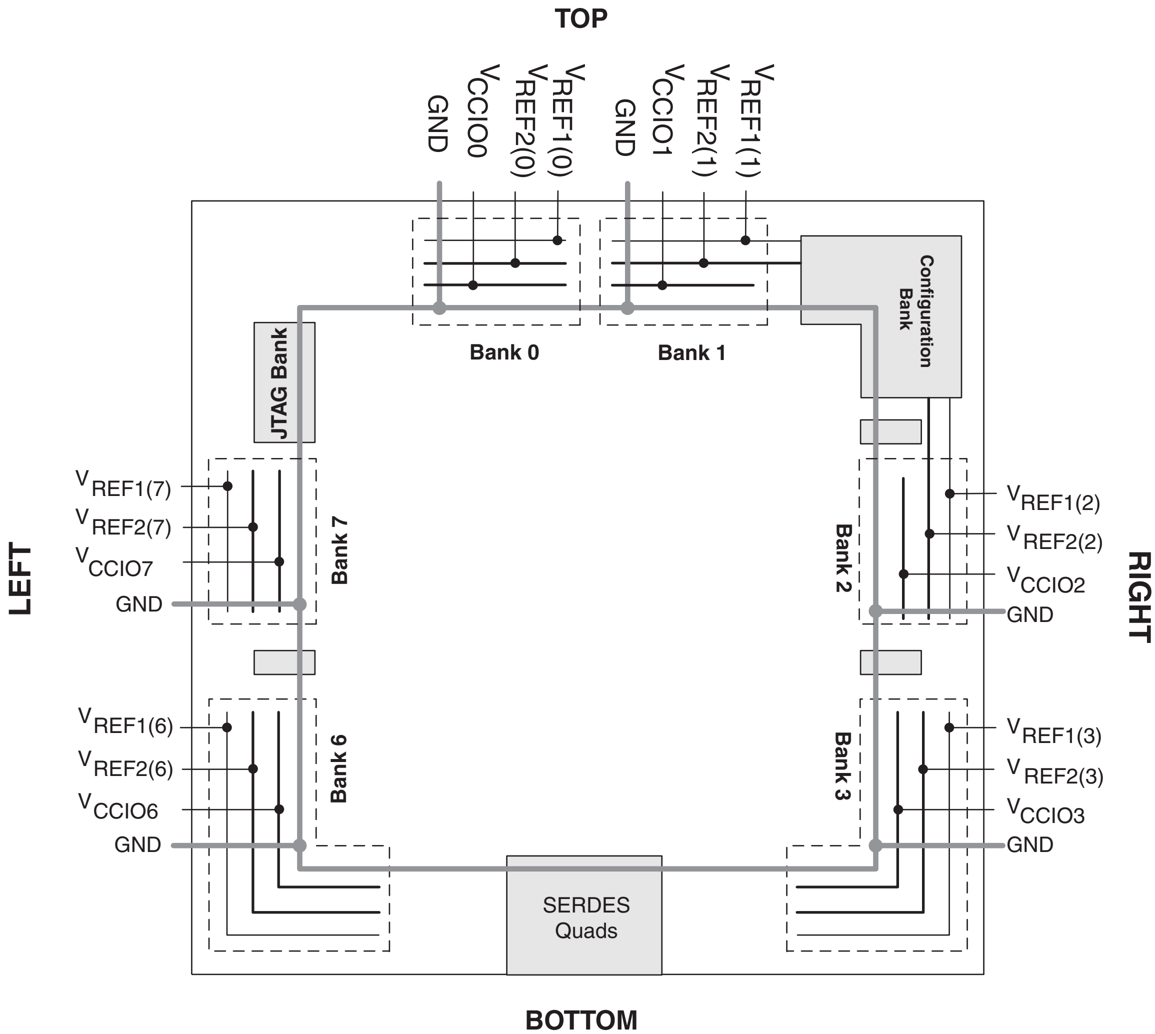
Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

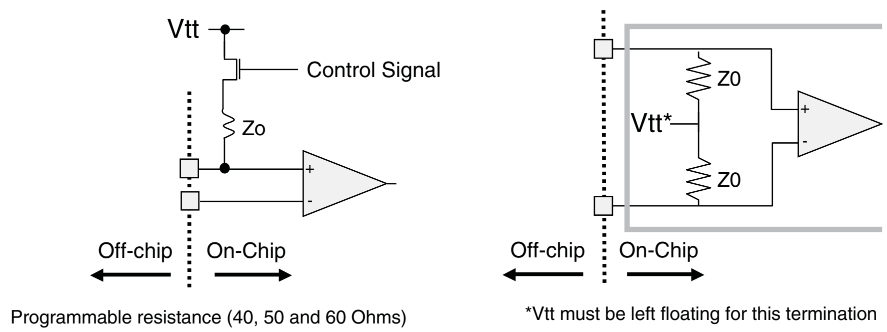
   The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

Figure 2-39. On-Chip Termination



Parallel Single-Ended Input **Differential Input**

See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT[1, 2]	DIFFERENTIAL TERMINATION RESISTOR[1]
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.
   Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
   On-chip termination tolerance +/– 20%
2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.

LatticeECP3 Family Data Sheet DC and Switching Characteristics

April 2014 | Data Sheet DS1021

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . –0.5 V to 1.32 V

Supply Voltage V_{CCAUX} . . . . –0.5 V to 3.75 V

Supply Voltage V_{CCJ} . . . . –0.5 V to 3.75 V

Output Supply Voltage V_{CCIO} . . . . –0.5 V to 3.75 V

Input or I/O Tristate Voltage Applied[4]. . . –0.5 V to 3.75 V

Storage Temperature (Ambient) . . . .–65 V to 150 °C

Junction Temperature (T_J) . . . .+125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[4]	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (Max.)	—	—	+/–1	mA
IDK[5]	Input or I/O Leakage Current	$0 \leq V_{IN} < V_{CCIO}$	—	—	+/–1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5V$	—	18	—	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the LatticeECP3 Product Family Qualification Summary for complete qualification data, including ESD performance.

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}[1], V_{INM}[1]	Input Voltage		0	—	2.4	V
V_{CM}[1]	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/–100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/–10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

1, On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

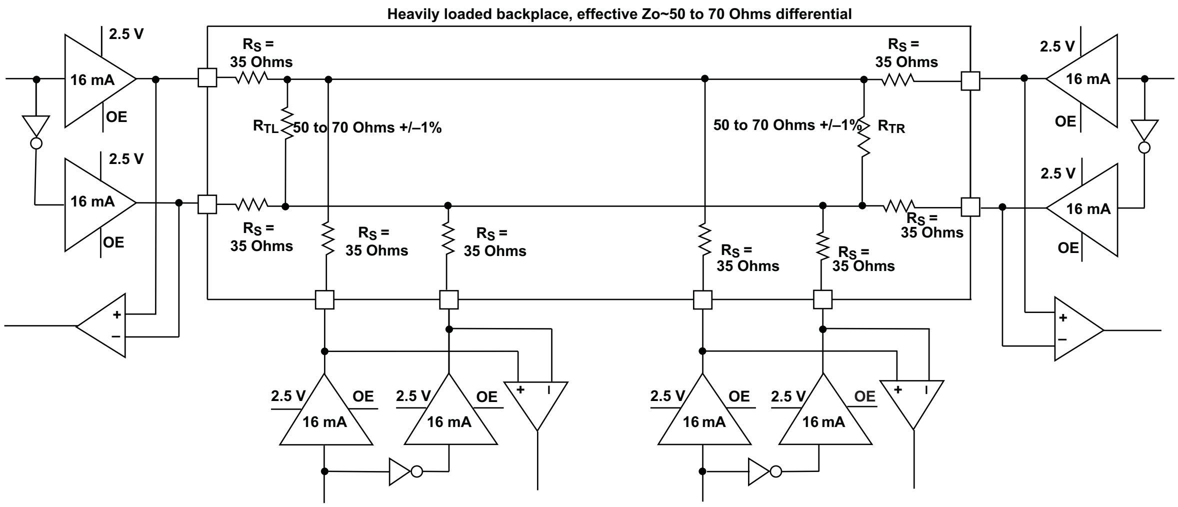


Table 3-5. MLVDS25 DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/–1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/–1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/–1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)[10]									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing									
t_{CH} (avg)[9]	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{CL} (avg)[9]	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{JIT} (per, lck)[9]	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	–90	90	–90	90	–90	90	ps
t_{JIT} (cc, lck)[9]	Output Cycle-to-Cycle Period Jitter During DLL Locking Period	All ECP3 Devices	—	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
9. Using settings generated by IPexpress.
10. These numbers are generated using best case PLL located in the center of the device.
11. Uses SSTL25 Class II Differential I/O Standard.
12. All numbers are generated with ispLEVER 8.1 software.
13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

LatticeECP3 Internal Switching Characteristics[1, 2, 5]

Over Recommended Commercial Operating Conditions

Parameter	Description	–8		–7		–6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t_{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	–0.097	—	–0.103	—	–0.109	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t_{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t_{SUDATA_PFU}	Data Setup Time	–0.137	—	–0.155	—	–0.174	—	ns
t_{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t_{SUADDR_PFU}	Address Setup Time	–0.227	—	–0.257	—	–0.286	—	ns
t_{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	–0.055	—	–0.055	—	–0.063	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay[4]	-	1.09	-	1.16	-	1.23	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	–0.085	—	–0.072	—	–0.058	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	–0.107	—	–0.094	—	–0.081	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	–0.218	—	–0.227	—	–0.237	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	–0.071	—	–0.070	—	–0.068	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	–0.107	—	–0.106	—	–0.106	—	ns

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP		133	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS		33.3	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	Edge Clock	40		60	%
		Primary Clock	30		70	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock < 250 MHz	45		55	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250 MHz	40		60	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting		—	—	100	ps
t_{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		—	—	+/-400	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)		550	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	—	ps
t_{INSTB}	Input clock period jitter		—	—	500	ps
t_{LOCK}	DLL lock time		8	—	8200	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t_{DEL}	Delay step size		27	45	70	ps
t_{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
For Top Edge of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ

Note: “n” is a row PIC number.

Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Breakdown table.
		Pinout Information	“Logic Signal Connections” section heading renamed “Package Pinout Information”. Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V_{CCA} signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for t_{RST}.
		Ordering Information	Updated topside marks with new logos in the Ordering Information section.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL TIming table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, t_{JIT}.
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t_{SUWREN_EBR} and t_{HWREN_EBR}.
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications

Date	Version	Section	Change Summary
			Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification
December 2010	01.7EA	Multiple	Data sheet made final. Removed “preliminary” headings.
			Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices.
			Updated for Lattice Diamond design software.
		Introduction	Corrected number of user I/Os
		Architecture	Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices.
			Updated description of General Purpose PLL
			Added additional information in the Flexible Quad SERDES Architecture section.
			Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal).
			Updated Figure 2-16, Per Region Secondary Clock Selection.
			Updated description for On-Chip Programmable Termination.
			Added information about number of rows of DSP slices.
			Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes.
			Updated information for sysIO buffer pairs.
			Corrected minimum number of General Purpose PLLs (was 4, now 2).
		DC and Switching Characteristics	Regenerated sysCONFIG Port Timing figure.
			Added t_W (clock pulse width) in External Switching Characteristics table.
			Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table.
			Added Jitter Transfer figures in SERDES External Reference Clock section.
			Corrected capacitance information in the DC Electrical Characteristics table.
			Corrected data in the Register-to-Register Performance table.
			Corrected GDDR Parameter name HOGDDR.
			Corrected RSDS25 -7 data in Family Timing Adders table.
			Added footnotes 10-12 to DDR data information in the External Switching Characteristics table.
			Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDRX2 Parameters).
			Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differential Signaling)) and 3-6 (Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)).
			Updated Supply Current table.
			Added GDDR interface information to the External Switching and Characteristics table.
			Added footnote to sysIO Recommended Operating Conditions table.
			Added footnote to LVDS25 table.
			Corrected DDR section footnotes and references.
			Corrected Hot Socketing support from “top and bottom banks” to “top and bottom I/O pins”.
		Pinout Information	Updated description for VTTx.