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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

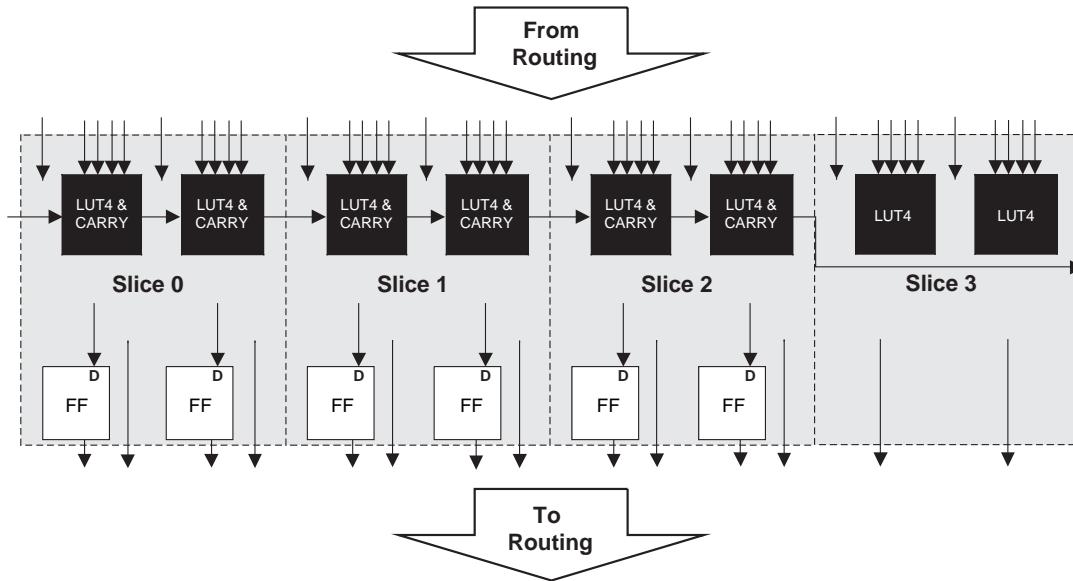
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	33000
Total RAM Bits	1358848
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-7ftn256i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-7ftn256i</a>

Figure 2-2. PFU Diagram



## Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

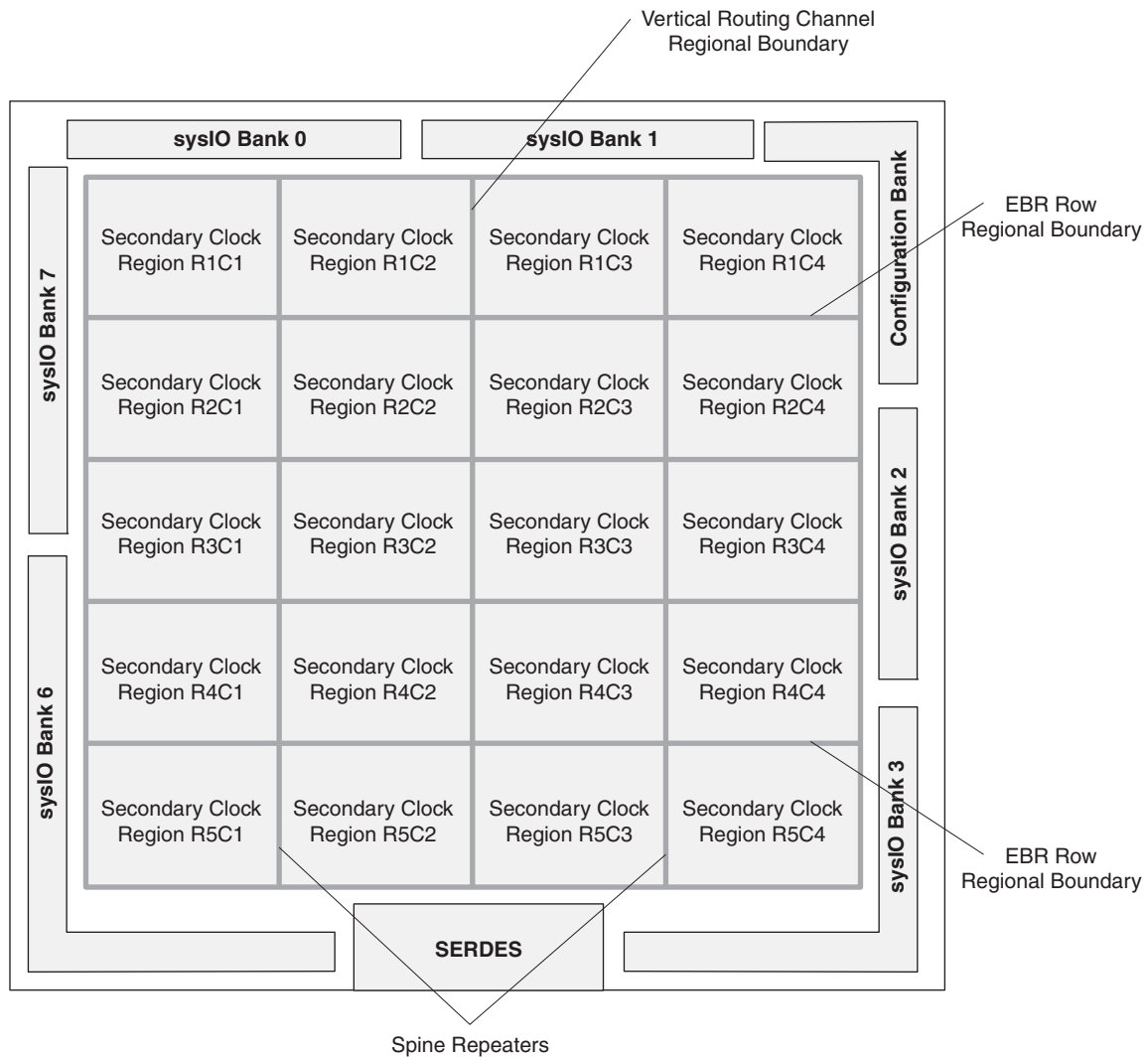
Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

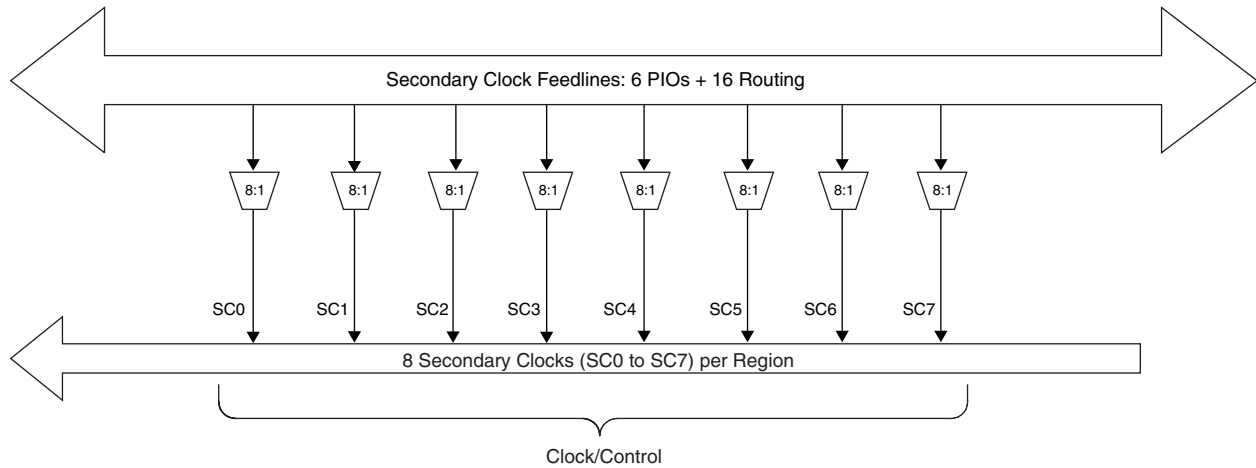
Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



**Figure 2-16. Per Region Secondary Clock Selection**

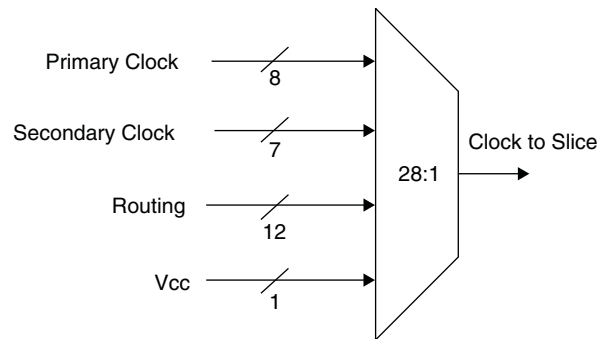


**Slice Clock Selection**

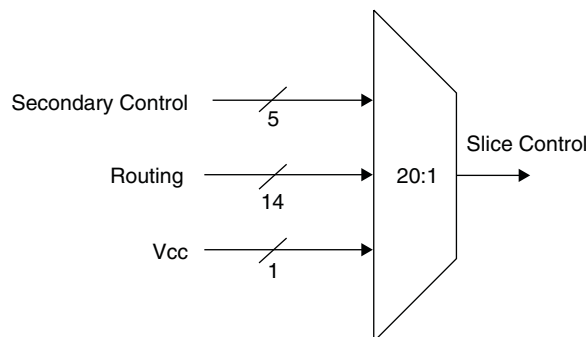
Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

**Figure 2-17. Slice0 through Slice2 Clock Selection**

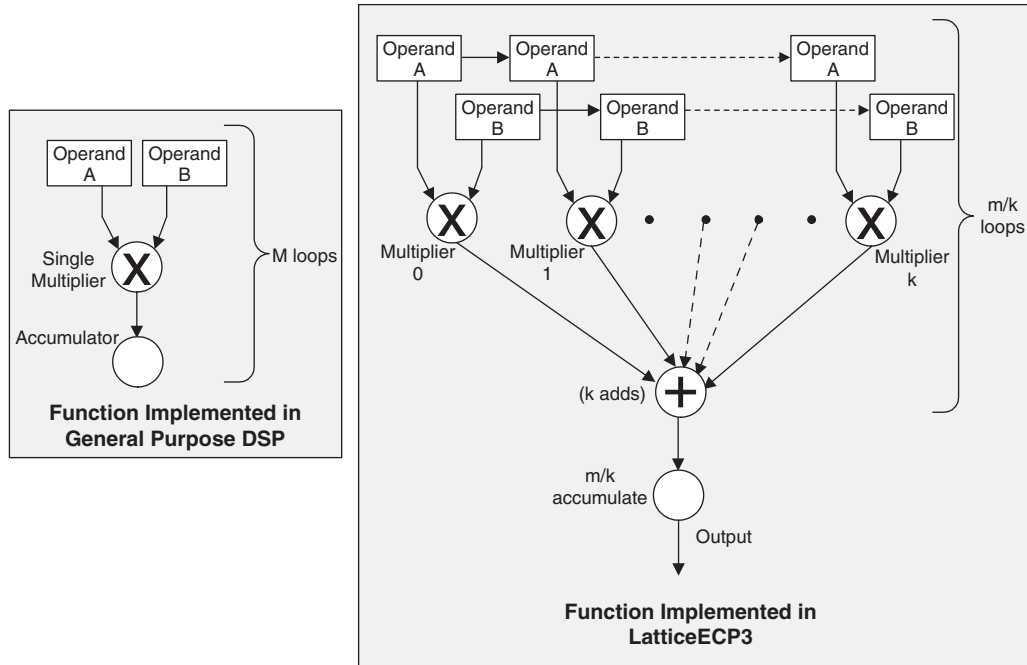


**Figure 2-18. Slice0 through Slice2 Control Selection**



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

**Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches**



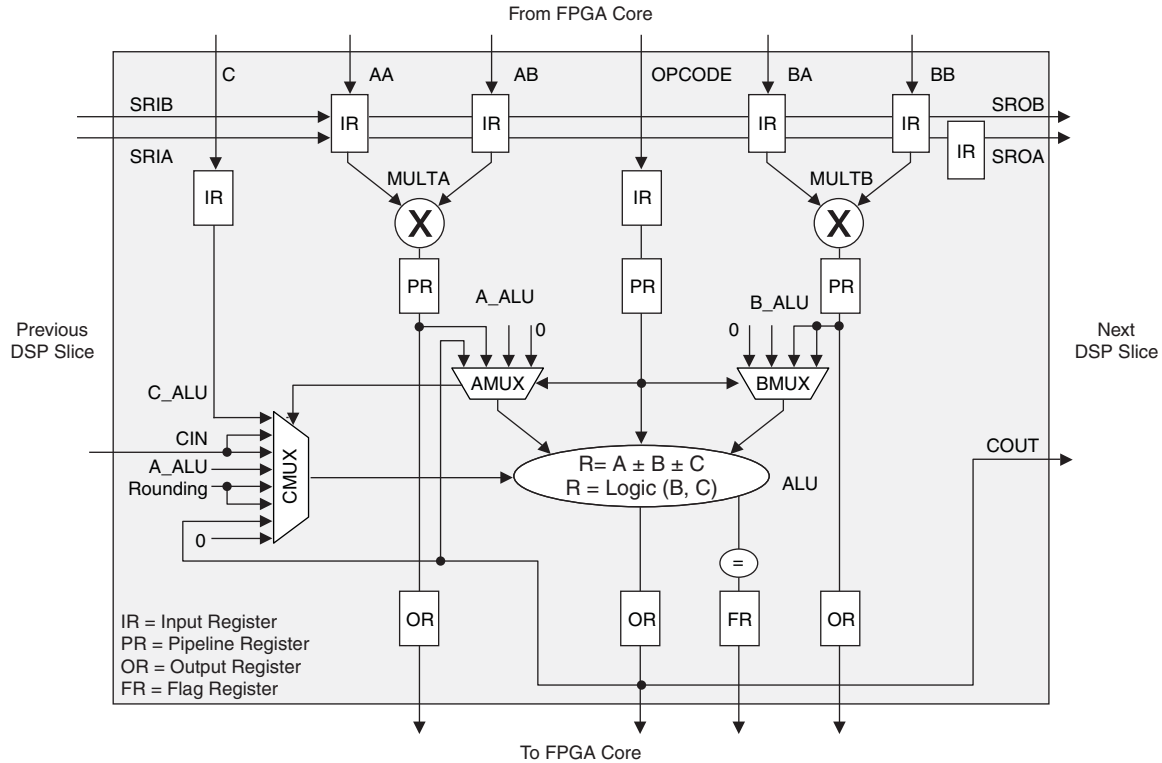
## LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multipliers per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multipliers feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A\_ALU, B\_ALU and C\_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 <sup>1</sup>	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

## SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

## Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

**Table 2-15. LatticeECP3 Primary and Secondary Protocol Support**

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

**Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)**

MCCLK (MHz)	MCCLK (MHz)
	10
2.5 <sup>1</sup>	13
4.3	15 <sup>2</sup>
5.4	20
6.9	26
8.1	33 <sup>3</sup>
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

## Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the [LatticeECP3 Pin Migration Tables](#) and Diamond software for specific restrictions and limitations.



### BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS25 Multi-point Output Example

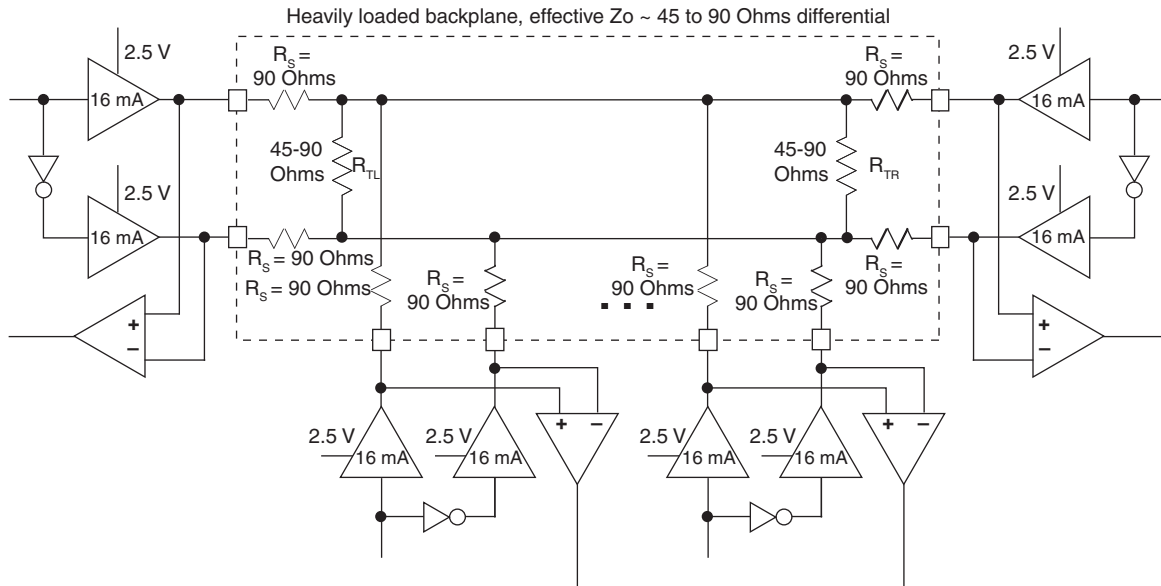


Table 3-2. BLVDS25 DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V <sub>CCIO</sub>	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R <sub>TR</sub>	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V <sub>OH</sub>	Output High Voltage	1.38	1.48	V
V <sub>OL</sub>	Output Low Voltage	1.12	1.02	V
V <sub>OD</sub>	Output Differential Voltage	0.25	0.46	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

### RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

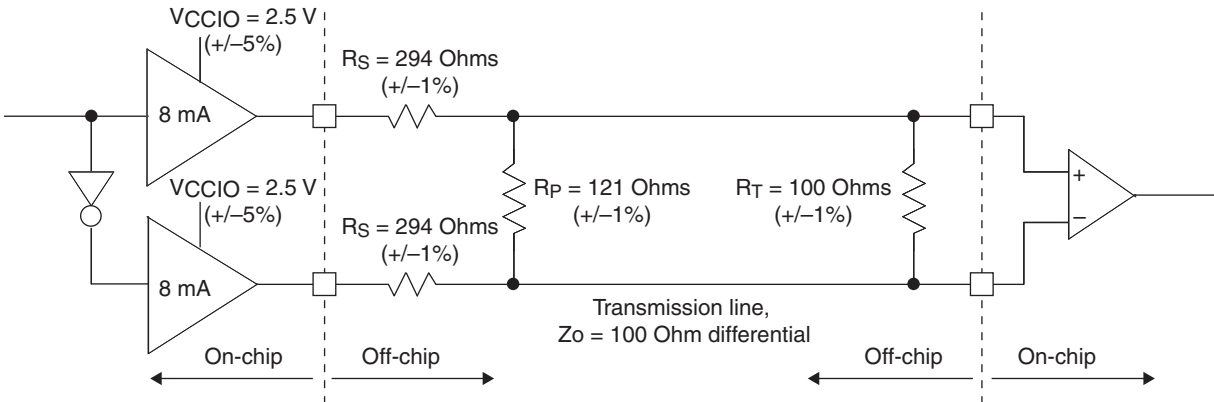


Table 3-4. RSDS25E DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	V
Z <sub>OUT</sub>	Driver Impedance	20	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	294	Ω
R <sub>P</sub>	Driver Parallel Resistor (+/-1%)	121	Ω
R <sub>T</sub>	Receiver Termination (+/-1%)	100	Ω
V <sub>OH</sub>	Output High Voltage	1.35	V
V <sub>OL</sub>	Output Low Voltage	1.15	V
V <sub>OD</sub>	Output Differential Voltage	0.20	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	V
Z <sub>BACK</sub>	Back Impedance	101.5	Ω
I <sub>DC</sub>	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

## LatticeECP3 External Switching Characteristics (Continued)<sup>1, 2, 3, 13</sup>

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.7	—	0.8	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.6	—	1.8	—	2.0	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	ECP3-35EA	—	3.2	—	3.4	—	3.6	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.6	—	0.7	—	0.8	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-35EA	0.3	—	0.3	—	0.4	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.6	—	1.7	—	1.8	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	ECP3-17EA	—	3.0	—	3.3	—	3.5	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.6	—	0.7	—	0.8	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-17EA	0.3	—	0.3	—	0.4	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.6	—	1.7	—	1.8	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
<b>Generic DDR<sup>12</sup></b>									
<b>Generic DDRX1 Inputs with Clock and Data (&gt;10 Bits Wide) Centered at Pin (GDDR1_RX.SCLK.Centered) Using PCLK Pin for Clock Input</b>									
t <sub>SUGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	480	—	480	—	480	—	ps
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	480	—	480	—	480	—	ps
f <sub>MAX_GDDR</sub>	DDR1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
<b>Generic DDRX1 Inputs with Clock and Data (&gt;10 Bits Wide) Aligned at Pin (GDDR1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input</b>									
<b>Data Left, Right, and Top Sides and Clock Left and Right Sides</b>									
t <sub>DVACKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
<b>Generic DDRX1 Inputs with Clock and Data (&gt;10 Bits Wide) Aligned at Pin (GDDR1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input</b>									
<b>Data Left, Right and Top Sides and Clock Left and Right Sides</b>									
t <sub>DVACKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f <sub>MAX_GDDR</sub>	DDR1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
<b>Generic DDRX1 Inputs with Clock and Data (&lt;10 Bits Wide) Centered at Pin (GDDR1_RX.DQS.Centered) Using DQS Pin for Clock Input</b>									
t <sub>SUGDDR</sub>	Data Setup After CLK	All ECP3EA Devices	535	—	535	—	535	—	ps
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	535	—	535	—	535	—	ps
f <sub>MAX_GDDR</sub>	DDR1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
<b>Generic DDRX1 Inputs with Clock and Data (&lt;10bits wide) Aligned at Pin (GDDR1_RX.DQS.Aligned) Using DQS Pin for Clock Input</b>									
<b>Data and Clock Left and Right Sides</b>									
t <sub>DVACKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI

Figure 3-6. Generic DDRX1/DDR2 (With Clock and Data Edges Aligned)

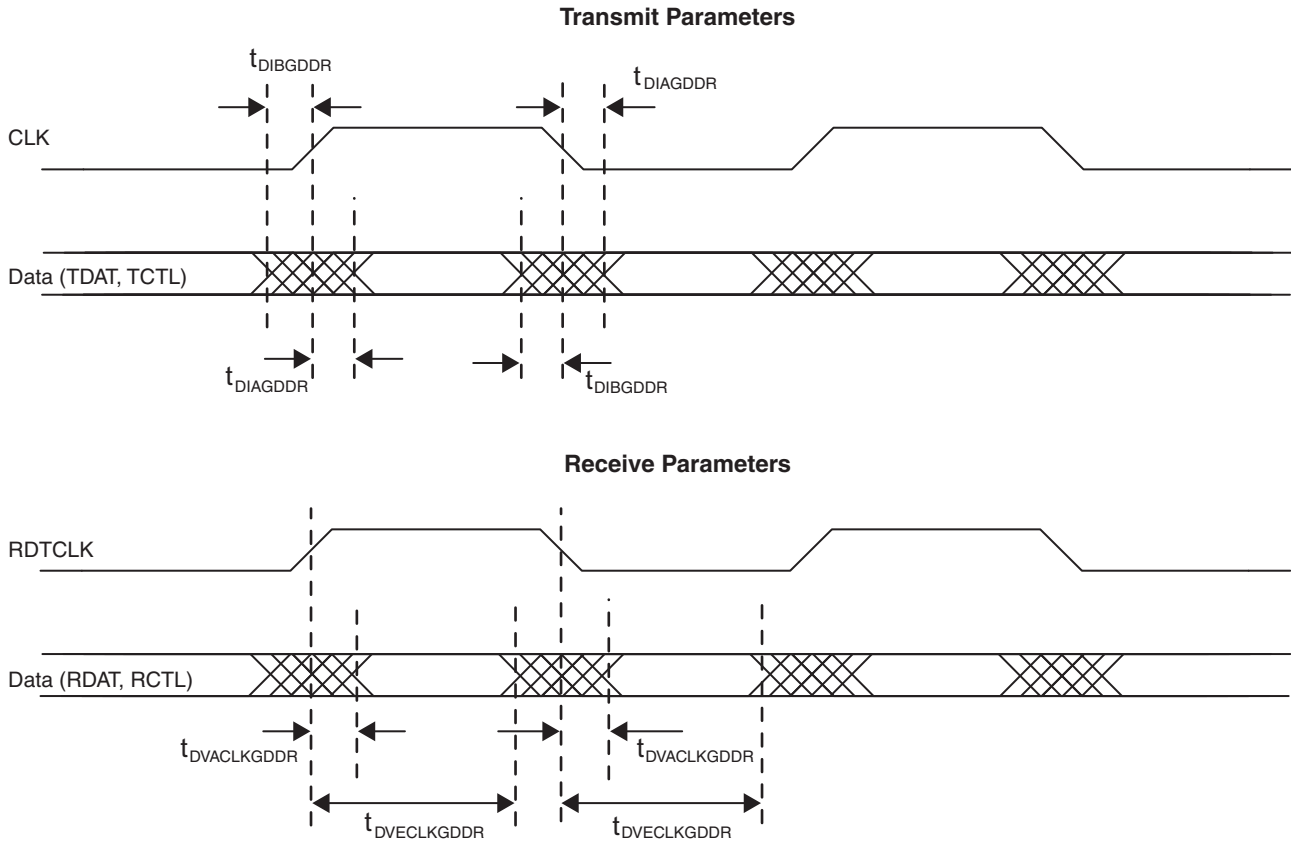
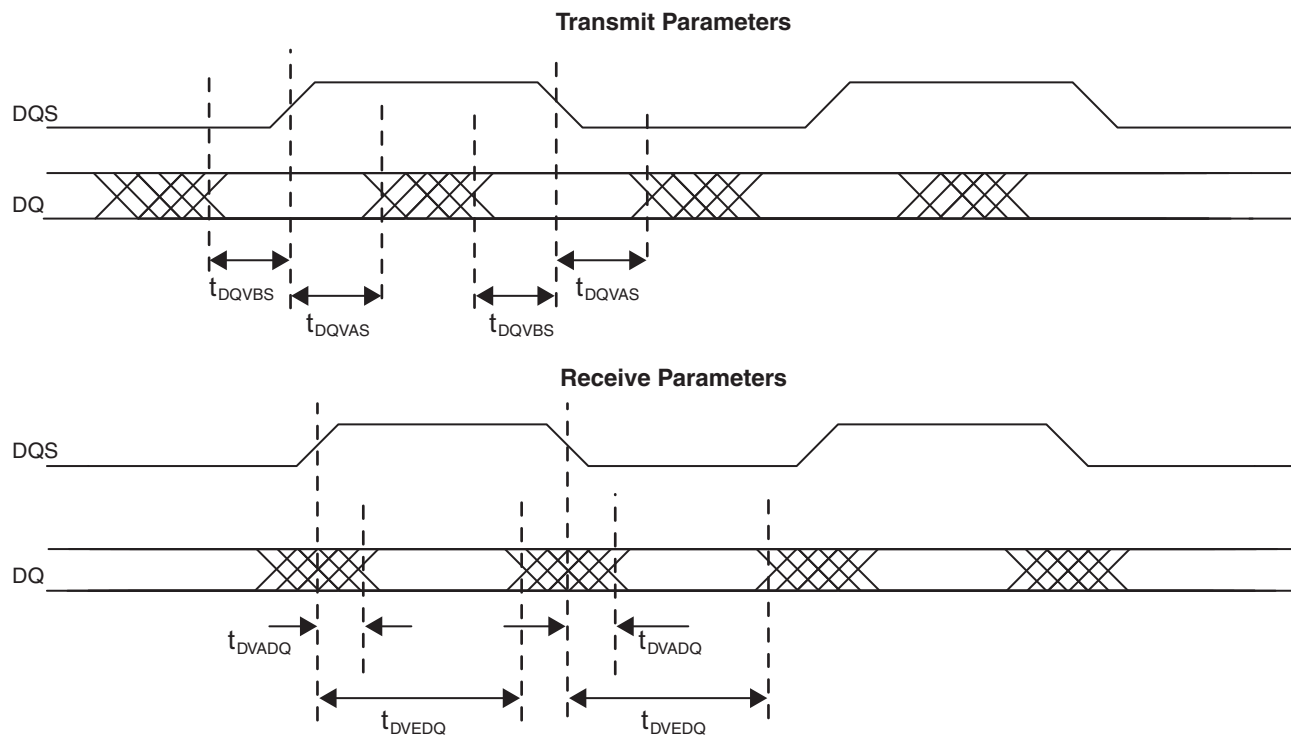
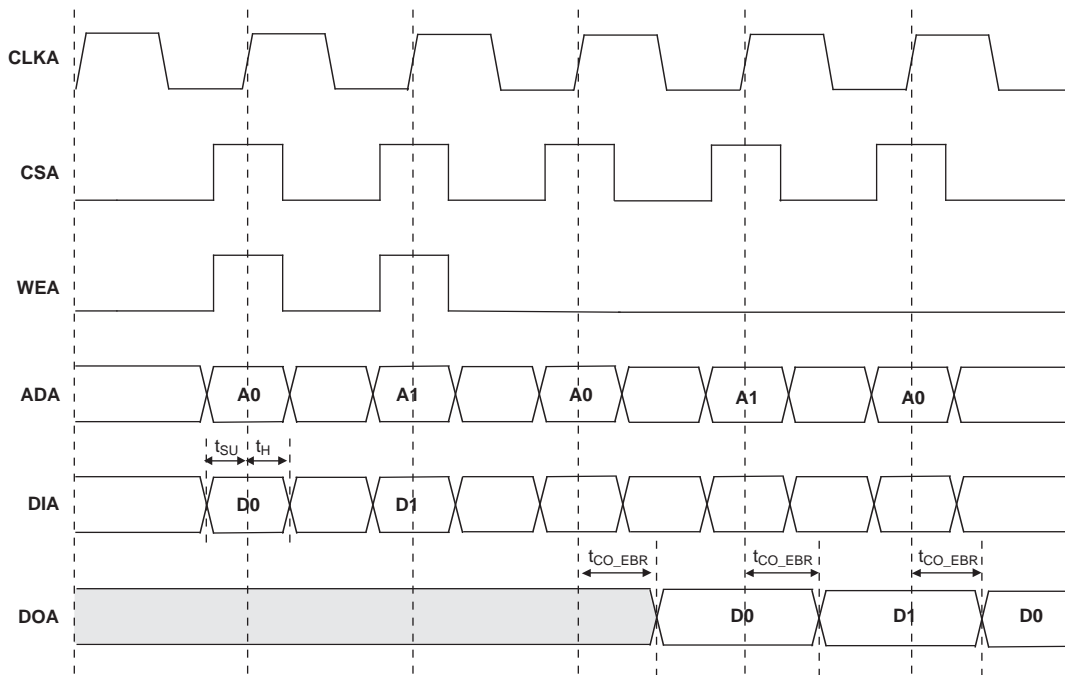


Figure 3-7. DDR/DDR2/DDR3 Parameters



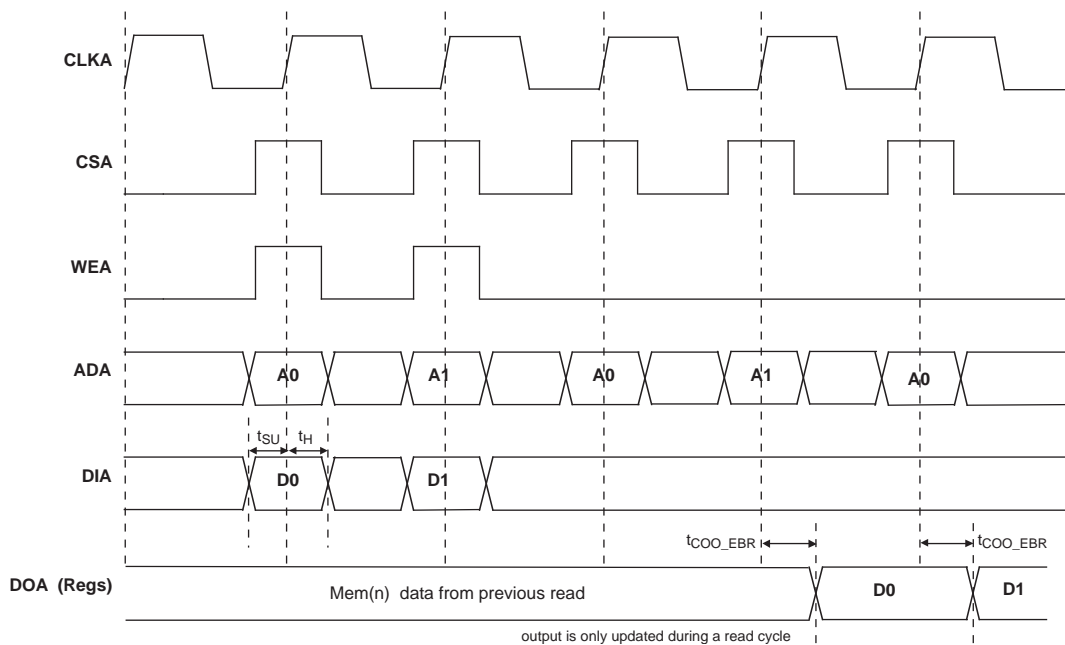
## Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



## SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units	
RX-CID <sub>S</sub>	Stream of nontransitions <sup>1</sup> (CID = Consecutive Identical Digits) @ 10 <sup>-12</sup> BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
V <sub>RX-DIFF-S</sub>	Differential input sensitivity	150	—	1760	mV, p-p	
V <sub>RX-IN</sub>	Input levels	0	—	V <sub>CCA</sub> +0.5 <sup>4</sup>	V	
V <sub>RX-CM-DC</sub>	Input common mode range (DC coupled)	0.6	—	V <sub>CCA</sub>	V	
V <sub>RX-CM-AC</sub>	Input common mode range (AC coupled) <sup>3</sup>	0.1	—	V <sub>CCA</sub> +0.2	V	
T <sub>RX-RELOCK</sub>	SCDR re-lock time <sup>2</sup>	—	1000	—	Bits	
Z <sub>RX-TERM</sub>	Input termination 50/75 Ohm/High Z	-20%	50/75/HiZ	+20%	Ohms	
RL <sub>RX-RL</sub>	Return loss (without package)	10	—	—	dB	

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

### Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

**Table 3-11. Periodic Receiver Jitter Tolerance Specification**

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

## LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

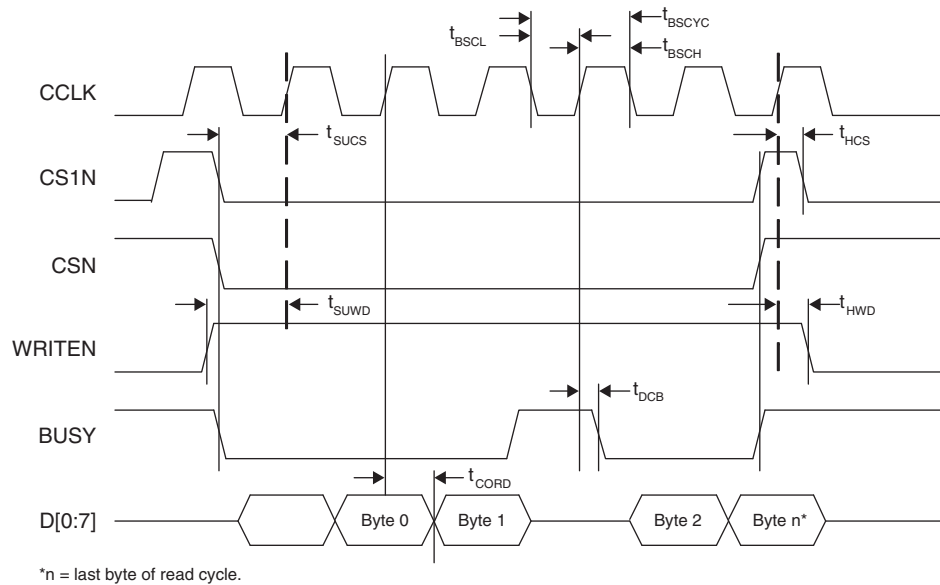
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
$t_{SSCL}$	CCLK Minimum Low Pulse	5	—	ns
$t_{HLCH}$	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
$t_{CHHH}$	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
<b>Master and Slave SPI (Continued)</b>				
$t_{CHHL}$	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
$t_{HHCH}$	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
$t_{HLQZ}$	HOLDN to Output High-Z	—	9	ns
$t_{HHQX}$	HOLDN to Output Low-Z	—	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

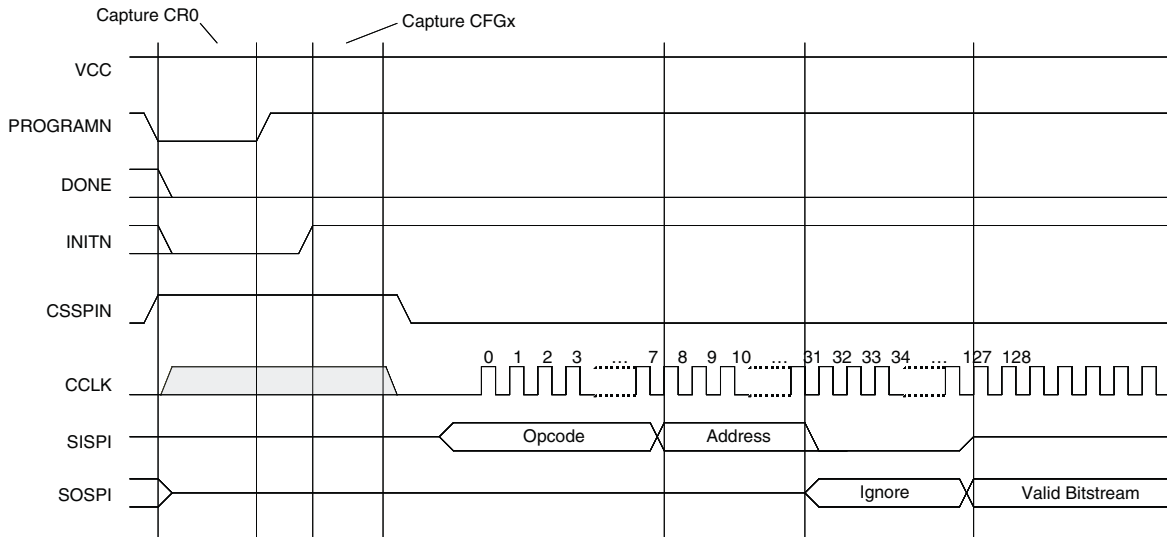
Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle

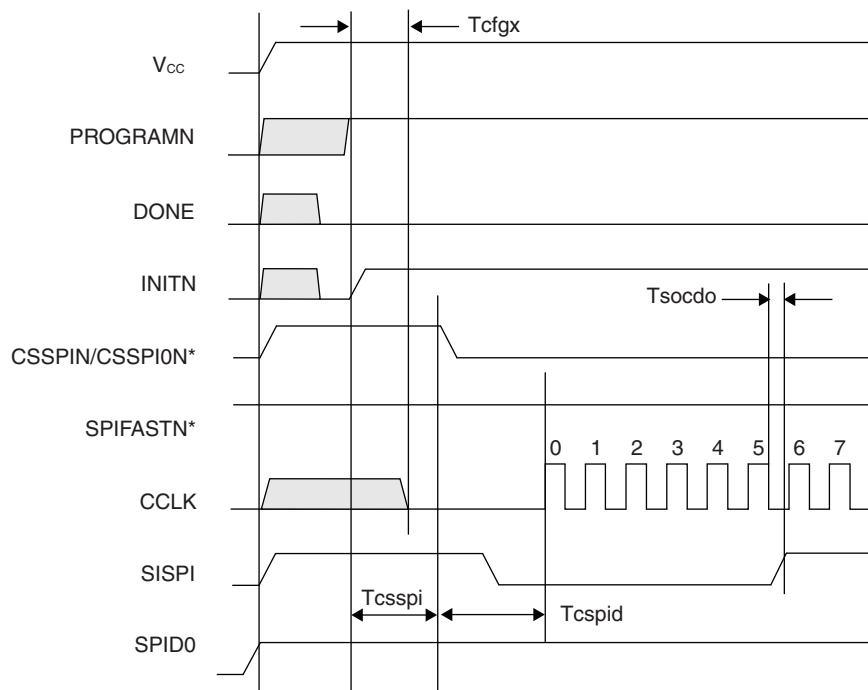




**Figure 3-28. Master SPI Configuration Waveforms**



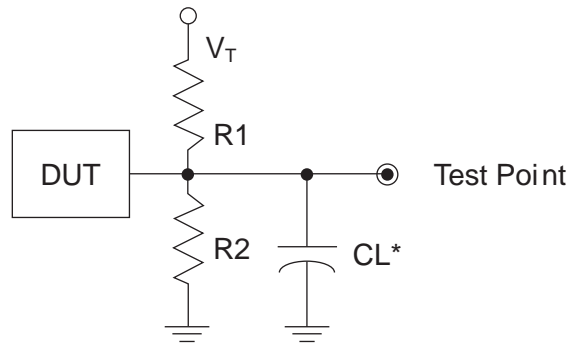
**Figure 3-29. Master SPI POR Waveforms**



## Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

**Figure 3-33. Output Test Load, LVTTTL and LVCMOS Standards**



\*CL Includes Test Fixture and Probe Capacitance

**Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V <sub>OH</sub> - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

**Signal Descriptions (Cont.)**

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
<b>Test and Programming (Dedicated Pins)</b>		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
<b>Configuration Pads (Used During sysCONFIG)</b>		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSN/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration.
		sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

**LatticeECP3 Devices, Green and Lead-Free Packaging**

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

**Commercial**

Part Number	Voltage	Grade	Power	Package <sup>1</sup>	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at [www.latticesemi.com](http://www.latticesemi.com).

- TN1169, [LatticeECP3 sysCONFIG Usage Guide](#)
- TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#)
- TN1177, [LatticeECP3 sysIO Usage Guide](#)
- TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#)
- TN1179, [LatticeECP3 Memory Usage Guide](#)
- TN1180, [LatticeECP3 High-Speed I/O Interface](#)
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- TN1182, [LatticeECP3 sysDSP Usage Guide](#)
- TN1184, [LatticeECP3 Soft Error Detection \(SED\) Usage Guide](#)
- TN1189, [LatticeECP3 Hardware Checklist](#)
- TN1215, [LatticeECP2MS and LatticeECP2S Devices](#)
- TN1216, [LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3](#)
- TN1222, [LatticeECP3 Slave SPI Port User's Guide](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): [www.jedec.org](http://www.jedec.org)
- PCI: [www.pcisig.com](http://www.pcisig.com)