# Lattice Semiconductor Corporation - LFE3-35EA-8FN484I Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4125 |
| Number of Logic Elements/Cells | 33000 |
| Total RAM Bits | 1358848 |
| Number of I/O | 295 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-8fn484i |

# Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

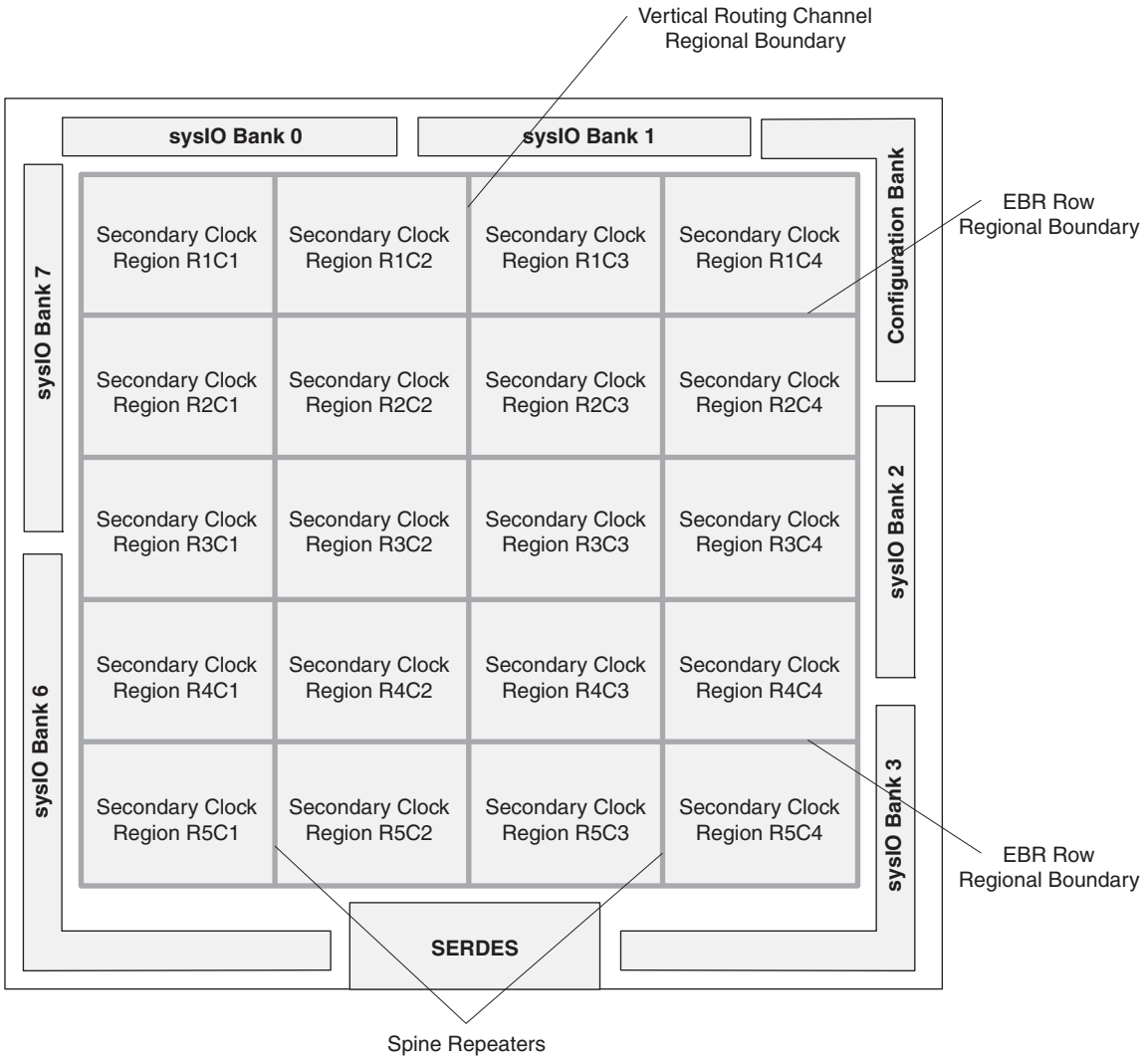
The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

*Table 2-6. Secondary Clock Regions*

| Device | Number of Secondary Clock Regions |
|---|---|
| ECP3-17 | 16 |
| ECP3-35 | 16 |
| ECP3-70 | 20 |
| ECP3-95 | 20 |
| ECP3-150 | 36 |

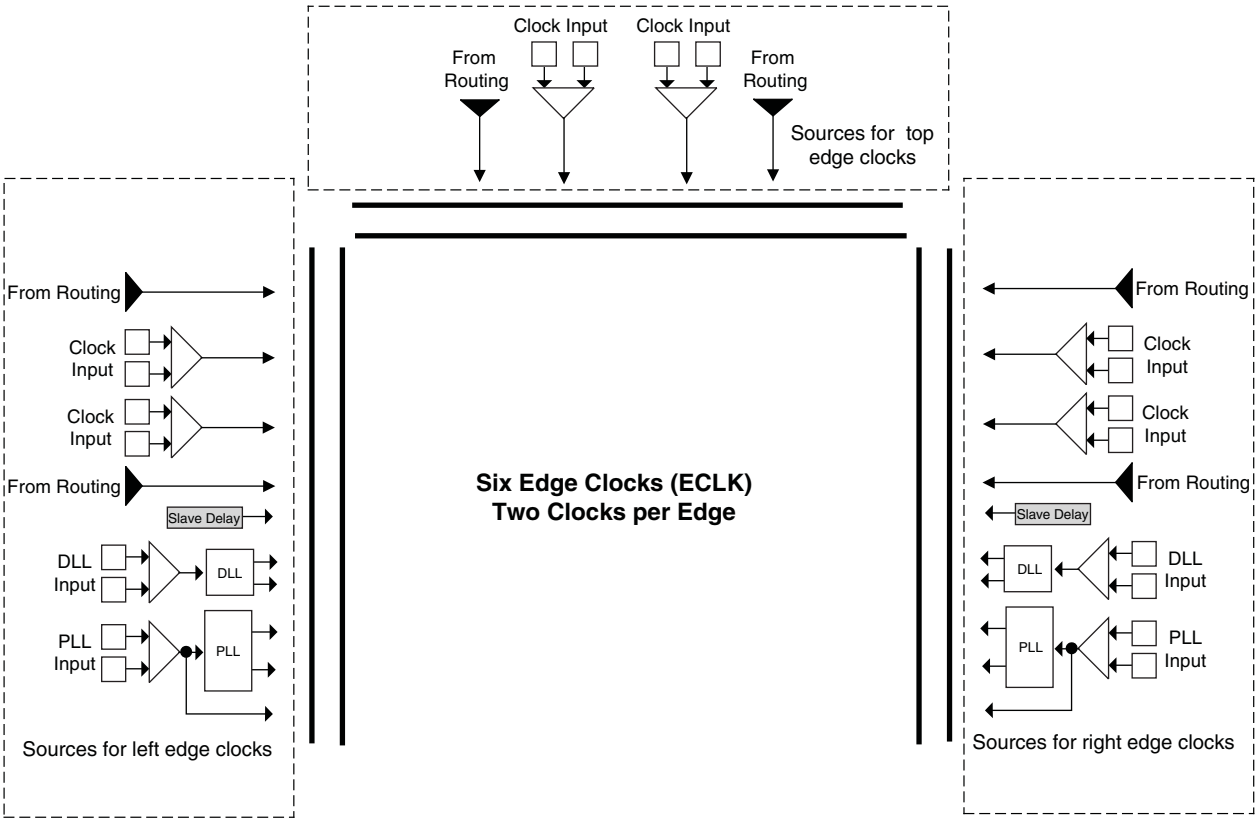
*Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions*



## Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

***Figure 2-19. Edge Clock Sources***




Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

## Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

## sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see TN1179, LatticeECP3 Memory Usage Guide.

***Table 2-7. sysMEM Block Configurations***

| Memory Mode | Configurations |
|---|---|
| Single Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |
| True Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18 |
| Pseudo Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

## MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

***Figure 2-26. MULT sysDSP Element***

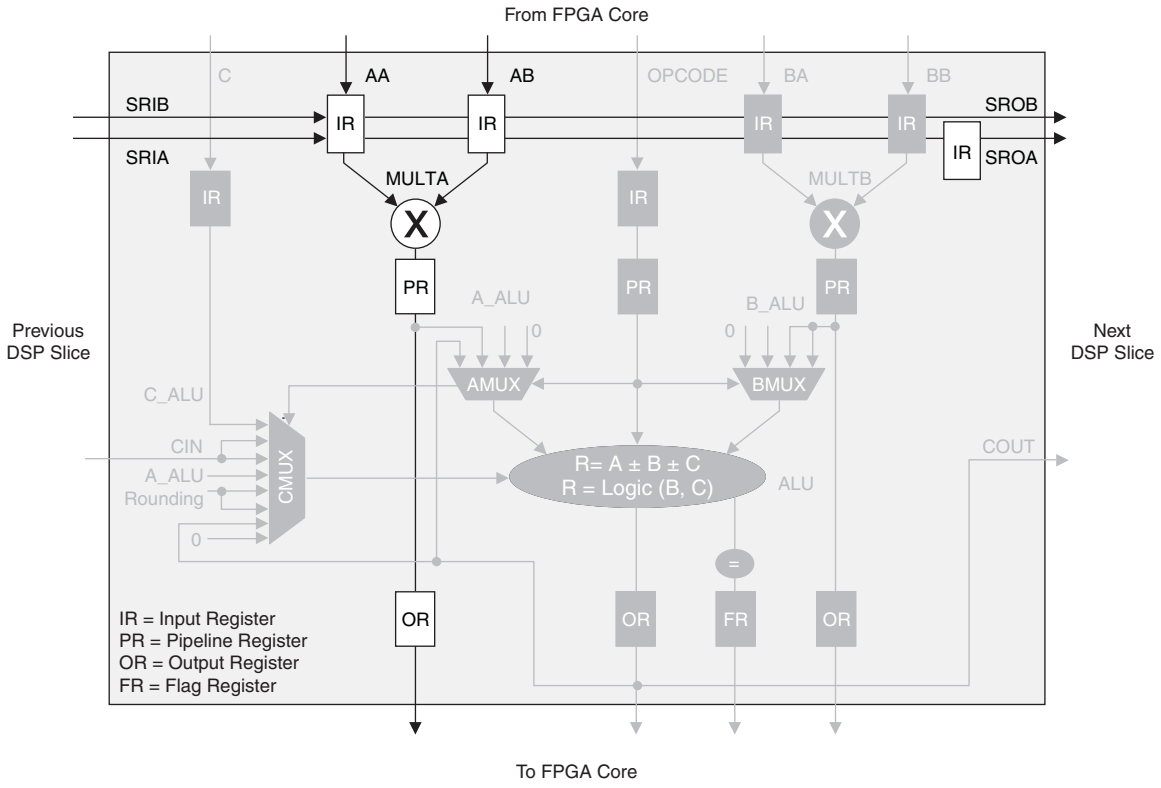
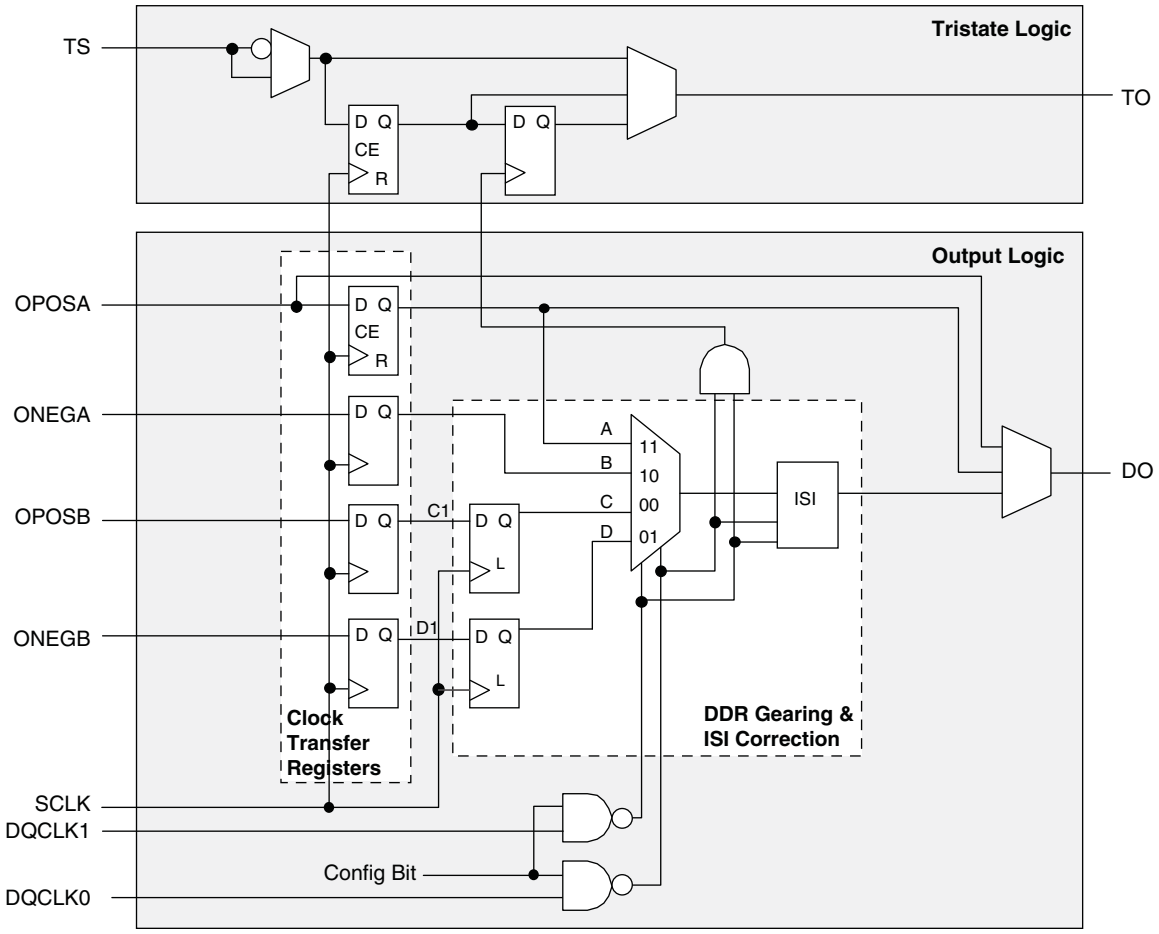


*Figure 2-34. Output and Tristate Block for Left and Right Edges*




## Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

## ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

## DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

### Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

### Bottom Edge

PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

### Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

***Figure 2-35. DQS Grouping on the Left, Right and Top Edges***

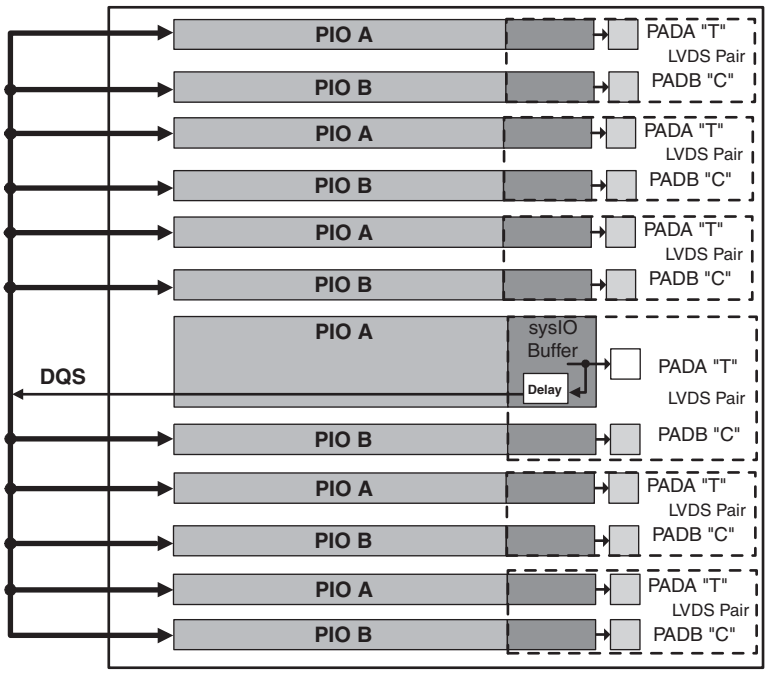
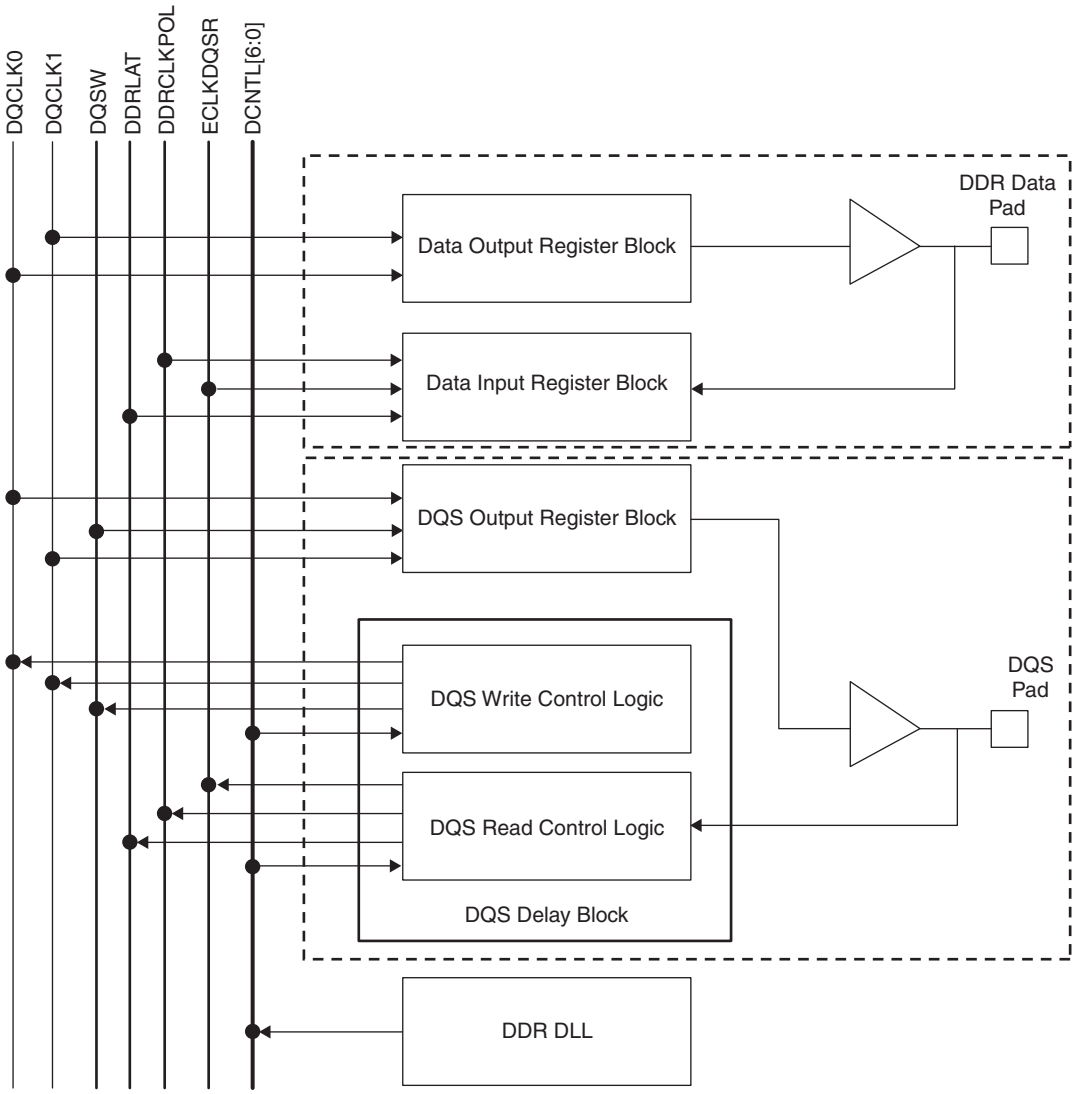


*Figure 2-37. DQS Local Bus*




## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

## DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

## LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical | | Units |
|---|---|---|---|---|---|
| | | | –6L, –7L, –8L | –6, –7, –8 | |
| $I_{CC}$ | Core Power Supply Current | ECP-17EA | 29.8 | 49.4 | mA |
| | | ECP3-35EA | 53.7 | 89.4 | mA |
| | | ECP3-70EA | 137.3 | 230.7 | mA |
| | | ECP3-95EA | 137.3 | 230.7 | mA |
| | | ECP3-150EA | 219.5 | 370.9 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP-17EA | 18.3 | 19.4 | mA |
| | | ECP3-35EA | 19.6 | 23.1 | mA |
| | | ECP3-70EA | 26.5 | 32.4 | mA |
| | | ECP3-95EA | 26.5 | 32.4 | mA |
| | | ECP3-150EA | 37.0 | 45.7 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (Per PLL) | ECP-17EA | 0.0 | 0.0 | mA |
| | | ECP3-35EA | 0.1 | 0.1 | mA |
| | | ECP3-70EA | 0.1 | 0.1 | mA |
| | | ECP3-95EA | 0.1 | 0.1 | mA |
| | | ECP3-150EA | 0.1 | 0.1 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP-17EA | 1.3 | 1.4 | mA |
| | | ECP3-35EA | 1.3 | 1.4 | mA |
| | | ECP3-70EA | 1.4 | 1.5 | mA |
| | | ECP3-95EA | 1.4 | 1.5 | mA |
| | | ECP3-150EA | 1.4 | 1.5 | mA |
| $I_{CCJ}$ | JTAG Power Supply Current | All Devices | 2.5 | 2.5 | mA |
| $I_{CCA}$ | Transmit, Receive, PLL and Reference Clock Buffer Power Supply | ECP-17EA | 6.1 | 6.1 | mA |
| | | ECP3-35EA | 6.1 | 6.1 | mA |
| | | ECP3-70EA | 18.3 | 18.3 | mA |
| | | ECP3-95EA | 18.3 | 18.3 | mA |
| | | ECP3-150EA | 24.4 | 24.4 | mA |

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

# LatticeECP3 External Switching Characteristics [1, 2, 3, 13]

**Over Recommended Commercial Operating Conditions**

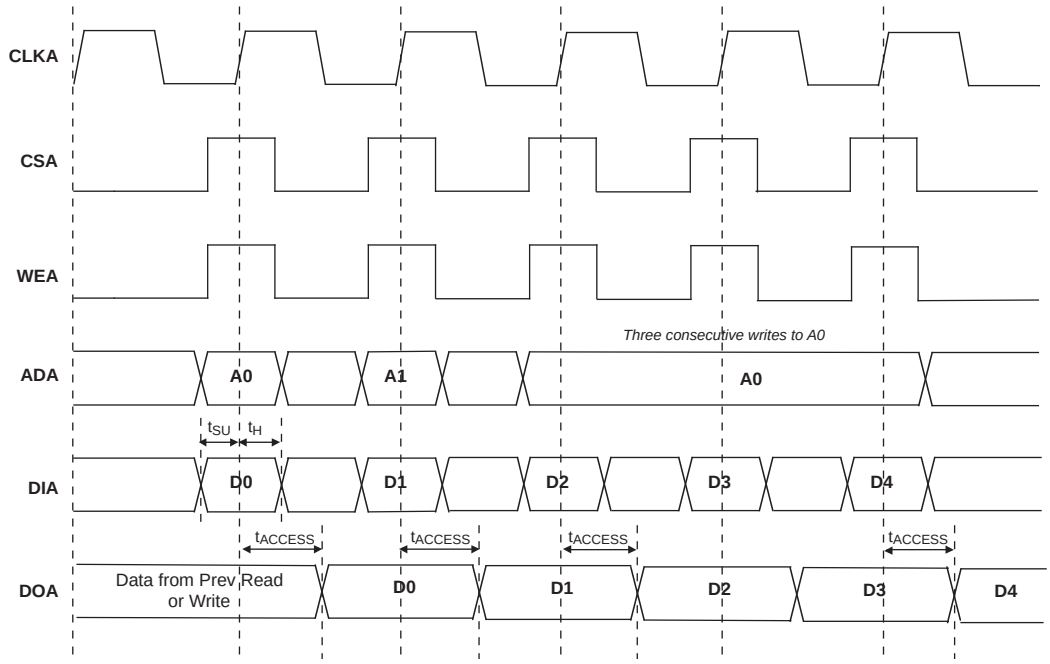
| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clock[6]** | | | | | | | | | |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | ECP3-150EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | ECP3-150EA | 0.8 | — | 0.9 | — | 1.0 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | ECP3-150EA | — | 300 | — | 330 | — | 360 | ps |
| $t_{SKEW\_PRIB}$ | Primary Clock Skew Within a Bank | ECP3-150EA | — | 250 | — | 280 | — | 300 | ps |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | ECP3-70EA/95EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_PRI}$ | Pulse Width for Primary Clock | ECP3-70EA/95EA | 0.8 | — | 0.9 | — | 1.0 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | ECP3-70EA/95EA | — | 360 | — | 370 | — | 380 | ps |
| $t_{SKEW\_PRIB}$ | Primary Clock Skew Within a Bank | ECP3-70EA/95EA | — | 310 | — | 320 | — | 330 | ps |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | ECP3-35EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_PRI}$ | Pulse Width for Primary Clock | ECP3-35EA | 0. 8 | — | 0.9 | — | 1.0 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | ECP3-35EA | — | 300 | — | 330 | — | 360 | ps |
| $t_{SKEW\_PRIB}$ | Primary Clock Skew Within a Bank | ECP3-35EA | — | 250 | — | 280 | — | 300 | ps |
| $f_{MAX\_PRI}$ | Frequency for Primary Clock Tree | ECP3-17EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_PRI}$ | Pulse Width for Primary Clock | ECP3-17EA | 0. 8 | — | 0.9 | — | 1.0 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | ECP3-17EA | — | 310 | — | 340 | — | 370 | ps |
| $t_{SKEW\_PRIB}$ | Primary Clock Skew Within a Bank | ECP3-17EA | — | 220 | — | 230 | — | 240 | ps |
| **Edge Clock[6]** | | | | | | | | | |
| $f_{MAX\_EDGE}$ | Frequency for Edge Clock | ECP3-150EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | ECP3-150EA | 0.9 | — | 1.0 | — | 1.2 | — | ns |
| $t_{SKEW\_EDGE\_DQS}$ | Edge Clock Skew Within an Edge of the Device | ECP3-150EA | — | 200 | — | 210 | — | 220 | ps |
| $f_{MAX\_EDGE}$ | Frequency for Edge Clock | ECP3-70EA/95EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | ECP3-70EA/95EA | 0. 9 | — | 1.0 | — | 1.2 | — | ns |
| $t_{SKEW\_EDGE\_DQS}$ | Edge Clock Skew Within an Edge of the Device | ECP3-70EA/95EA | — | 200 | — | 210 | — | 220 | ps |
| $f_{MAX\_EDGE}$ | Frequency for Edge Clock | ECP3-35EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | ECP3-35EA | 0. 9 | — | 1.0 | — | 1.2 | — | ns |
| $t_{SKEW\_EDGE\_DQS}$ | Edge Clock Skew Within an Edge of the Device | ECP3-35EA | — | 200 | — | 210 | — | 220 | ps |
| $f_{MAX\_EDGE}$ | Frequency for Edge Clock | ECP3-17EA | — | 500 | — | 420 | — | 375 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | ECP3-17EA | 0. 9 | — | 1.0 | — | 1.2 | — | ns |
| $t_{SKEW\_EDGE\_DQS}$ | Edge Clock Skew Within an Edge of the Device | ECP3-17EA | — | 200 | — | 210 | — | 220 | ps |
| **Generic SDR** | | | | | | | | | |
| **General I/O Pin Parameters Using Dedicated Clock Input Primary Clock Without PLL[2]** | | | | | | | | | |
| $t_{CO}$ | Clock to Output - PIO Output Register | ECP3-150EA | — | 3.9 | — | 4.3 | — | 4.7 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | ECP3-150EA | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | ECP3-150EA | 1.5 | — | 1.7 | — | 2.0 | — | ns |
| $t_{SU\_DEL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-150EA | 1.3 | — | 1.5 | — | 1.7 | — | ns |

# LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-35EA | 683 | — | 688 | — | 690 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-35EA | 683 | — | 688 | — | 690 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-17EA | 683 | — | 688 | — | 690 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-17EA | 683 | — | 688 | — | 690 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Output with Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned)[10]** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-150EA | — | 335 | — | 338 | — | 341 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-150EA | — | 335 | — | 338 | — | 341 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-70EA/95EA | — | 339 | — | 343 | — | 347 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-70EA/95EA | — | 339 | — | 343 | — | 347 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-35EA | — | 322 | — | 320 | — | 321 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-35EA | — | 322 | — | 320 | — | 321 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-17EA | — | 322 | — | 320 | — | 321 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-17EA | — | 322 | — | 320 | — | 321 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_TX.DQS.Centered)[10]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-70EA/95EA | 657 | — | 652 | — | 650 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-70EA/95EA | 657 | — | 652 | — | 650 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-35EA | 670 | — | 675 | — | 676 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-35EA | 670 | — | 675 | — | 676 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-17EA | 670 | — | 670 | — | 670 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-17EA | 670 | — | 670 | — | 670 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_TX.Aligned)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | All ECP3EA Devices | — | 200 | — | 210 | — | 220 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | All ECP3EA Devices | — | 200 | — | 210 | — | 220 | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 500 | — | 420 | — | 375 | MHz |
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQSDLL.Centered)[11]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | All ECP3EA Devices | 400 | — | 400 | — | 431 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | All ECP3EA Devices | 400 | — | 400 | — | 432 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 400 | — | 400 | — | 375 | MHz |

*Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

## LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5, 7] (Continued)

**Over Recommended Commercial Operating Conditions**

| Buffer Type | Description | –8 | –7 | –6 | Units |
|---|---|---|---|---|---|
| RSDS25 | RSDS, VCCIO = 2.5 V | –0.07 | –0.04 | –0.01 | ns |
| PPLVDS | Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V | –0.22 | –0.19 | –0.16 | ns |
| LVPECL33 | LVPECL, Emulated, VCCIO = 3.3 V | 0.67 | 0.76 | 0.86 | ns |
| HSTL18_I | HSTL_18 class I 8mA drive, VCCIO = 1.8 V | 1.20 | 1.34 | 1.47 | ns |
| HSTL18_II | HSTL_18 class II, VCCIO = 1.8 V | 0.89 | 1.00 | 1.11 | ns |
| HSTL18D_I | Differential HSTL 18 class I 8 mA drive | 1.20 | 1.34 | 1.47 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.89 | 1.00 | 1.11 | ns |
| HSTL15_I | HSTL_15 class I 4 mA drive, VCCIO = 1.5 V | 1.67 | 1.83 | 1.99 | ns |
| HSTL15D_I | Differential HSTL 15 class I 4 mA drive | 1.67 | 1.83 | 1.99 | ns |
| SSTL33_I | SSTL_3 class I, VCCIO = 3.3 V | 1.12 | 1.17 | 1.21 | ns |
| SSTL33_II | SSTL_3 class II, VCCIO = 3.3 V | 1.08 | 1.12 | 1.15 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 1.12 | 1.17 | 1.21 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 1.08 | 1.12 | 1.15 | ns |
| SSTL25_I | SSTL_2 class I 8 mA drive, VCCIO = 2.5 V | 1.06 | 1.19 | 1.31 | ns |
| SSTL25_II | SSTL_2 class II 16 mA drive, VCCIO = 2.5 V | 1.04 | 1.17 | 1.31 | ns |
| SSTL25D_I | Differential SSTL_2 class I 8 mA drive | 1.06 | 1.19 | 1.31 | ns |
| SSTL25D_II | Differential SSTL_2 class II 16 mA drive | 1.04 | 1.17 | 1.31 | ns |
| SSTL18_I | SSTL_1.8 class I, VCCIO = 1.8 V | 0.70 | 0.84 | 0.97 | ns |
| SSTL18_II | SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V | 0.70 | 0.84 | 0.97 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.70 | 0.84 | 0.97 | ns |
| SSTL18D_II | Differential SSTL_1.8 class II 8 mA drive | 0.70 | 0.84 | 0.97 | ns |
| SSTL15 | SSTL_1.5, VCCIO = 1.5 V | 1.22 | 1.35 | 1.48 | ns |
| SSTL15D | Differential SSTL_15 | 1.22 | 1.35 | 1.48 | ns |
| LVTTL33_4mA | LVTTL 4 mA drive, VCCIO = 3.3V | 0.25 | 0.24 | 0.23 | ns |
| LVTTL33_8mA | LVTTL 8 mA drive, VCCIO = 3.3V | –0.06 | –0.06 | –0.07 | ns |
| LVTTL33_12mA | LVTTL 12 mA drive, VCCIO = 3.3V | –0.01 | –0.02 | –0.02 | ns |
| LVTTL33_16mA | LVTTL 16 mA drive, VCCIO = 3.3V | –0.07 | –0.07 | –0.08 | ns |
| LVTTL33_20mA | LVTTL 20 mA drive, VCCIO = 3.3V | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4 mA drive, fast slew rate | 0.25 | 0.24 | 0.23 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8 mA drive, fast slew rate | –0.06 | –0.06 | –0.07 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12 mA drive, fast slew rate | –0.01 | –0.02 | –0.02 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16 mA drive, fast slew rate | –0.07 | –0.07 | –0.08 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4 mA drive, fast slew rate | 0.12 | 0.10 | 0.09 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8 mA drive, fast slew rate | –0.05 | –0.06 | –0.07 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12 mA drive, fast slew rate | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4 mA drive, fast slew rate | 0.11 | 0.12 | 0.14 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8 mA drive, fast slew rate | 0.11 | 0.12 | 0.14 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12 mA drive, fast slew rate | –0.04 | –0.03 | –0.03 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16 mA drive, fast slew rate | –0.04 | –0.03 | –0.03 | ns |

# PCI Express Electrical and Timing Characteristics

## AC and DC Characteristics

**Over Recommended Operating Conditions**

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Transmit**[1] | | | | | | |
| UI | Unit interval | | 399.88 | 400 | 400.12 | ps |
| $V_{TX-DIFF\_P-P}$ | Differential peak-to-peak output voltage | | 0.8 | 1.0 | 1.2 | V |
| $V_{TX-DE-RATIO}$ | De-emphasis differential output voltage ratio | | –3 | –3.5 | -4 | dB |
| $V_{TX-CM-AC\_P}$ | RMS AC peak common-mode output voltage | | — | — | 20 | mV |
| $V_{TX-RCV-DETECT}$ | Amount of voltage change allowed during receiver detection | | — | — | 600 | mV |
| $V_{TX-DC-CM}$ | Tx DC common mode voltage | | 0 | — | $V_{CCOB}$ + 5% | V |
| $I_{TX-SHORT}$ | Output short circuit current | $V_{TX-D+}$=0.0 V $V_{TX-D-}$=0.0 V | — | — | 90 | mA |
| $Z_{TX-DIFF-DC}$ | Differential output impedance | | 80 | 100 | 120 | Ohms |
| $RL_{TX-DIFF}$ | Differential return loss | | 10 | — | — | dB |
| $RL_{TX-CM}$ | Common mode return loss | | 6.0 | — | — | dB |
| $T_{TX-RISE}$ | Tx output rise time | 20 to 80% | 0.125 | — | — | UI |
| $T_{TX-FALL}$ | Tx output fall time | 20 to 80% | 0.125 | — | — | UI |
| $L_{TX-SKEW}$ | Lane-to-lane static output skew for all lanes in port/link | | — | — | 1.3 | ns |
| $T_{TX-EYE}$ | Transmitter eye width | | 0.75 | — | — | UI |
| $T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$ | Maximum time between jitter median and maximum deviation from median | | — | — | 0.125 | UI |
| **Receive**[1, 2] | | | | | | |
| UI | Unit Interval | | 399.88 | 400 | 400.12 | ps |
| $V_{RX-DIFF\_P-P}$ | Differential peak-to-peak input voltage | | 0.34[3] | — | 1.2 | V |
| $V_{RX-IDLE-DET-DIFF\_P-P}$ | Idle detect threshold voltage | | 65 | — | 340[3] | mV |
| $V_{RX-CM-AC\_P}$ | Receiver common mode voltage for AC coupling | | — | — | 150 | mV |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | | 80 | 100 | 120 | Ohms |
| $Z_{RX-DC}$ | DC input impedance | | 40 | 50 | 60 | Ohms |
| $Z_{RX-HIGH-IMP-DC}$ | Power-down DC input impedance | | 200K | — | — | Ohms |
| $RL_{RX-DIFF}$ | Differential return loss | | 10 | — | — | dB |
| $RL_{RX-CM}$ | Common mode return loss | | 6.0 | — | — | dB |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Maximum time required for receiver to recognize and signal an unexpected idle on link | | — | — | — | ms |

1. Values are measured at 2.5 Gbps.
2. Measured with external AC-coupling on the receiver.
3.Not in compliance with PCI Express 1.1 standard.

# Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-17. Transmit***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{RF}$ | Differential rise/fall time | 20%-80% | — | 80 | — | ps |
| $Z_{TX\_DIFF\_DC}$ | Differential impedance | | 80 | 100 | 120 | Ohms |
| $J_{TX\_DDJ}$[3, 4, 5] | Output data deterministic jitter | | — | — | 0.10 | UI |
| $J_{TX\_TJ}$[2, 3, 4, 5] | Total output data jitter | | — | — | 0.24 | UI |

1. Rise and fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

***Table 3-18. Receive and Jitter Tolerance***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RL_{RX\_DIFF}$ | Differential return loss | From 100 MHz to 1.25 GHz | 10 | — | — | dB |
| $RL_{RX\_CM}$ | Common mode return loss | From 100 MHz to 1.25 GHz | 6 | — | — | dB |
| $Z_{RX\_DIFF}$ | Differential termination resistance | | 80 | 100 | 120 | Ohms |
| $J_{RX\_DJ}$[1, 2, 3, 4, 5] | Deterministic jitter tolerance (peak-to-peak) | | — | — | 0.34 | UI |
| $J_{RX\_RJ}$[1, 2, 3, 4, 5] | Random jitter tolerance (peak-to-peak) | | — | — | 0.26 | UI |
| $J_{RX\_SJ}$[1, 2, 3, 4, 5] | Sinusoidal jitter tolerance (peak-to-peak) | | — | — | 0.11 | UI |
| $J_{RX\_TJ}$[1, 2, 3, 4, 5] | Total jitter tolerance (peak-to-peak) | | — | — | 0.71 | UI |
| $T_{RX\_EYE}$ | Receiver eye opening | | 0.29 | — | — | UI |

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

# LatticeECP3 sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

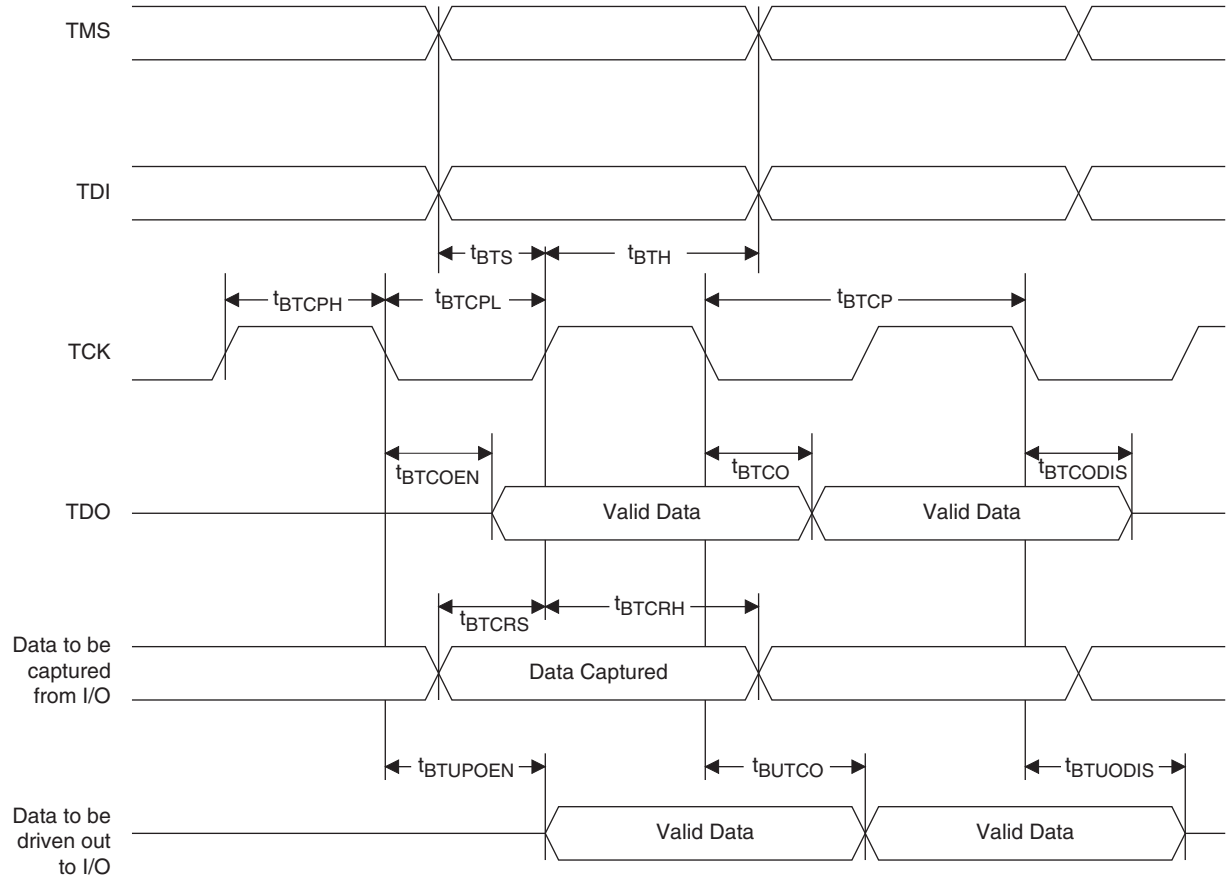
| Parameter | Description | | Min. | Max. | Units |
|---|---|---|---|---|---|
| **POR, Configuration Initialization, and Wakeup** | | | | | |
| $t_{ICFG}$ | Time from the Application of $V_{CC}$, $V_{CCAUX}$ or $V_{CCIO8}$* (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN | Master mode | — | 23 | ms |
| | | Slave mode | — | 6 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to the Valid Master MCLK | | — | 5 | µs |
| $t_{PRGM}$ | PROGRAMN Low Time to Start Configuration | | 25 | — | ns |
| $t_{PRGMRJ}$ | PROGRAMN Pin Pulse Rejection | | — | 10 | ns |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INITN Low | | — | 37 | ns |
| $t_{DPPDONE}$ | Delay Time from PROGRAMN Low to DONE Low | | — | 37 | ns |
| $t_{DINIT}$[1] | PROGRAMN High to INITN High Delay | | — | 1 | ms |
| $t_{MWC}$ | Additional Wake Master Clock Signals After DONE Pin is High | | 100 | 500 | cycles |
| $t_{CZ}$ | MCLK From Active To Low To High-Z | | — | 300 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | | — | 100 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | | — | 100 | ns |
| **All Configuration Modes** | | | | | |
| $t_{SUCDI}$ | Data Setup Time to CCLK/MCLK | | 5 | — | ns |
| $t_{HCDI}$ | Data Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{CODO}$ | CCLK/MCLK to DOUT in Flowthrough Mode | | -0.2 | 12 | ns |
| **Slave Serial** | | | | | |
| $t_{SSCH}$ | CCLK Minimum High Pulse | | 5 | — | ns |
| $t_{SSCL}$ | CCLK Minimum Low Pulse | | 5 | — | ns |
| $f_{CCLK}$ | CCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| **Master and Slave Parallel** | | | | | |
| $t_{SUCS}$ | CSN[1:0] Setup Time to CCLK/MCLK | | 7 | — | ns |
| $t_{HCS}$ | CSN[1:0] Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{SUWD}$ | WRITEN Setup Time to CCLK/MCLK | | 7 | — | ns |
| $t_{HWD}$ | WRITEN Hold Time to CCLK/MCLK | | 1 | — | ns |
| $t_{DCB}$ | CCLK/MCLK to BUSY Delay Time | | — | 12 | ns |
| $t_{CORD}$ | CCLK to Out for Read Data | | — | 12 | ns |
| $t_{BSCH}$ | CCLK Minimum High Pulse | | 6 | — | ns |
| $t_{BSCL}$ | CCLK Minimum Low Pulse | | 6 | — | ns |
| $t_{BSCYC}$ | Byte Slave Cycle Time | | 30 | — | ns |
| $f_{CCLK}$ | CCLK/MCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| **Master and Slave SPI** | | | | | |
| $t_{CFGX}$ | INITN High to MCLK Low | | — | 80 | ns |
| $t_{CSSPI}$ | INITN High to CSSPIN Low | | 0.2 | 2 | µs |
| $t_{SOCDO}$ | MCLK Low to Output Valid | | — | 15 | ns |
| $t_{CSPID}$ | CSSPIN[0:1] Low to First MCLK Edge Setup Time | | 0.3 | | µs |
| $f_{CCLK}$ | CCLK Frequency | Without encryption | — | 33 | MHz |
| | | With encryption | — | 20 | MHz |
| $t_{SSCH}$ | CCLK Minimum High Pulse | | 5 | — | ns |

# JTAG Port Timing Specifications

**Over Recommended Operating Conditions**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

***Figure 3-32. JTAG Port Timing Waveforms***



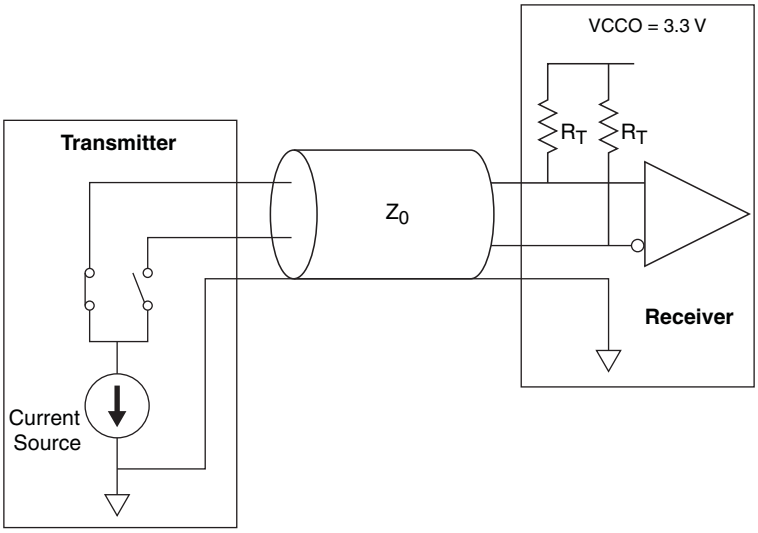
# sysI/O Differential Electrical Characteristics

## Transition Reduced LVDS (TRLVDS DC Specification)

**Over Recommended Operating Conditions**

| Symbol | Description | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCO}$ | Driver supply voltage (+/– 5%) | 3.14 | 3.3 | 3.47 | V |
| $V_{ID}$ | Input differential voltage | 150 | — | 1200 | mV |
| $V_{ICM}$ | Input common mode voltage | 3 | — | 3.265 | V |
| $V_{CCO}$ | Termination supply voltage | 3.14 | 3.3 | 3.47 | V |
| $R_T$ | Termination resistance (off-chip) | 45 | 50 | 55 | Ohms |

Note: LatticeECP3 only supports the TRLVDS receiver.




## Mini LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $Z_O$ | Single-ended PCB trace impedance | 30 | 50 | 75 | Ohms |
| $R_T$ | Differential termination resistance | 50 | 100 | 150 | Ohms |
| $V_{OD}$ | Output voltage, differential, $\|V_{OP} - V_{OM}\|$ | 300 | — | 600 | mV |
| $V_{OS}$ | Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$ | 1 | 1.2 | 1.4 | V |
| $\Delta V_{OD}$ | Change in $V_{OD}$, between H and L | — | — | 50 | mV |
| $\Delta V_{ID}$ | Change in $V_{OS}$, between H and L | — | — | 50 | mV |
| $V_{THD}$ | Input voltage, differential, $\|V_{INP} - V_{INM}\|$ | 200 | — | 600 | mV |
| $V_{CM}$ | Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$ | $0.3+(V_{THD}/2)$ | — | $2.1-(V_{THD}/2)$ | |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | — | 550 | ps |
| $T_{ODUTY}$ | Output clock duty cycle | 40 | — | 60 | % |

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

## Point-to-Point LVDS (PPLVDS)

**Over Recommended Operating Conditions**

| Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Output driver supply (+/– 5%) | 3.14 | 3.3 | 3.47 | V |
| | 2.25 | 2.5 | 2.75 | V |
| Input differential voltage | 100 | — | 400 | mV |
| Input common mode voltage | 0.2 | — | 2.3 | V |
| Output differential voltage | 130 | — | 400 | mV |
| Output common mode voltage | 0.5 | 0.8 | 1.4 | V |

## RSDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OD}$ | Output voltage, differential, $R_T$ = 100 Ohms | 100 | 200 | 600 | mV |
| $V_{OS}$ | Output voltage, common mode | 0.5 | 1.2 | 1.5 | V |
| $I_{RSDS}$ | Differential driver output current | 1 | 2 | 6 | mA |
| $V_{THD}$ | Input voltage differential | 100 | — | — | mV |
| $V_{CM}$ | Input common mode voltage | 0.3 | — | 1.5 | V |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | 500 | — | ps |
| $T_{ODUTY}$ | Output clock duty cycle | 35 | 50 | 65 | % |

Note: Data is for 2 mA drive. Other differential driver current options are available.

## Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software