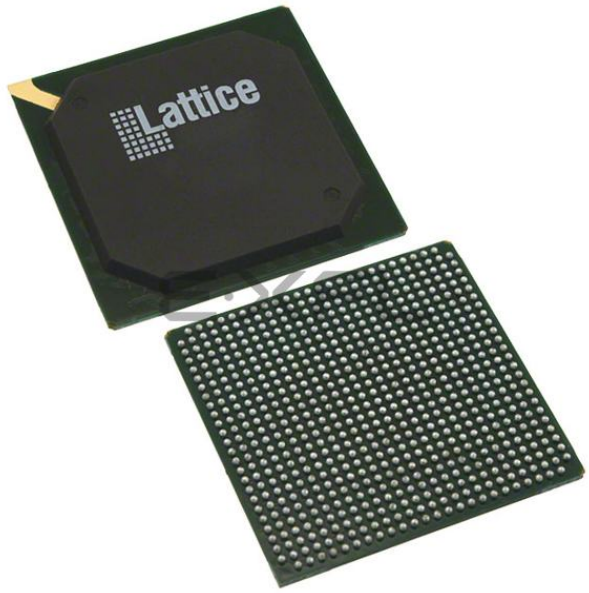
Lattice Semiconductor Corporation - LFE3-35EA-8LFN672I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

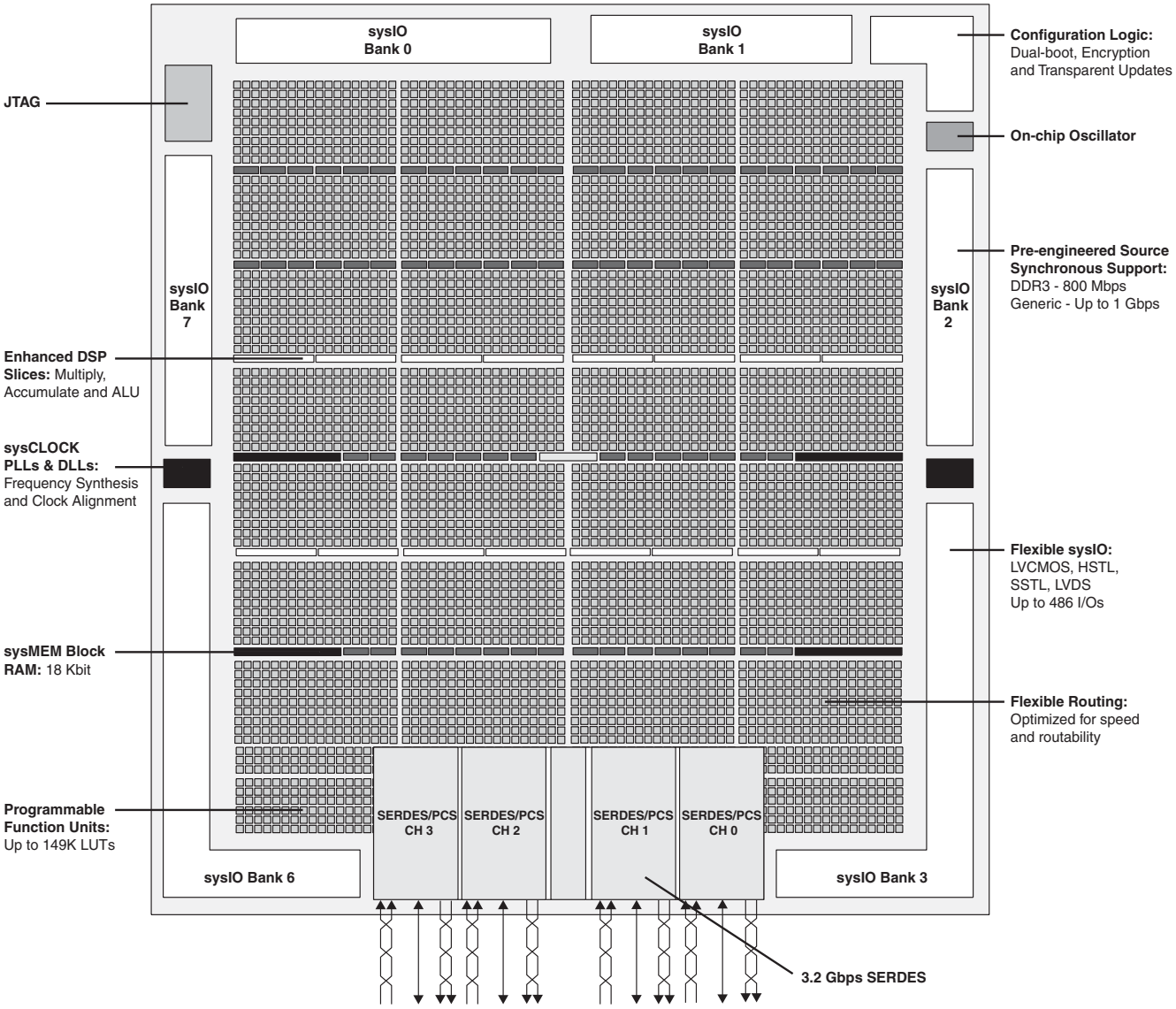
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	33000
Total RAM Bits	1358848
Number of I/O	310
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-8lfn672i

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

Table 2-5. DLL Signals

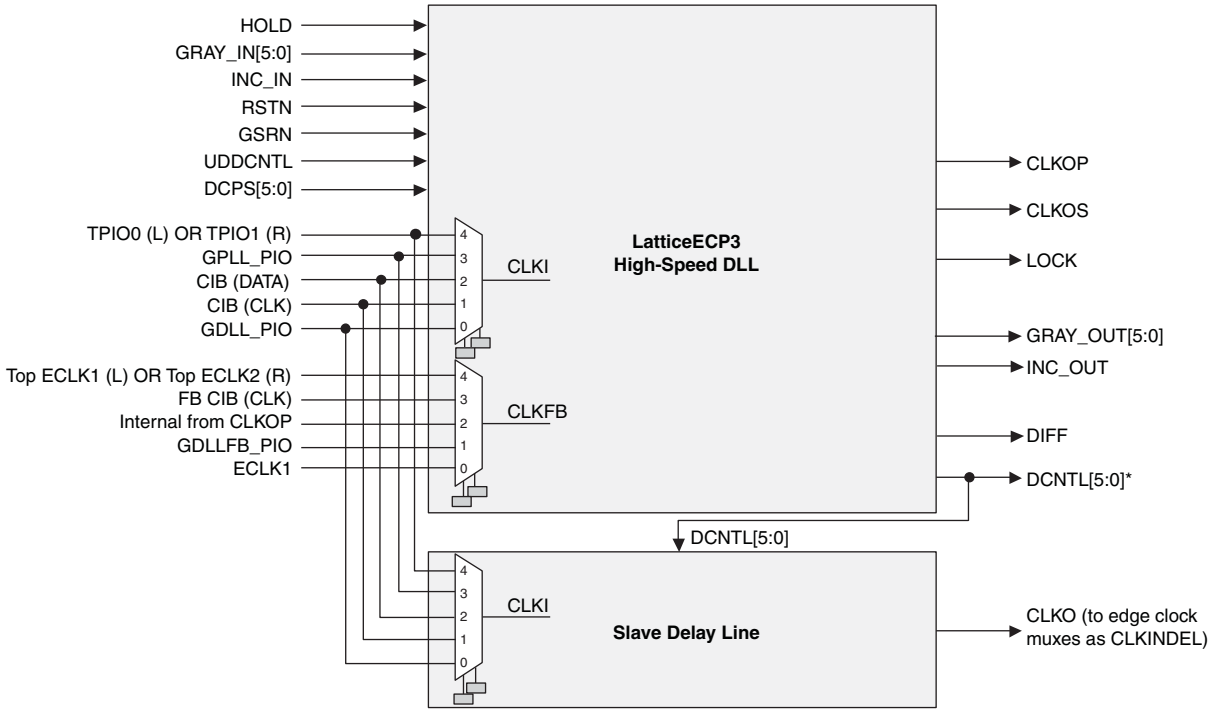
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



* This signal is not user accessible. It can only be used to feed the slave delay line.

PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

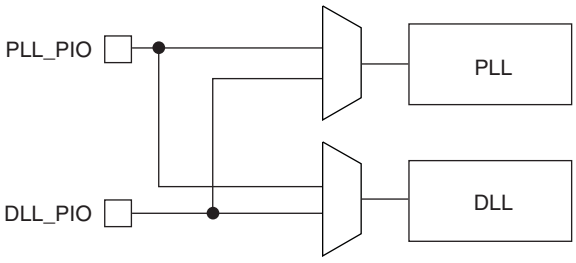
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.

The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

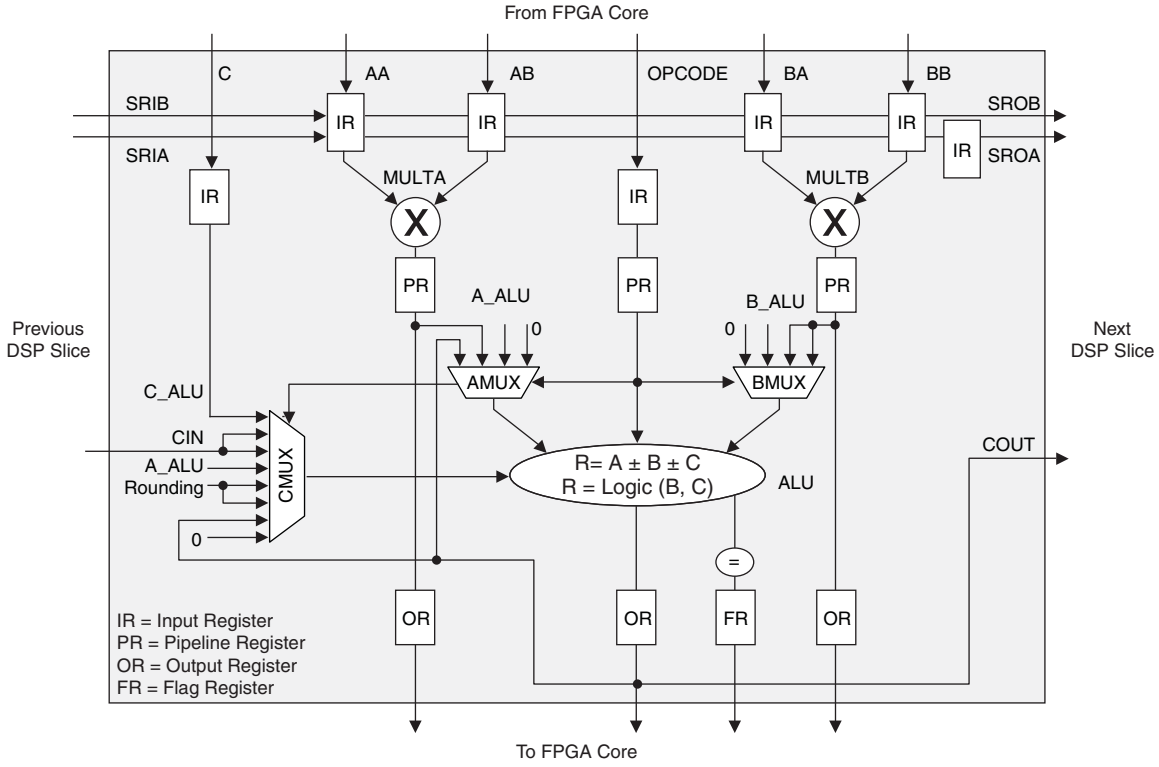
RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

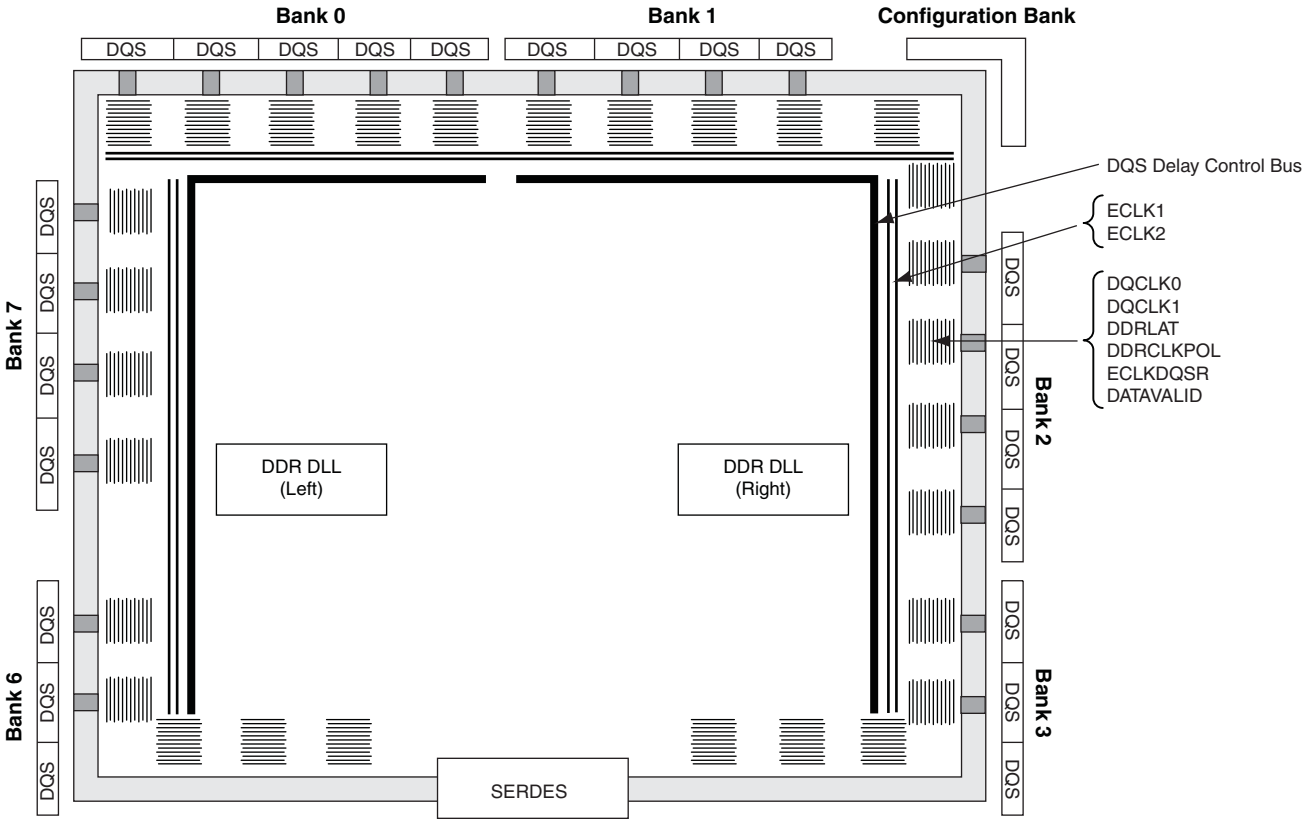
Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



*Includes shared configuration I/Os and dedicated configuration I/Os.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[4]	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)	—	—	+/–1	mA
IDK[5]	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$	—	—	+/–1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5V	—	18	—	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the LatticeECP3 Product Family Qualification Summary for complete qualification data, including ESD performance.

RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

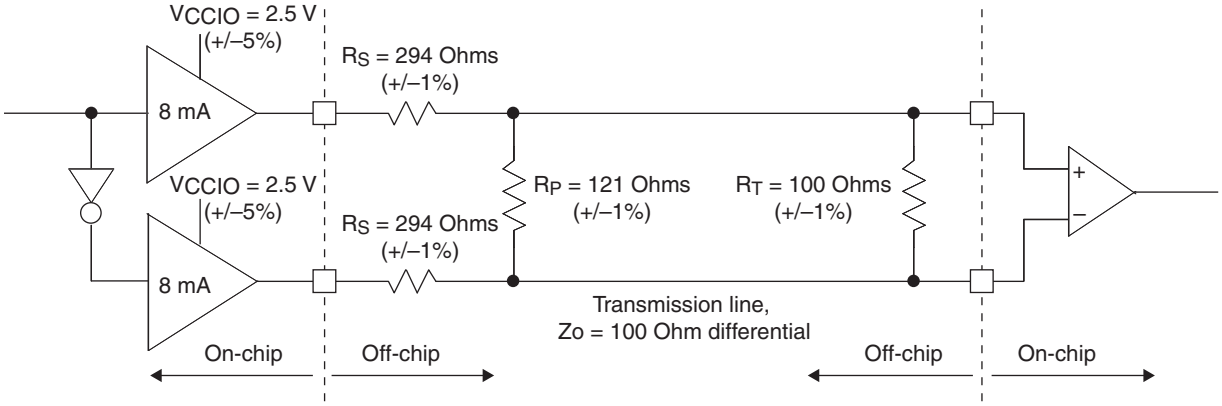


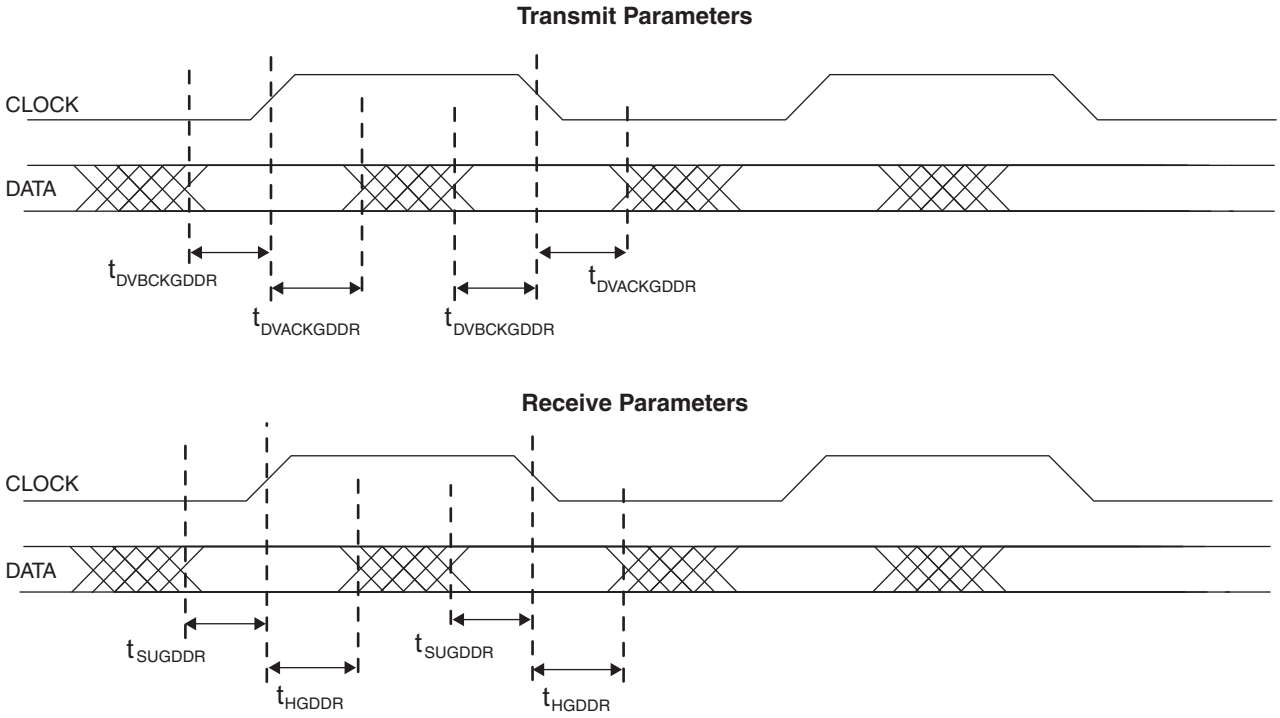
Table 3-4. RSDS25E DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	294	Ω
R_P	Driver Parallel Resistor (+/–1%)	121	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

Figure 3-8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)



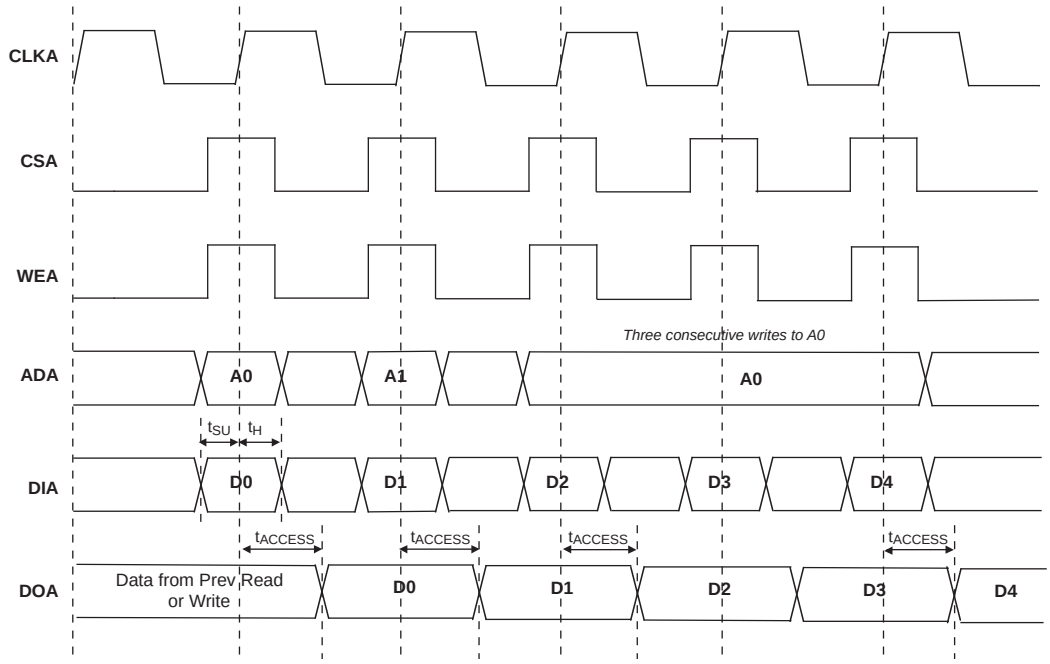
LatticeECP3 Internal Switching Characteristics[1, 2, 5] (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	–8		–7		–6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141	—	0.145	—	0.149	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087	—	0.096	—	0.104	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	–0.066	—	–0.080	—	–0.094	—	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	–0.071	—	–0.070	—	–0.068	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118	—	0.098	—	0.077	—	ns
DSP Block Timing[3]								
t_{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	–0.17	—	–0.19	—	–0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	–1.02	—	–1.09	—	–1.15	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t_{HO_DSP}	Output Register Hold Time	–1.67	—	–1.76	—	–1.84	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.05	—	3.35	—	3.73	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	–0.20	—	–0.24	—	–0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69	—	1.94	—	2.14	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	–0.58	—	–0.80	—	–0.97	—	ns

1. Internal parameters are characterized but not tested on every device.
2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.
4. The output register is in Flip-flop mode.
5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

SERDES/PCS Block Latency

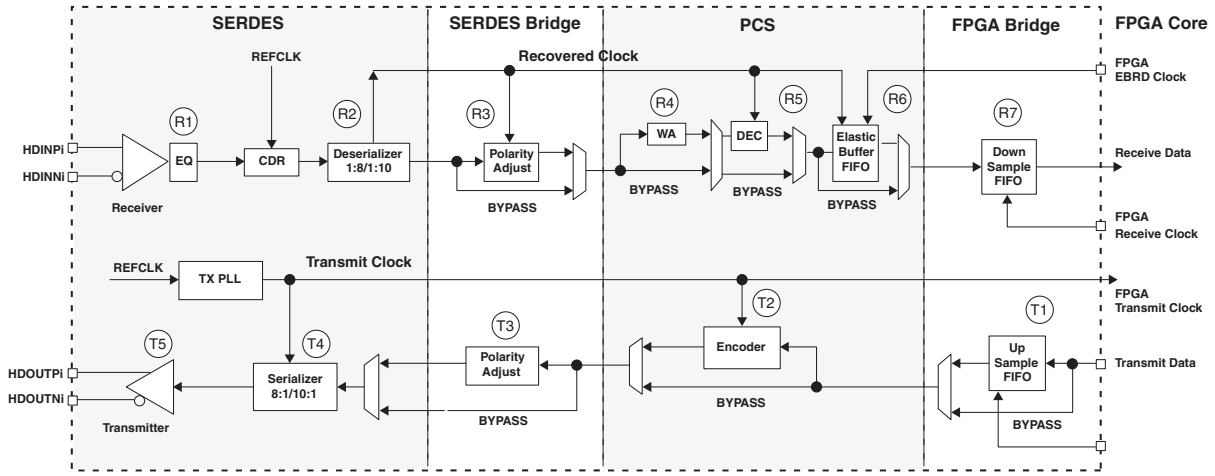
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms

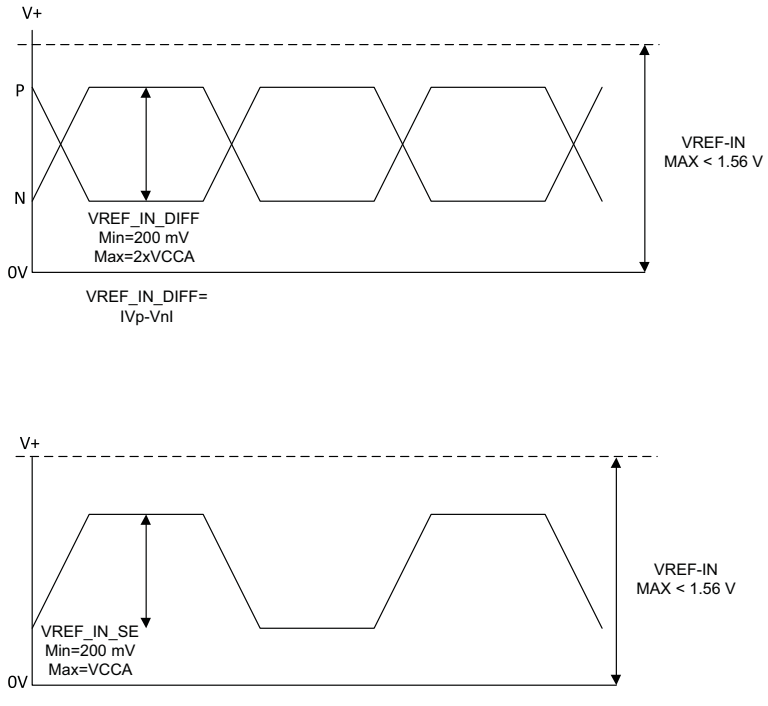
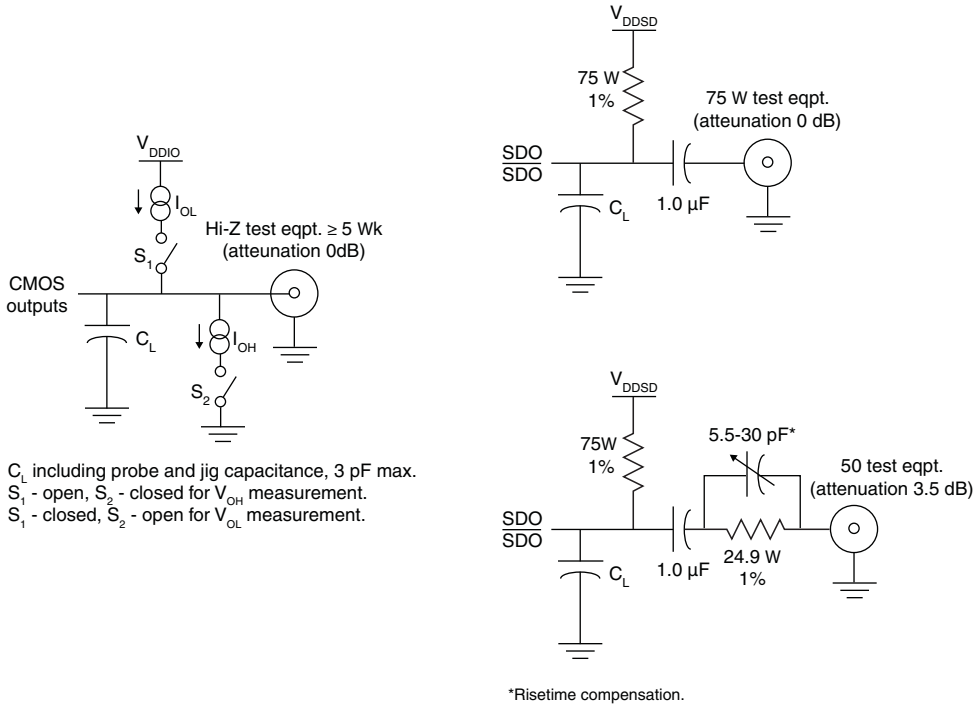


Figure 3-19. Test Loads

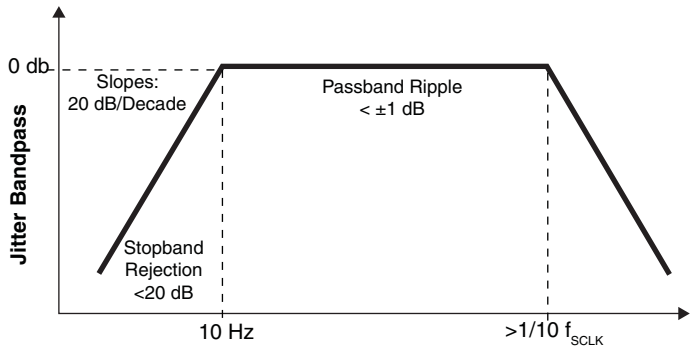
Test Loads



C_L including probe and jig capacitance, 3 pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

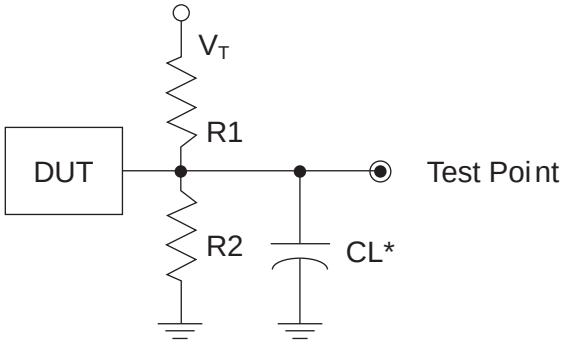
Timing Jitter Bandpass



Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0 pF	V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Pin Information Summary

Pin Information Summary		ECP3-17EA			ECP3-35EA			ECP3-70EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	20	36	26	42	48	42	60	86
	Bank 1	14	10	24	14	36	36	36	48	78
	Bank 2	6	7	12	6	24	24	24	34	36
	Bank 3	18	12	44	16	54	59	54	59	86
	Bank 6	20	11	44	18	63	61	63	67	86
	Bank 7	19	26	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4	4	8	8
	Bank 3	0	0	0	2	4	4	4	12	12
	Bank 6	0	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310	295	380	490
VCC		6	16	16	6	16	32	16	32	32
VCCAUX		4	5	8	4	8	12	8	12	16
VTT		4	7	4	4	4	4	4	4	8
VCCA		4	6	4	4	4	8	4	8	16
VCCPLL		2	2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	3	2	2	2	4	2	4	4
	Bank 1	2	3	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	2	4	2	4	4
	Bank 3	2	3	2	2	2	4	2	4	4
	Bank 6	2	3	2	2	2	4	2	4	4
	Bank 7	2	3	2	2	2	4	2	4	4
	Bank 8	1	2	2	1	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139	98	139	233
NC		0	0	73	0	0	96	0	0	238
Reserved[1]		0	0	2	0	2	2	2	2	2
SERDES		26	18	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672	484	672	1156

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank[2]	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43
	Bank 1	18	24	39
	Bank 2	8	12	13
	Bank 3	20	23	33
	Bank 6	22	25	33
	Bank 7	11	16	18
	Bank 8	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0
	Bank 1	0	0	0
	Bank 2	6	9	9
	Bank 3	9	12	16
	Bank 6	11	14	16
	Bank 7	9	12	13
	Bank 8	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49
	Bank 6	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12
DDR Groups Bonded per Bank[1]	Bank 0	3	5	7
	Bank 1	3	4	7
	Bank 2	2	3	3
	Bank 3	3	4	5
	Bank 6	4	4	5
	Bank 7	3	4	4
	Configuration Bank 8	0	0	0
SERDES Quads		1	2	3

1. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.