Lattice Semiconductor Corporation - LFE3-35EA-9FN484C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Not For New Designs
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	33000
Total RAM Bits	1358848
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-9fn484c

LatticeECP3 Family Data Sheet Introduction

February 2012 Data Sheet DS1021

Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP3 Family Data Sheet Architecture

June 2013 Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

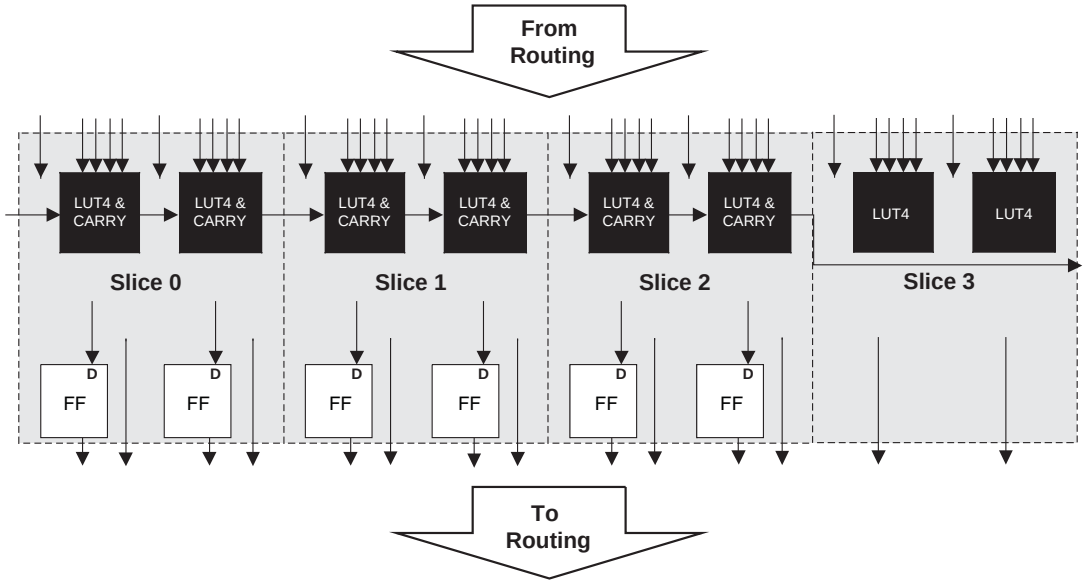
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

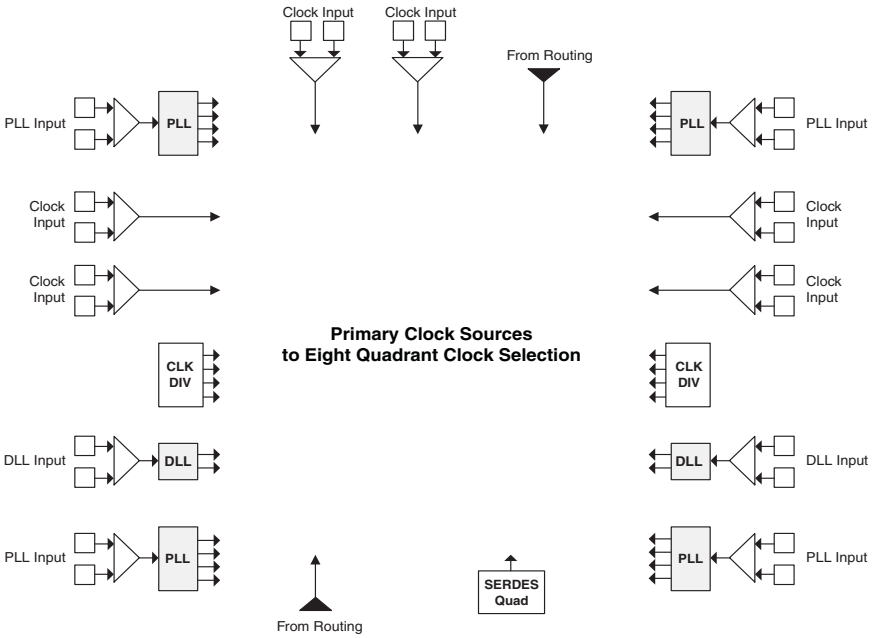
Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

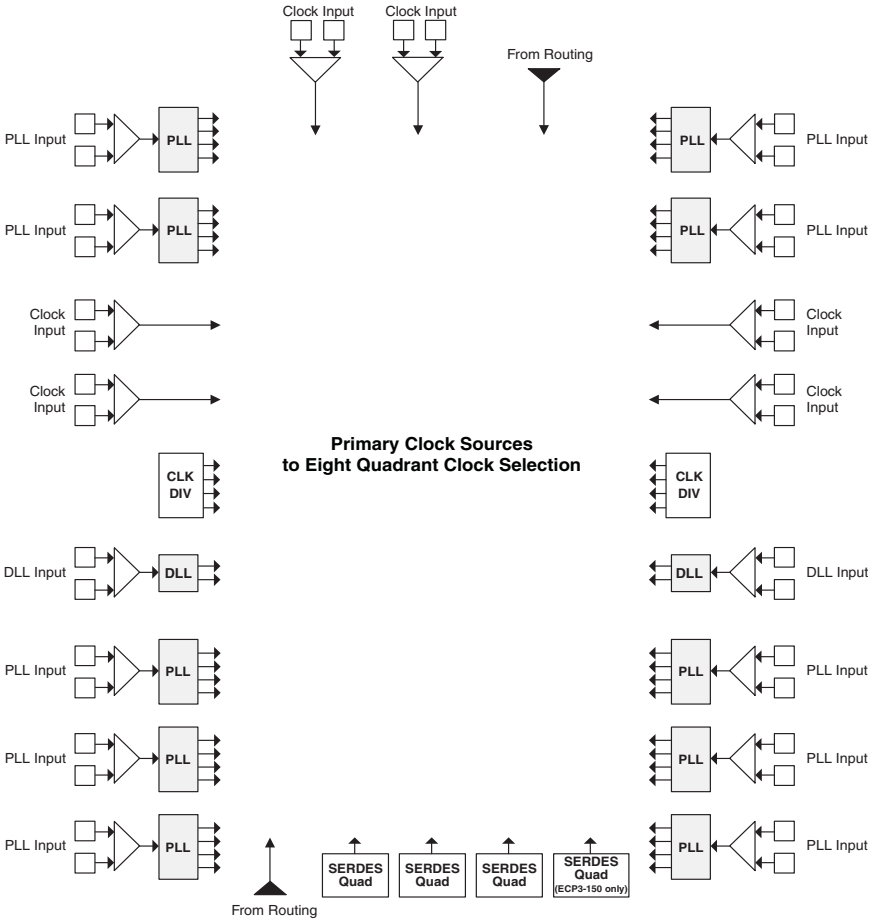
Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Figure 2-10. Primary Clock Sources for LatticeECP3-35



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150



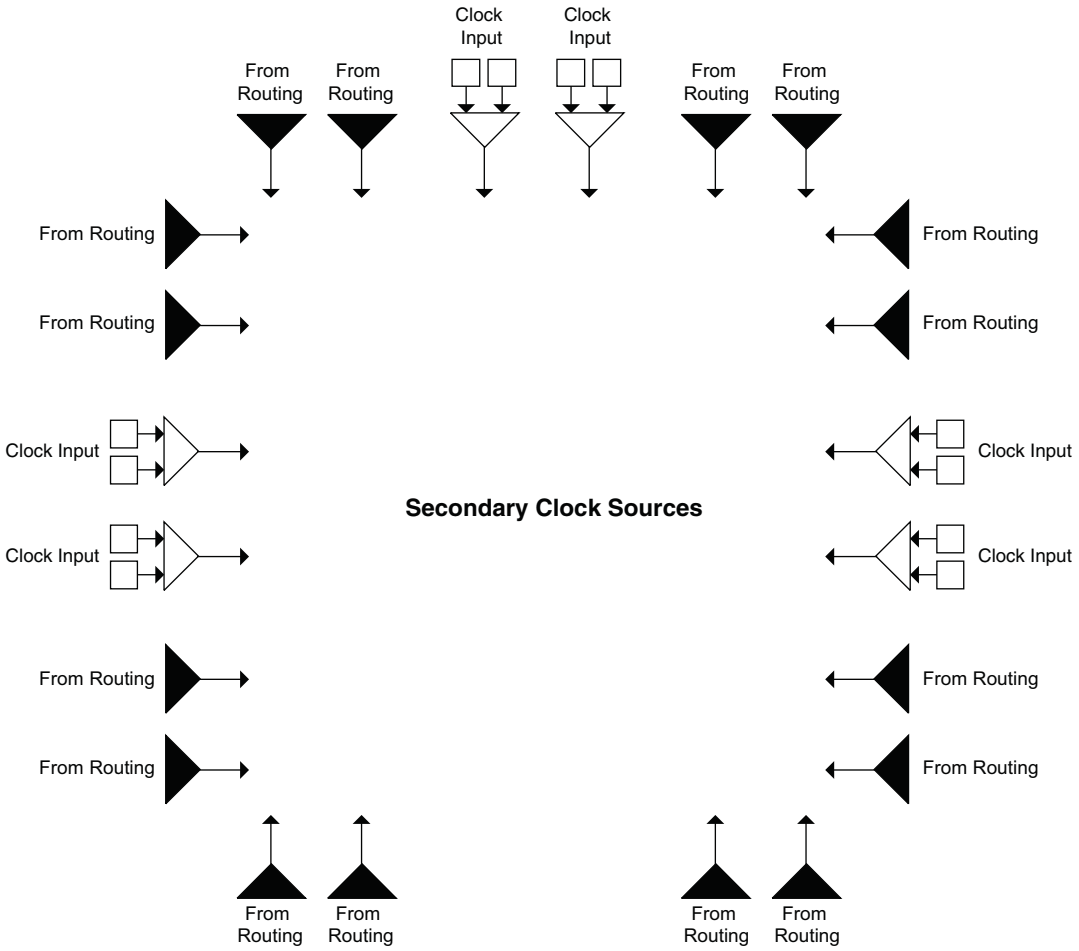
Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

Figure 2-14. Secondary Clock Sources



Note: Clock inputs can be configured in differential or single-ended mode.

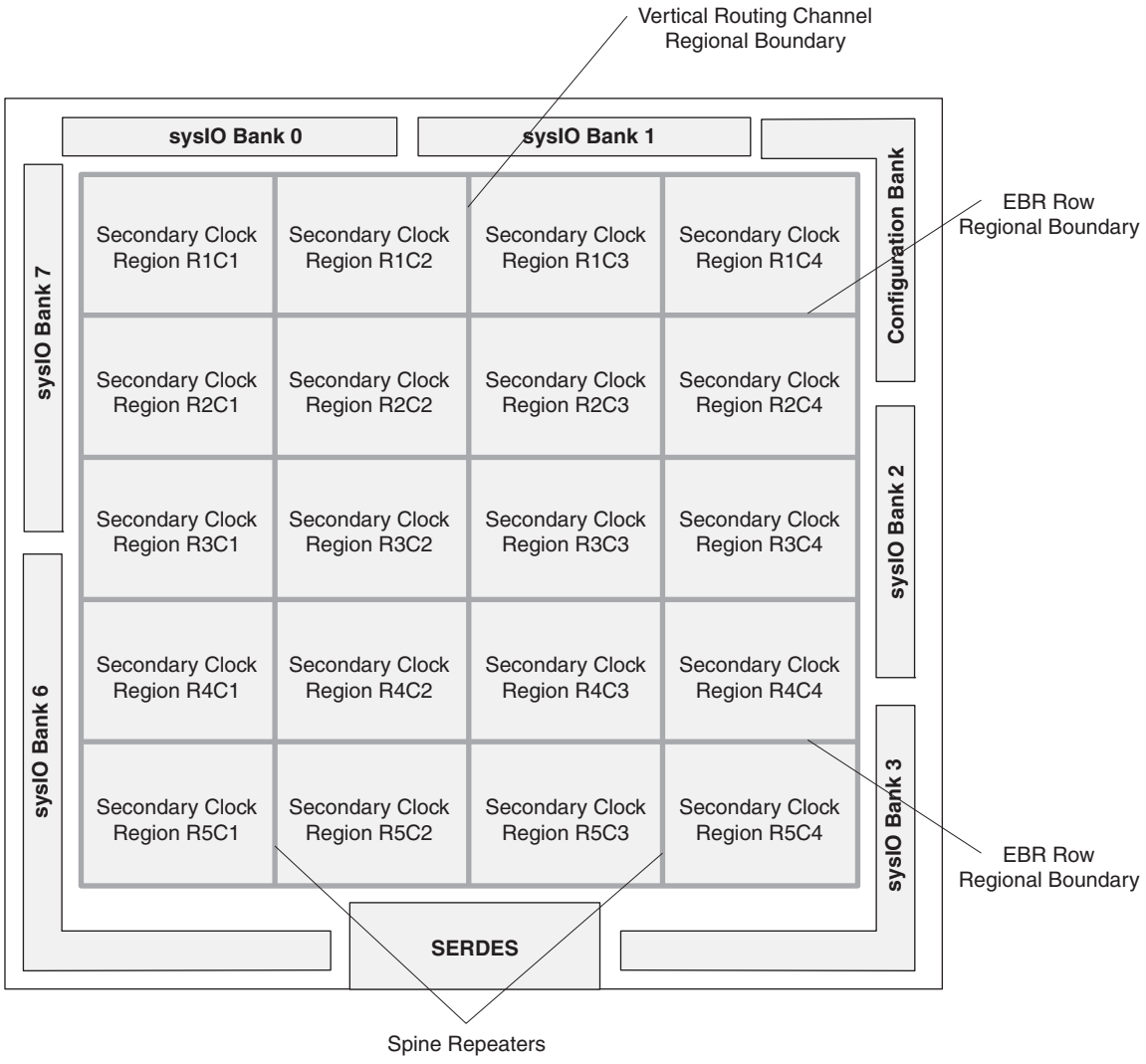
Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}[1], V_{INM}[1]	Input Voltage		0	—	2.4	V
V_{CM}[1]	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/–100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/–10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

1, On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LatticeECP3 Internal Switching Characteristics[1, 2, 5] (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	–8		–7		–6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141	—	0.145	—	0.149	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087	—	0.096	—	0.104	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	–0.066	—	–0.080	—	–0.094	—	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	–0.071	—	–0.070	—	–0.068	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118	—	0.098	—	0.077	—	ns
DSP Block Timing[3]								
t_{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	–0.17	—	–0.19	—	–0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	–1.02	—	–1.09	—	–1.15	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t_{HO_DSP}	Output Register Hold Time	–1.67	—	–1.76	—	–1.84	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.05	—	3.35	—	3.73	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	–0.20	—	–0.24	—	–0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69	—	1.94	—	2.14	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	–0.58	—	–0.80	—	–0.97	—	ns

1. Internal parameters are characterized but not tested on every device.
2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.
4. The output register is in Flip-flop mode.
5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.

LatticeECP3 Maximum I/O Buffer Speed (Continued)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
PCI33	PCI, V_{CCIO} = 3.3 V	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f_{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock[4]	2	—	420	MHz
f_{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock[4]	4	—	420	MHz
f_{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f_{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f_{VCO}	PLL VCO frequency			500	—	1000	MHz
f_{PFD}[3]	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock[4]	2	—	420	MHz
AC Characteristics							
t_{PA}	Programmable delay unit			65	130	260	ps
t_{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		$f_{OUT} \leq 250$ MHz	Primary clock	45	50	55	%
		$f_{OUT} > 250$ MHz	Primary clock	30	50	70	%
t_{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t_{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t_{OPJIT}[1]	Output clock period jitter	$f_{OUT} \geq 420$ MHz		—	—	200	ps
		420 MHz > $f_{OUT} \geq 100$ MHz		—	—	250	ps
		$f_{OUT} < 100$ MHz		—	—	0.025	UIPP
t_{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps
t_{LOCK}[2]	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t_{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t_{HI}	Input clock high time	90% to 90%		0.5	—	—	ns
t_{LO}	Input clock low time	10% to 10%		0.5	—	—	ns
t_{IPJIT}	Input clock period jitter			—	—	400	ps
t_{RST}	Reset signal pulse width high, RSTK			10	—	—	ns
	Reset signal pulse width high, RST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}[1]	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[3, 4, 5]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[2, 3, 4, 5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[2, 3, 4, 5]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[2, 3, 4, 5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4, 5]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDO}	Serial data rate		270	—	2975	Mbps
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [1, 2]	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

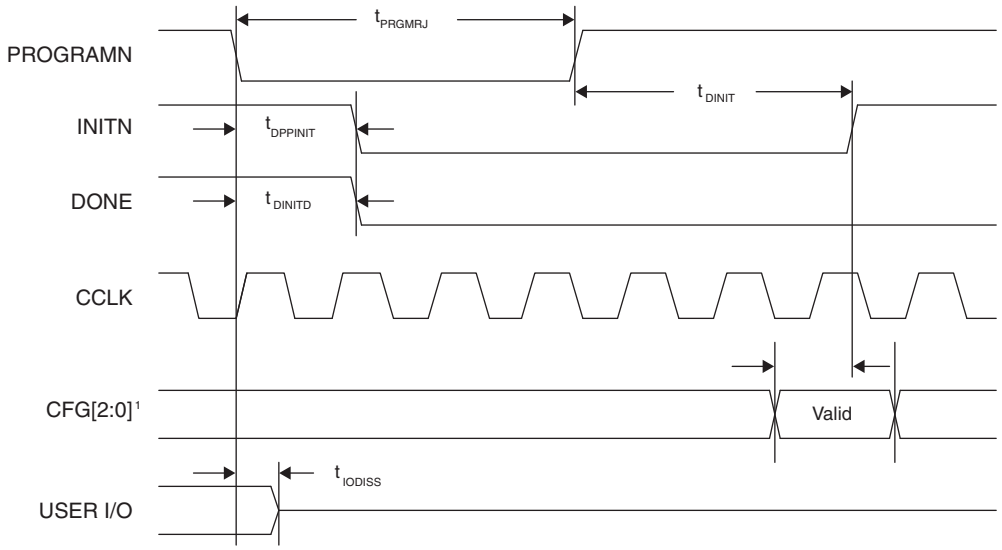
Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

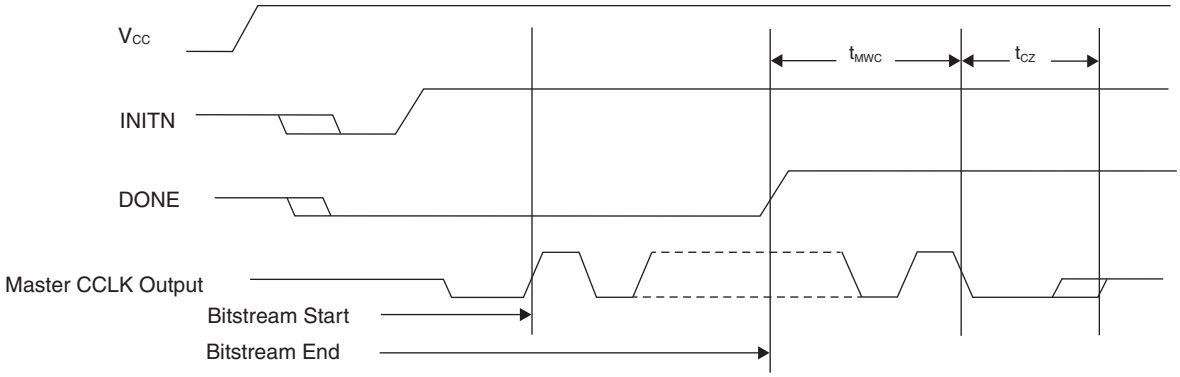
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC_V	Duty cycle, video clock		45	50	55	%

Figure 3-26. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-27. Wake-Up Timing



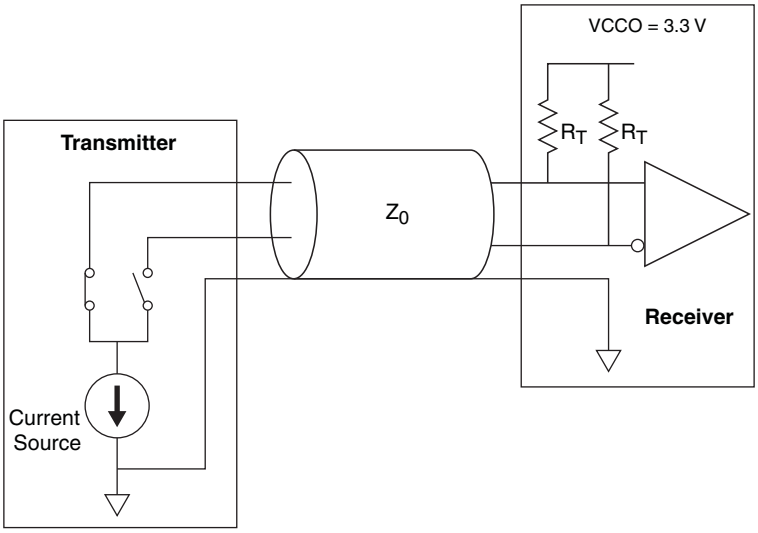
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/– 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals[3]		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	O	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	O	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	30	47
	Bank 1	18	24	39	24	43
	Bank 2	8	12	13	12	18
	Bank 3	20	23	33	23	37
	Bank 6	22	25	33	25	37
	Bank 7	11	16	18	16	24
	Bank 8	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	6	9	9	9	15
	Bank 3	9	12	16	12	21
	Bank 6	11	14	16	14	21
	Bank 7	9	12	13	12	18
	Bank 8	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	60/30	94/47
	Bank 1	36/18	48/24	78/39	48/24	86/43
	Bank 2	28/14	42/21	44/22	42/21	66/33
	Bank 3	58/29	71/35	98/49	71/35	116/58
	Bank 6	67/33	78/39	98/49	78/39	116/58
	Bank 7	40/20	56/28	62/31	56/28	84/42
	Bank 8	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	5	7
	Bank 1	3	4	7	4	7
	Bank 2	2	3	3	3	4
	Bank 3	3	4	5	4	7
	Bank 6	4	4	5	4	7
	Bank 7	3	4	4	4	6
	Configuration Bank8	0	0	0	0	0
SERDES Quads		1	2	3	2	4

1.These pins must remain floating on the board.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.