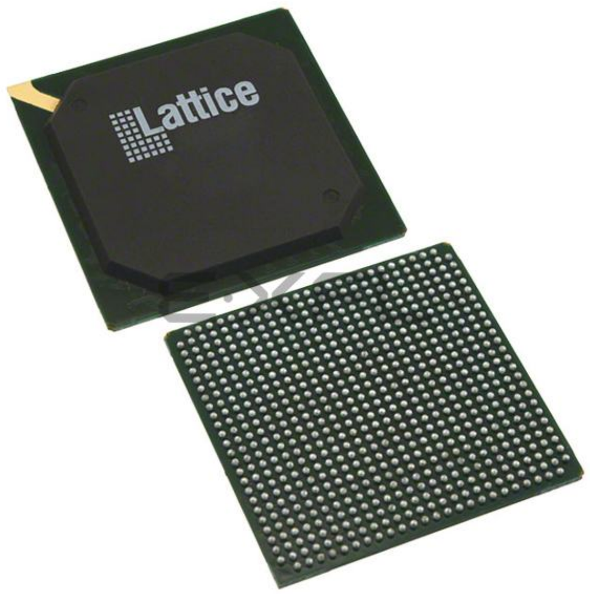

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Number of LABs/CLBs | 4125 |
| Number of Logic Elements/Cells | 33000 |
| Total RAM Bits | 1358848 |
| Number of I/O | 310 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-35ea-9fn672c |

# LatticeECP3 Family Data Sheet Architecture

June 2013 | Data Sheet DS1021

## Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

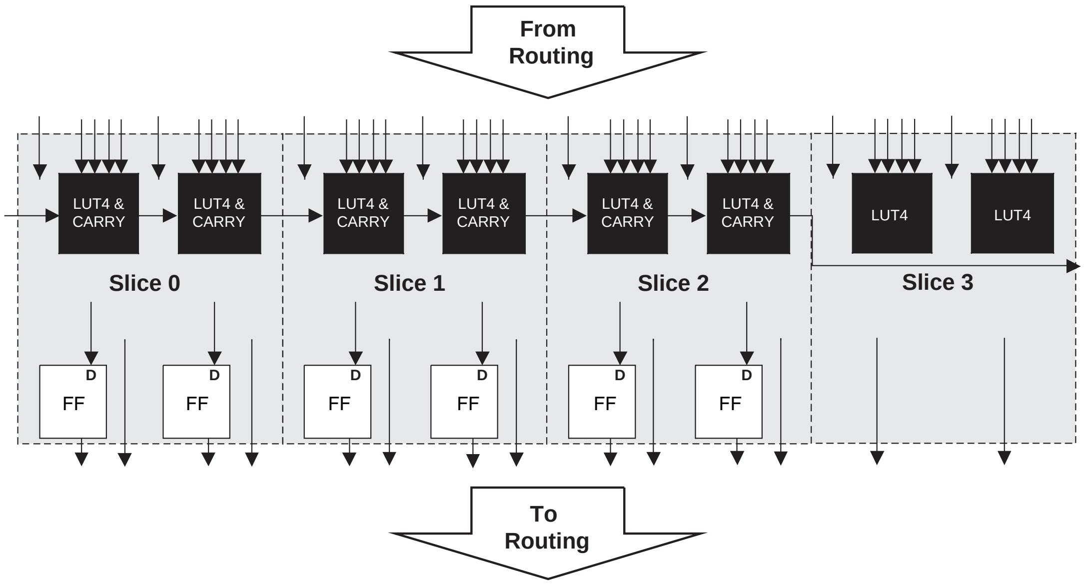
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

*Figure 2-2. PFU Diagram*




## Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

***Table 2-1. Resources and Modes Available per Slice***

| Slice | PFU BLock | | PFF Block | |
|---|---|---|---|---|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s | Logic, ROM | 2 LUT4s | Logic, ROM |

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

**ROM Mode**

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

## Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

## sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

### General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

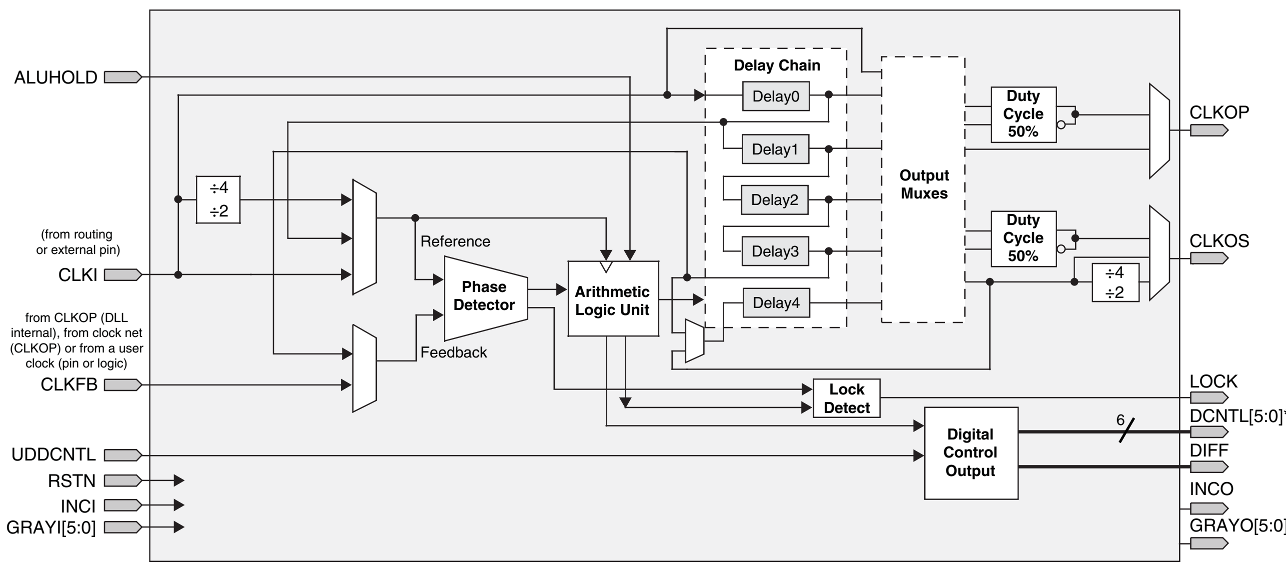
The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

***Figure 2-5. Delay Locked Loop Diagram (DLL)***

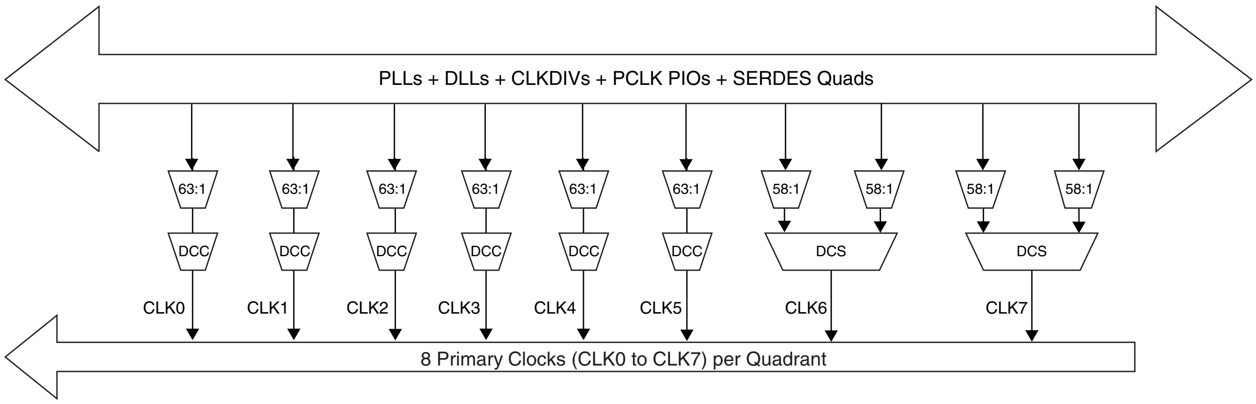



* This signal is not user accessible. This can only be used to feed the slave delay line.

## Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

*Figure 2-12. Per Quadrant Primary Clock Selection*




## Dynamic Clock Control (DCC)

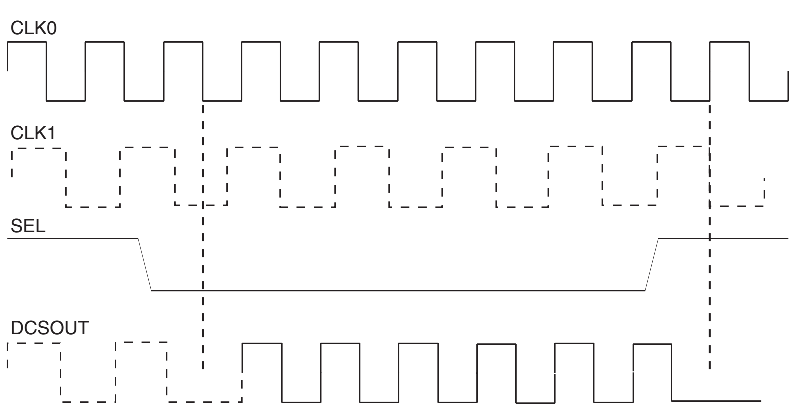
The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

*Figure 2-13. DCS Waveforms*



## Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

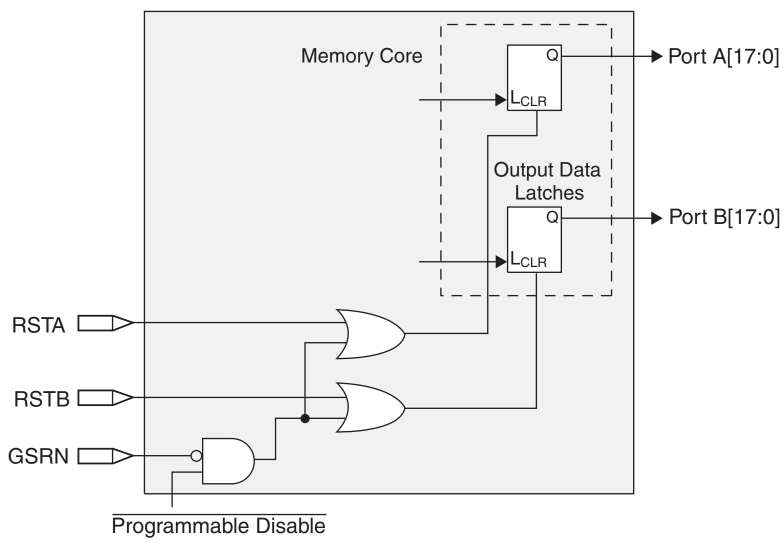
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

***Figure 2-22. Memory Core Reset***




For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

# sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

## sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

as, overflow, underflow and convergent rounding, etc.
— Flexible cascading across slices to get larger functions

- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-24, the LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2™ sysDSP block, such that, legacy applications can be targeted to the LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LatticeECP3 sysDSP slices, as shown in Figure 2-25.

***Figure 2-24. Simplified sysDSP Slice Block Diagram***

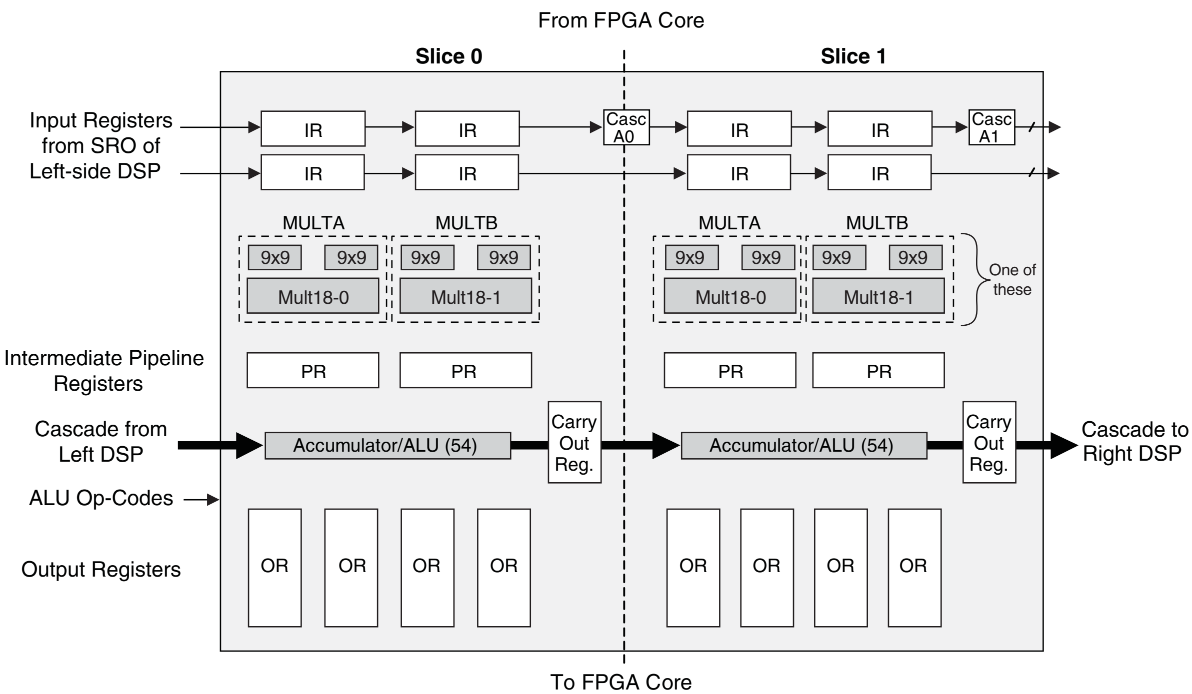
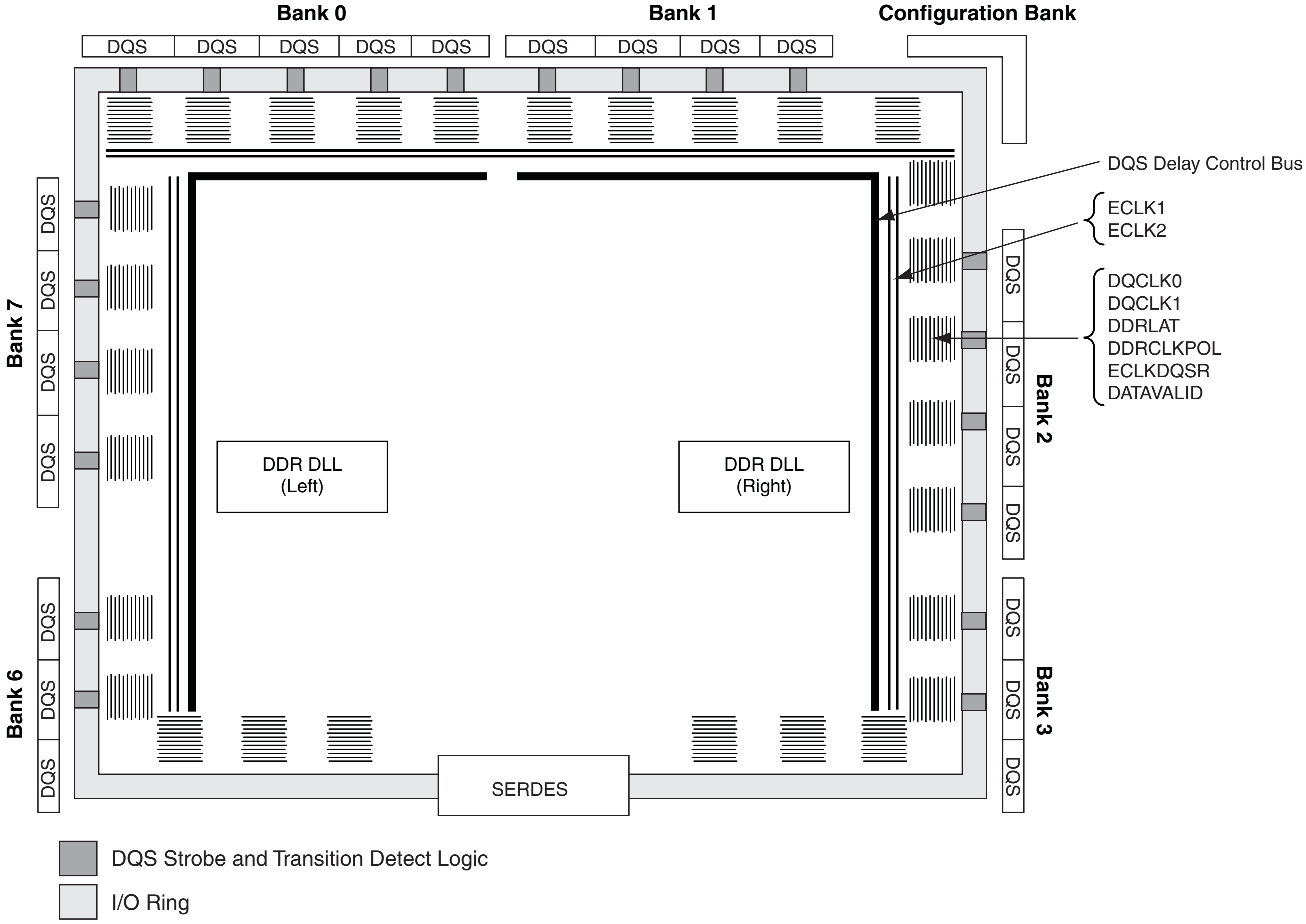


*Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution*




*Includes shared configuration I/Os and dedicated configuration I/Os.

## BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS25 Multi-point Output Example***

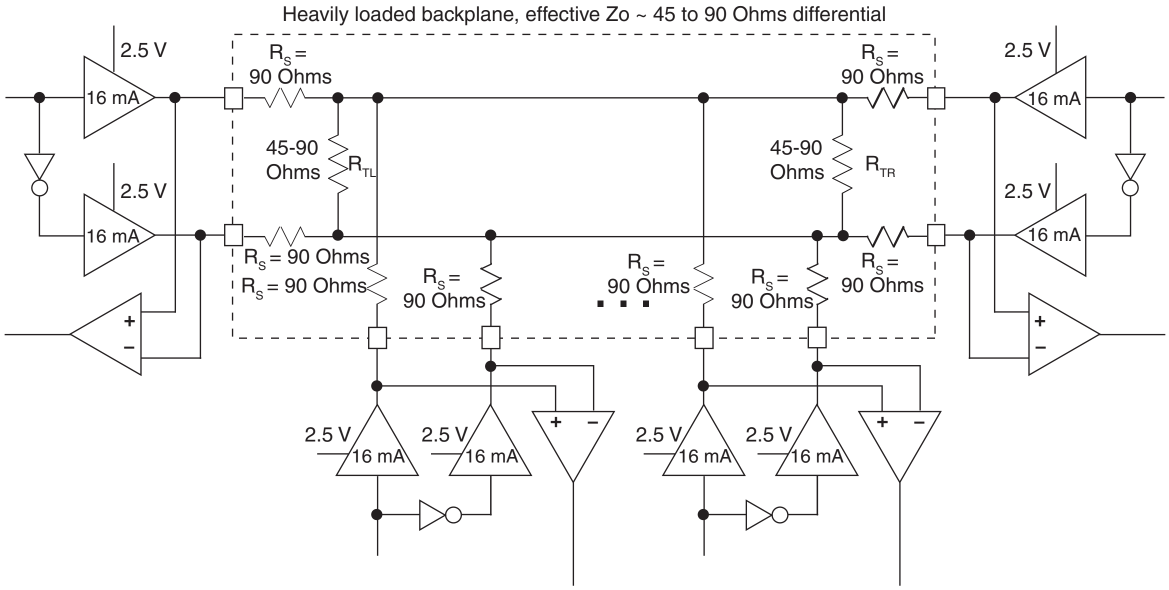



***Table 3-2. BLVDS25 DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45Ω | Zo = 90Ω | |
| $V_{CCIO}$ | Output Driver Supply (+/– 5%) | 2.50 | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 10.00 | 10.00 | Ω |
| $R_S$ | Driver Series Resistor (+/– 1%) | 90.00 | 90.00 | Ω |
| $R_{TL}$ | Driver Parallel Resistor (+/– 1%) | 45.00 | 90.00 | Ω |
| $R_{TR}$ | Receiver Termination (+/– 1%) | 45.00 | 90.00 | Ω |
| $V_{OH}$ | Output High Voltage | 1.38 | 1.48 | V |
| $V_{OL}$ | Output Low Voltage | 1.12 | 1.02 | V |
| $V_{OD}$ | Output Differential Voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC Output Current | 11.24 | 10.20 | mA |

1. For input buffer, see LVDS table.

# SERDES/PCS Block Latency

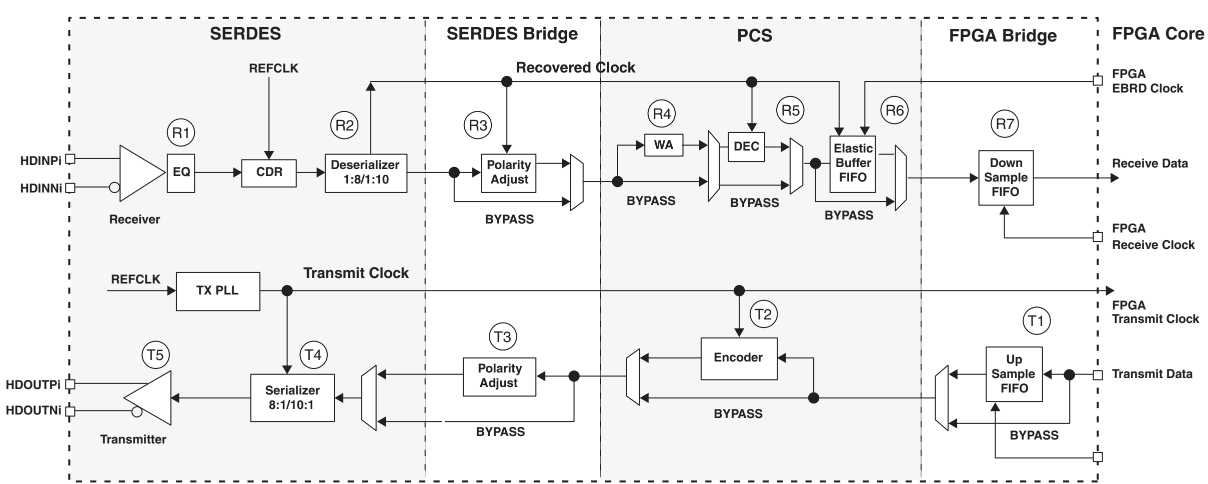
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

*Table 3-8. SERDES/PCS Latency Breakdown*

| Item | Description | Min. | Avg. | Max. | Fixed | Bypass | Units |
|---|---|---|---|---|---|---|---|
| **Transmit Data Latency[1]** | | | | | | | |
| T1 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |
| T2 | 8b10b Encoder | — | — | — | 2 | 1 | word clk |
| T3 | SERDES Bridge transmit | — | — | — | 2 | 1 | word clk |
| T4 | Serializer: 8-bit mode | — | — | — | 15 + Δ1 | — | UI + ps |
| | Serializer: 10-bit mode | — | — | — | 18 + Δ1 | — | UI + ps |
| T5 | Pre-emphasis ON | — | — | — | 1 + Δ2 | — | UI + ps |
| | Pre-emphasis OFF | — | — | — | 0 + Δ3 | — | UI + ps |
| **Receive Data Latency[2]** | | | | | | | |
| R1 | Equalization ON | — | — | — | Δ1 | — | UI + ps |
| | Equalization OFF | — | — | — | Δ2 | — | UI + ps |
| R2 | Deserializer: 8-bit mode | — | — | — | 10 + Δ3 | — | UI + ps |
| | Deserializer: 10-bit mode | — | — | — | 12 + Δ3 | — | UI + ps |
| R3 | SERDES Bridge receive | — | — | — | 2 | — | word clk |
| R4 | Word alignment | 3.1 | — | 4 | — | — | word clk |
| R5 | 8b10b decoder | — | — | — | 1 | — | word clk |
| R6 | Clock Tolerance Compensation | 7 | 15 | 23 | 1 | 1 | word clk |
| R7 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

*Figure 3-12. Transmitter and Receiver Latency Block Diagram*



# SERDES High Speed Data Receiver

*Table 3-9. Serial Input Data Specifications*

| Symbol | Description | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RX\text{-}CID_S$ | Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ $10^{-12}$ BER | 3.125 G | — | — | 136 | Bits |
| | | 2.5 G | — | — | 144 | |
| | | 1.485 G | — | — | 160 | |
| | | 622 M | — | — | 204 | |
| | | 270 M | — | — | 228 | |
| | | 150 M | — | — | 296 | |
| $V_{RX\text{-}DIFF\text{-}S}$ | Differential input sensitivity | | 150 | — | 1760 | mV, p-p |
| $V_{RX\text{-}IN}$ | Input levels | | 0 | — | $V_{CCA}$ +0.5[4] | V |
| $V_{RX\text{-}CM\text{-}DC}$ | Input common mode range (DC coupled) | | 0.6 | — | $V_{CCA}$ | V |
| $V_{RX\text{-}CM\text{-}AC}$ | Input common mode range (AC coupled)[3] | | 0.1 | — | $V_{CCA}$ +0.2 | V |
| $T_{RX\text{-}RELOCK}$ | SCDR re-lock time[2] | | — | 1000 | — | Bits |
| $Z_{RX\text{-}TERM}$ | Input termination 50/75 Ohm/High Z | | –20% | 50/75/HiZ | +20% | Ohms |
| $RL_{RX\text{-}RL}$ | Return loss (without package) | | 10 | — | — | dB |

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/– 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

## Input Data Jitter Tolerance

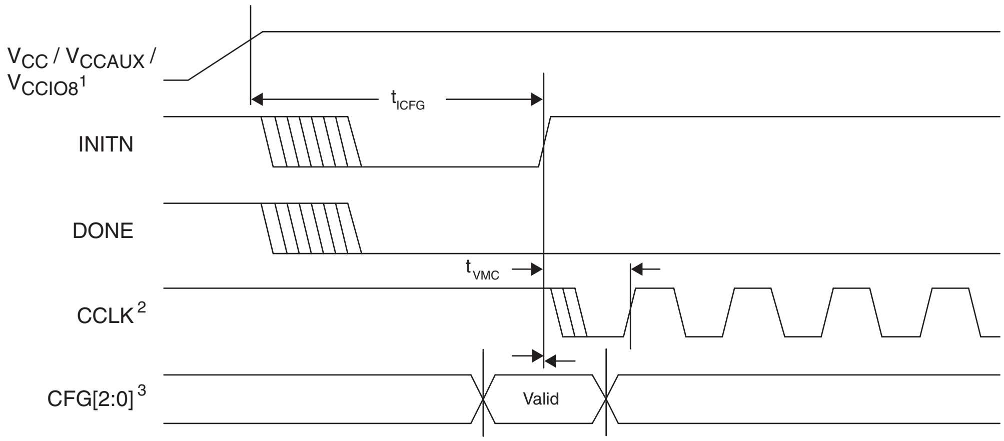
A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

*Table 3-10. Receiver Total Jitter Tolerance Specification*

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 2.5 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 1.25 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 622 Mbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |

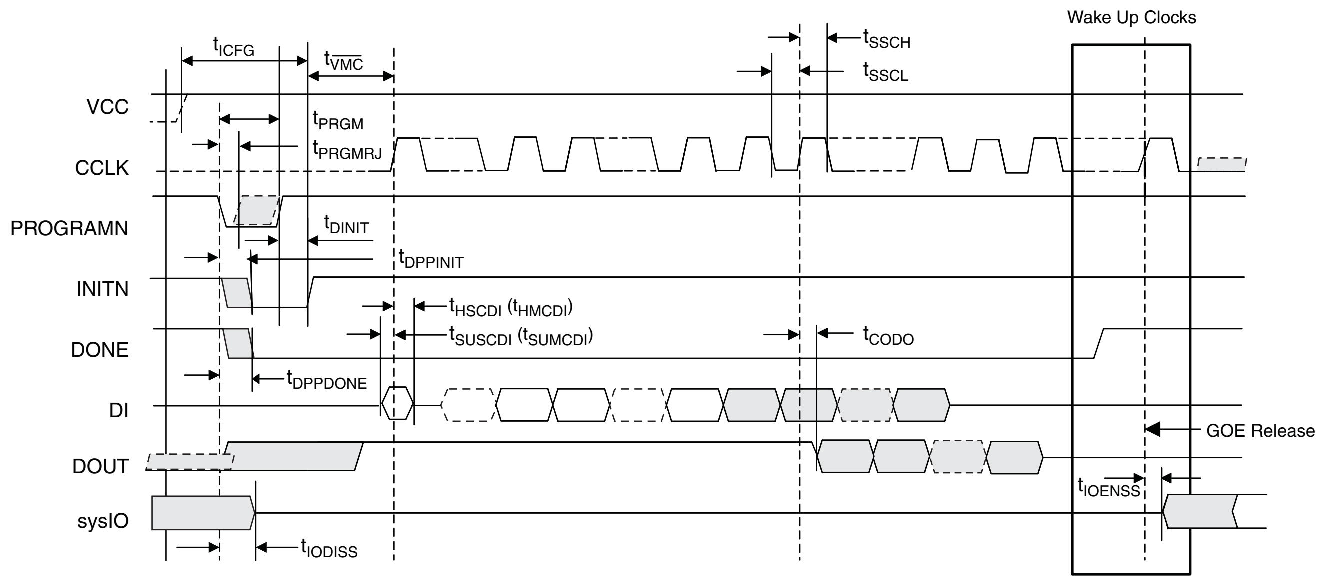
Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

*Figure 3-24. Power-On-Reset (POR) Timing*




1. Time taken from $V_{CC}$, $V_{CCAUX}$ or $V_{CCIO8}$, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

*Figure 3-25. sysCONFIG Port Timing*

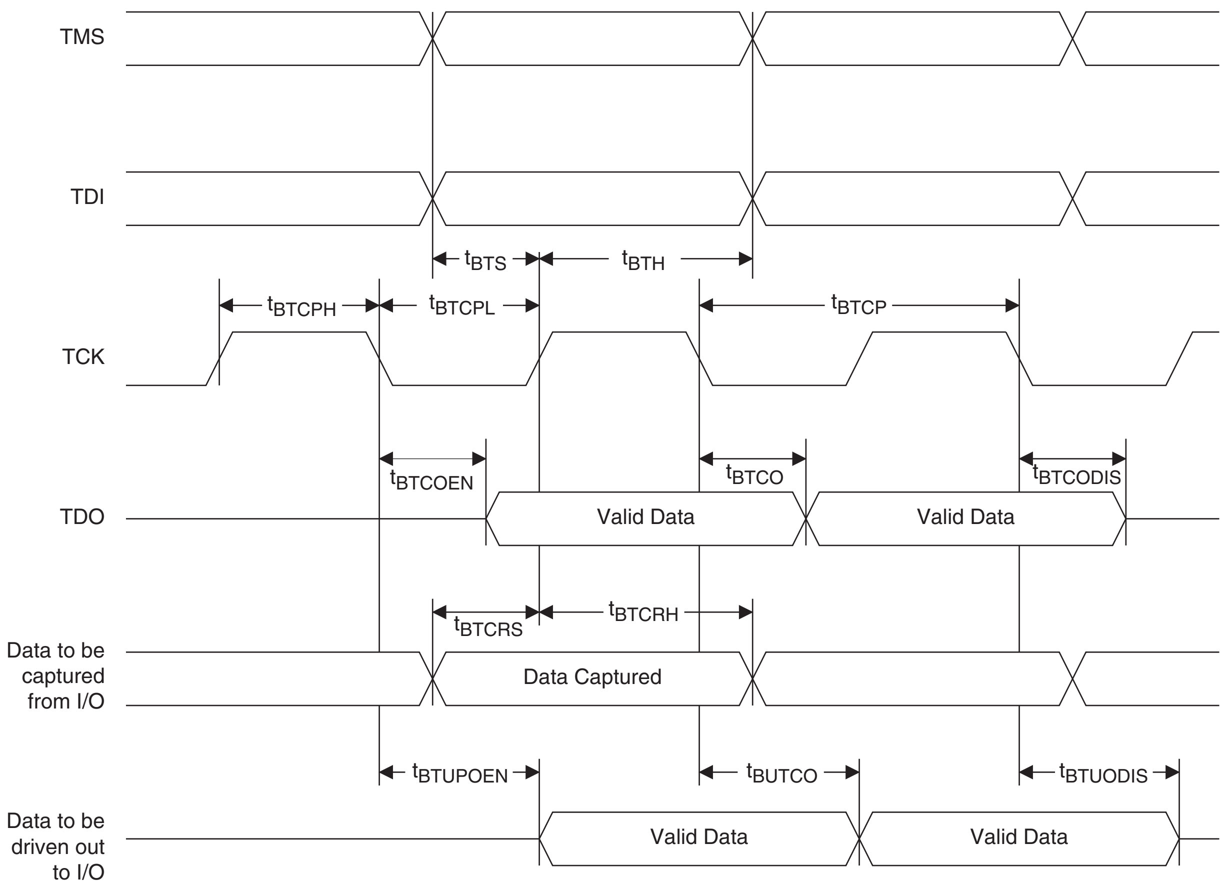


## JTAG Port Timing Specifications

**Over Recommended Operating Conditions**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

***Figure 3-32. JTAG Port Timing Waveforms***



## Point-to-Point LVDS (PPLVDS)

**Over Recommended Operating Conditions**

| Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Output driver supply (+/– 5%) | 3.14 | 3.3 | 3.47 | V |
| | 2.25 | 2.5 | 2.75 | V |
| Input differential voltage | 100 | — | 400 | mV |
| Input common mode voltage | 0.2 | — | 2.3 | V |
| Output differential voltage | 130 | — | 400 | mV |
| Output common mode voltage | 0.5 | 0.8 | 1.4 | V |

## RSDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{OD}$ | Output voltage, differential, $R_T$ = 100 Ohms | 100 | 200 | 600 | mV |
| $V_{OS}$ | Output voltage, common mode | 0.5 | 1.2 | 1.5 | V |
| $I_{RSDS}$ | Differential driver output current | 1 | 2 | 6 | mA |
| $V_{THD}$ | Input voltage differential | 100 | — | — | mV |
| $V_{CM}$ | Input common mode voltage | 0.3 | — | 1.5 | V |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | 500 | — | ps |
| $T_{ODUTY}$ | Output clock duty cycle | 35 | 50 | 65 | % |

Note: Data is for 2 mA drive. Other differential driver current options are available.

## LatticeECP3 Part Number Description

LFE3 – XXX XX – X X XXXXXX X

**Device Family**
ECP3 (LatticeECP3 FPGA + SERDES)

**Logic Capacity**
- 17 = 17K LUTs
- 35 = 33K LUTs
- 70 = 67K LUTs
- 95 = 92K LUTs
- 150 = 149K LUTs

**Supply Voltage**
EA = 1.2 V

**Speed**
- 6 = Slowest
- 7
- 8 = Fastest for LatticeECP3-17EA

**Grade**
- C = Commercial
- I = Industrial

**Package**
- FTN256 = 256-ball Lead-Free ftBGA
- FN484 = 484-ball Lead-Free fpBGA
- FN672 = 672-ball Lead-Free fpBGA
- FN1156 = 1156-ball Lead-Free fpBGA
- MG328 = 328-ball Green csBGA[1]

**Power**
- Blank = Standard Power
- L = Low Power

1. Green = Halogen free and lead free.

## Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:

| Commercial | Industrial |
|---|---|
| LATTICE<br>LFE3-95EA<br>7FN672C<br>Datecode | LATTICE<br>LFE3-95EA<br>7FN672I<br>Datecode |

Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

## LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

**Commercial**

| Part Number | Voltage | Grade | Power | Package[1] | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-17EA-6FTN256C | 1.2 V | –6 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-7FTN256C | 1.2 V | –7 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-8FTN256C | 1.2 V | –8 | STD | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-6LFTN256C | 1.2 V | –6 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-7LFTN256C | 1.2 V | –7 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-8LFTN256C | 1.2 V | –8 | LOW | Lead-Free ftBGA | 256 | COM | 17 |
| LFE3-17EA-6MG328C | 1.2 V | –6 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-7MG328C | 1.2 V | –7 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-8MG328C | 1.2 V | –8 | STD | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-6LMG328C | 1.2 V | –6 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-7LMG328C | 1.2 V | –7 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-8LMG328C | 1.2 V | –8 | LOW | Green csBGA | 328 | COM | 17 |
| LFE3-17EA-6FN484C | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-7FN484C | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-8FN484C | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-6LFN484C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-7LFN484C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | COM | 17 |
| LFE3-17EA-8LFN484C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | COM | 17 |

1. Green = Halogen free and lead free.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-35EA-6FTN256C | 1.2 V | –6 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-7FTN256C | 1.2 V | –7 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-8FTN256C | 1.2 V | –8 | STD | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-6LFTN256C | 1.2 V | –6 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-7LFTN256C | 1.2 V | –7 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-8LFTN256C | 1.2 V | –8 | LOW | Lead-Free ftBGA | 256 | COM | 33 |
| LFE3-35EA-6FN484C | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-7FN484C | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-8FN484C | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-6LFN484C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-7LFN484C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-8LFN484C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | COM | 33 |
| LFE3-35EA-6FN672C | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-7FN672C | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-8FN672C | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-6LFN672C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-7LFN672C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | COM | 33 |
| LFE3-35EA-8LFN672C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | COM | 33 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672C | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672C | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672C | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6LFN672C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7LFN672C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8LFN672C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156C | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156C | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156C | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-6LFN1156C | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7LFN1156C | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8LFN1156C | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | COM | 149 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672CTW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672CTW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672CTW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156CTW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156CTW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156CTW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | COM | 149 |

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250 V.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-70EA-6FN484I | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-7FN484I | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-8FN484I | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-6LFN484I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-7LFN484I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-8LFN484I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-6FN672I | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-7FN672I | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-8FN672I | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-6LFN672I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-7LFN672I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-8LFN672I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-6FN1156I | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-7FN1156I | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-8FN1156I | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-6LFN1156I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-7LFN1156I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-8LFN1156I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-95EA-6FN484I | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-7FN484I | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-8FN484I | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-6LFN484I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-7LFN484I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-8LFN484I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-6FN672I | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-7FN672I | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-8FN672I | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-6LFN672I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-7LFN672I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-8LFN672I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-6FN1156I | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-7FN1156I | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-8FN1156I | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-6LFN1156I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-7LFN1156I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-8LFN1156I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

# LatticeECP3 Family Data Sheet Revision History

**March 2015** **Data Sheet DS1021**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2015 | 2.8EA | Pinout Information<br>All | Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3. |
| | | | Minor style/formatting changes. |
| April 2014 | 02.7EA | DC and Switching Characteristics | Updated LatticeECP3 Supply Current (Standby) table power numbers. |
| | | | Removed speed grade -9 timing numbers in the following sections:<br>— Typical Building Block Function Performance<br>— LatticeECP3 External Switching Characteristics<br>— LatticeECP3 Internal Switching Characteristics<br>— LatticeECP3 Family Timing Adders |
| | | Ordering Information | Removed ordering information for -9 speed grade devices. |
| March 2014 | 02.6EA | DC and Switching Characteristics | Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote. |
| February 2014 | 02.5EA | DC and Switching Characteristics | Updated Hot Socketing Specifications table. Changed $I_{PW}$ to $I_{PD}$ in footnote 3. |
| | | | Updated the following figures:<br>— Figure 3-25, sysCONFIG Port Timing<br>— Figure 3-27, Wake-Up Timing |
| | | Supplemental Information | Added technical note references. |
| September 2013 | 02.4EA | DC and Switching Characteristics | Updated the Wake-Up Timing Diagram |
| | | | Added the following figures:<br>— Master SPI POR Waveforms<br>— SPI Configuration Waveforms<br>— Slave SPI HOLDN Waveforms |
| | | | Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table. |
| June 2013 | 02.3EA | Architecture | sysI/O Buffer Banks text section – Updated description of "Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)" for hot socketing information. |
| | | | sysI/O Buffer Banks text section – Updated description of "Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)" for PCI clamp information. |
| | | | On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%). |
| | | | Architecture Overview section – Added information on the state of the register on power up and after configuration. |
| | | DC and Switching Characteristics | sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard. |
| | | | sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1. |
| | | | Added Oscillator Output Frequency table. |
| | | | LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for $t_{CODO}$ parameter. |
| | | | LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| | | | Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram. |
| | | | Updated Device Configuration text section. |
| | | | Corrected software default value of MCCLK to be 2.5 MHz. |
| | | DC and Switching Characteristics | Updated VCCOB Min/Max data in Recommended Operating Conditions table. |
| | | | Corrected footnote 2 in sysIO Recommended Operating Conditions table. |
| | | | Added added footnote 7 for $t_{SKEW\_PRIB}$ to External Switching Characteristics table. |
| | | | Added 2-to-1 Gearing text section and table. |
| | | | Updated External Reference Clock Specification (refclkp/refclkn) table. |
| | | | LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{DINIT}$ information. |
| | | | Added sysCONFIG Port Timing waveform. |
| | | | Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$. |
| | | | Added footnote 4 to sysCLOCK PLL Timing table for $t_{PFD}$. |
| | | | Added SERDES/PCS Block Latency Breakdown table. |
| | | | External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF. |
| | | | Added SERDES External Reference Clock Waveforms. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Pin-to-pin performance table, changed "typically 3% slower" to "typically slower". |
| | | | Updated timing information |
| | | | Updated SERDES minimum frequency. |
| | | | Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements. |
| | | | Updated Serial Input Data Specifications table. |
| | | | Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section. |
| | | Pinout Information | Updated Signal Description tables. |
| | | | Updated Pin Information Summary tables and added footnote 1. |
| February 2009 | 01.0 | — | Initial release. |