E. Lattice Semiconductor Corporation - LFE3-70EA-6FN1156I Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-6fn1156i

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Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36





Spine Repeaters



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.





Notes:

1. Clock inputs can be configured in differential or single ended mode.

2. The two DLLs can also drive the two top edge clocks.

3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- 1. **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- 3. **Read-Before-Write (EA devices only)** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP[™] Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element



To FPGA Core



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB





ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850



2. Left and Right (Banks 2, 3, 6 and 7) sysl/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysl/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysl/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysl/O Standards

The LatticeECP3 sysl/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysl/O buffer to support a variety of standards please see TN1177, LatticeECP3 syslO Usage Guide.



Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.



LatticeECP3 Supply Current (Standby)^{1, 2, 3, 4, 5, 6}

			Тур	ical	
Symbol	Parameter	Device	-6L, -7L, -8L	-6, -7, -8	Units
		ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
I _{CC}	Core Power Supply Current	ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
		ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
I _{CCAUX}	Auxiliary Power Supply Current	ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
		ECP-17EA	0.0	0.0	mA
	PLL Power Supply Current (Per PLL)	ECP3-35EA	0.1	0.1	mA
I _{CCPLL}	PLL Power Supply Current (Per PLL)	ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
		ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I _{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
		ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
I _{CCA}	Iransmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{\mbox{CCIO}}$ or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 85$ °C, power supplies at nominal voltage.

6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.



RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

Table 3-4. RSDS25E DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/–1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.35	V
V _{OL}	Output Low Voltage	1.15	V
V _{OD}	Output Differential Voltage	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-8 -7		_	-6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.7	_	0.8	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.6	—	1.8	_	2.0	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-35EA	_	3.2	—	3.4	—	3.6	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.6	_	0.7	—	0.8	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-35EA	0.3	—	0.3	—	0.4	-	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.6	_	1.7	_	1.8	_	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	_	0.0	_	0.0	_	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-17EA	_	3.0	—	3.3	—	3.5	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.6	_	0.7	_	0.8	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-17EA	0.3	_	0.3	_	0.4	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.6	—	1.7	—	1.8	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	_	0.0	_	0.0	—	ns
Generic DDR ¹²									
Generic DDRX1 In Input	puts with Clock and Data (>10 Bits	Wide) Centered at Pi	n (GDDF	RX1_RX.S	SCLK.Ce	ntered) L	Ising PC	LK Pin fo	or Clock
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	480	—	480	_	480		ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	480	—	480	—	480		ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.SC	CLK.PLL	Aligned)	Using P	LLCLKIN	Pin for
Data Left, Right, a	nd Top Sides and Clock Left and F	Right Sides							
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	_	0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	_	UI
f _{MAX GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.S0	CLK.Alig	ned) Usiı	ng DLL -	CLKIN P	in for
Data Left, Right ar	d Top Sides and Clock Left and R	ight Sides							
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	_	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775		UI
f _{MAX GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	—	250	MHz
Generic DDRX1 In Input	puts with Clock and Data (<10 Bits	Wide) Centered at Pi	n (GDDF	X1_RX.	DQS.Cen	tered) U	sing DQ	S Pin for	Clock
t _{SUGDDB}	Data Setup After CLK	All ECP3EA Devices	535	_	535		535		ps
tHOGDDR	Data Hold After CLK	All ECP3EA Devices	535	—	535		535	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In	puts with Clock and Data (<10bits	wide) Aligned at Pin (GDDRX	1_RX.DQ	S.Aligne	d) Using	DQS Pin	for Cloc	k Input
Data and Clock Le	ft and Right Sides	`			-				-
t _{DVACI KGDDB}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	_	0.225		0.225	UI
STROLIGED									

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial	Operating Conditions
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			-	-8	-7		-6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 Ou	tput with Clock and Data (>10 Bits	Wide) Centered at Pir	n Using I	PLL (GDI	DRX2_TX	.PLL.Cer	ntered) ¹⁰		
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	_	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	_	432	_	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin	Parameters (Input Data are Strobe	Edge Aligned, Output	ut Strobe	e Edge is	Data Ce	ntered)4			
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL f	or SCLK) I/O Pin Parameters	•							
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	_	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	_	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing	9								
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	-90	90	-90	90	-90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jit- ter During DLL Locking Period	All ECP3 Devices	_	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.

3. Generic DDR timing numbers based on LVDS I/O.

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.

5. DDR3 timing numbers based on SSTL15.

6. Uses LVDS I/O standard.

7. The current version of software does not support per bank skew numbers; this will be supported in a future release.

8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

9. Using settings generated by IPexpress.

10. These numbers are generated using best case PLL located in the center of the device.

11. Uses SSTL25 Class II Differential I/O Standard.

12. All numbers are generated with ispLEVER 8.1 software.

13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



Timing Diagrams





Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers





Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF} ¹	Differential rise/fall time	20%-80%	—	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{3, 4, 5}	Output data deterministic jitter			_	0.17	UI
J _{TX_TJ} ^{2, 3, 4, 5}	Total output data jitter			_	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	_	_	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{2, 3, 4, 5}	Deterministic jitter tolerance (peak-to-peak)		_	—	0.37	UI
J _{RX_RJ} ^{2, 3, 4, 5}	Random jitter tolerance (peak-to-peak)		_	_	0.18	UI
J _{RX_SJ} ^{2, 3, 4, 5}	Sinusoidal jitter tolerance (peak-to-peak)		_	_	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4, 5}	Total jitter tolerance (peak-to-peak)		_	_	0.65	UI
T _{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.



Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals ³		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	0	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	0	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm		Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm		Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins							
For Left and Right Edges of the Device									
D[Edgo] [n 2]	А	DQ							
	В	DQ							
P[Edge] [n-2]	А	DQ							
	В	DQ							
D[Edgo] [n 1]	A	DQ							
	В	DQ							
P[Edge] [n]	А	[Edge]DQSn							
	В	DQ							
P[Edge] [n 1]	А	DQ							
	В	DQ							
D[Edgo] [n 2]	A	DQ							
r[Euge][II+2]	В	DQ							
For Top Edge of the Devi	ce								
P[Edge] [n-3]	А	DQ							
	В	DQ							
P[Edge] [n-2]	А	DQ							
	В	DQ							
P[Edge] [n-1]	А	DQ							
	В	DQ							
P[Edge] [n]	А	[Edge]DQSn							
r [⊏uge] [n]	В	DQ							
P[Edge] [n+1]	А	DQ							
i [Euge] [iit i]	В	DQ							
P[Edge] [n 2]	А	DQ							
י נבטשכן נוידבן	В	DQ							

Note: "n" is a row PIC number.



LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.



Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t _{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t _{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t _{PFD} .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Out- put Jitter, Typical Building Block Function Performance, Register-to- Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	_	Initial release.