E. Lattice Semiconductor Corporation - LFE3-70EA-7FN1156C Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7fn1156c

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Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.





Notes:

1. Clock inputs can be configured in differential or single ended mode.

2. The two DLLs can also drive the two top edge clocks.

3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sys-DSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA ¹ , OPOSB, ONEGB ¹	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR ¹	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL ¹	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT ¹	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 ¹ , DQCLK1 ¹	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW ²	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID ¹	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.



Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysl/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.



2. Left and Right (Banks 2, 3, 6 and 7) sysl/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysl/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysl/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysl/O Standards

The LatticeECP3 sysl/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysl/O buffer to support a variety of standards please see TN1177, LatticeECP3 syslO Usage Guide.



Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.



sysl/O Recommended Operating Conditions

		V _{CCIO}		V _{REF} (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS33 ²	3.135	3.3	3.465	—	—	—
LVCMOS33D	3.135	3.3	3.465	—	—	—
LVCMOS25 ²	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12 ²	1.14	1.2	1.26	—	—	—
LVTTL33 ²	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15 ³	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ²	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ²	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_l ²	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II ²	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 ²	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 2}	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25 ^{1, 2}	2.375	2.5	2.625		—	—
RSDS ²	2.375	2.5	2.625	—	—	—
RSDSE ^{1, 2}	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D ³	1.43	1.5	1.57		—	—
SSTL18D_I ^{2, 3} , II ^{2, 3}	1.71	1.8	1.89		—	—
SSTL25D_ I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_ I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_ I ²	1.425	1.5	1.575	_	—	—
HSTL18D_ I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. For input voltage compatibility, see TN1177, LatticeECP3 sysIO Usage Guide.

3. VREF is required when using Differential SSTL to interface to DDR memory.



MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.





Table 3-5. MLVDS25 DC Conditions¹

		Typical		
Parameter	Description	Ζο=50 Ω	Ζο=70 Ω	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R _{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R _{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V _{OH}	Output High Voltage	1.52	1.60	V
V _{OL}	Output Low Voltage	0.98	0.90	V
V _{OD}	Output Differential Voltage	0.54	0.70	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.



DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Тур.	Max.	Units
f _{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{CLKOP} ¹	Output clock frequency, CLKOP		133	—	500	MHz
f _{CLKOS} ²	Output clock frequency, CLKOS		33.3	—	500	MHz
t _{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
	Output clock duty cycle (at 50% levels, 50% duty	Edge Clock	40		60	%
t _{DUTY}	off, time reference delay mode)	Primary Clock	30		70	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	45		55	%
t _{DUTYTRD}	DUTYTRD duty cycle input clock, 50% duty cycle circuit	Primary Clock ≥ 250 MHz	30		70	%
	enabled, time reference delay mode)	Edge Clock	45		55	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	40		60	%
t _{DUTYCIB} du	duty cycle input clock, 50% duty cycle circuit	Primary Clock ≥ 250 MHz	30		70	%
	cascading	Edge Clock	45		55	%
t _{SKEW} ³	Output clock to clock skew between two outputs with the same phase setting		_	—	100	ps
t _{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		_	—	+/-400	ps
t _{PWH}	Input clock minimum pulse width high (at 80% level)		550	_	_	ps
t _{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	_	ps
t _{INSTB}	Input clock period jitter			—	500	ps
t _{LOCK}	DLL lock time		8	—	8200	cycles
t _{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t _{DEL}	Delay step size		27	45	70	ps
t _{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t _{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a "path-matching" design guideline and is not a measurable specification.



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F _{REF}	Frequency range	15	_	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	_	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ²	200	_	V _{CCA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	_	2*V _{CCA}	mV, p-p differential
V _{REF-IN}	Input levels	0	_	V _{CCA} + 0.3	V
D _{REF}	Duty cycle ³	40	_	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-20%	100/2K	+20%	Ohms
C _{REF-IN-CAP}	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms





Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).



LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t _{SSCL}	CCLK Minimum Low Pulse	5		ns
t _{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	_	ns
t _{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	_	ns
Master and	Slave SPI (Continued)			
t _{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	_	ns
t _{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	_	ns
t _{HLQZ}	HOLDN to Output High-Z	_	9	ns
t _{HHQX}	HOLDN to Output Low-Z	_	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle





Figure 3-24. Power-On-Reset (POR) Timing



Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
Device is in a Master Mode (SPI, SPIm).
The CFG pins are normally static (hard wired).



Figure 3-25. sysCONFIG Port Timing



Signal Descriptions (Cont.)

Signal Name	I/O	Description			
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.			
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.			
Dedicated SERDES Signals ³					
PCS[Index]_HDINNm	I	High-speed input, negative channel m			
PCS[Index]_HDOUTNm	0	High-speed output, negative channel m			
PCS[Index]_REFCLKN	I	Negative Reference Clock Input			
PCS[Index]_HDINPm	I	High-speed input, positive channel m			
PCS[Index]_HDOUTPm	0	High-speed output, positive channel m			
PCS[Index]_REFCLKP	I	Positive Reference Clock Input			
PCS[Index]_VCCOBm		Output buffer power supply, channel m (1.2V/1.5)			
PCS[Index]_VCCIBm		Input buffer power supply, channel m (1.2V/1.5V)			

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.



Package Pinout Information

Package pinout information can be found under "Data Sheets" on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software



LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.