E. Lattice Semiconductor Corporation - <u>LFE3-70EA-7FN1156I Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7fn1156i

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ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.



Figure 2-10. Primary Clock Sources for LatticeECP3-35



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150



Note: Clock inputs can be configured in differential or single-ended mode.



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.





Notes:

1. Clock inputs can be configured in differential or single ended mode.

2. The two DLLs can also drive the two top edge clocks.

3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- 1. **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- 3. **Read-Before-Write (EA devices only)** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP[™] Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB





MCCLK (MHz)	MCCLK (MHz)
	10
2.5 ¹	13
4.3	15 ²
5.4	20
6.9	26
8.1	33 ³
9.2	

 Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the LatticeECP3 Pin Migration Tables and Diamond software for specific restrictions and limitations.



LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.





Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5 V	-0.07	-0.04	-0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	-0.22	-0.19	-0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.3V	-0.06	-0.06	-0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.3V	-0.01	-0.02	-0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.3V	-0.07	-0.07	-0.08	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.3V	-0.12	-0.13	-0.14	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	-0.06	-0.06	-0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	-0.01	-0.02	-0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	-0.07	-0.07	-0.08	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	-0.05	-0.06	-0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns

Over Recommended Commercial Operating Conditions



LatticeECP3 Maximum I/O Buffer Speed ^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Buffer	Description	Max.	Units		
Maximum Input Frequency					
LVDS25	LVDS, $V_{CCIO} = 2.5 V$	400	MHz		
MLVDS25	MLVDS, Emulated, V _{CCIO} = 2.5 V	400	MHz		
BLVDS25	BLVDS, Emulated, V _{CCIO} = 2.5 V	400	MHz		
PPLVDS	Point-to-Point LVDS	400	MHz		
TRLVDS	Transition-Reduced LVDS	612	MHz		
Mini LVDS	Mini LVDS	400	MHz		
LVPECL33	LVPECL, Emulated, V _{CCIO} = 3.3 V	400	MHz		
HSTL18 (all supported classes)	HSTL_18 class I, II, V _{CCIO} = 1.8 V	400	MHz		
HSTL15	HSTL_15 class I, V _{CCIO} = 1.5 V	400	MHz		
SSTL33 (all supported classes)	SSTL_3 class I, II, V _{CCIO} = 3.3 V	400	MHz		
SSTL25 (all supported classes)	SSTL_2 class I, II, V _{CCIO} = 2.5 V	400	MHz		
SSTL18 (all supported classes)	SSTL_18 class I, II, V _{CCIO} = 1.8 V	400	MHz		
LVTTL33	LVTTL, V _{CCIO} = 3.3 V	166	MHz		
LVCMOS33	LVCMOS, V _{CCIO} = 3.3 V	166	MHz		
LVCMOS25	LVCMOS, V _{CCIO} = 2.5 V	166	MHz		
LVCMOS18	LVCMOS, V _{CCIO} = 1.8 V	166	MHz		
LVCMOS15	LVCMOS 1.5, V _{CCIO} = 1.5 V	166	MHz		
LVCMOS12	LVCMOS 1.2, V _{CCIO} = 1.2 V	166	MHz		
PCI33	PCI, V _{CCIO} = 3.3 V	66	MHz		
Maximum Output Frequency					
LVDS25E	LVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz		
LVDS25	LVDS, $V_{CCIO} = 2.5 V$	612	MHz		
MLVDS25	MLVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz		
RSDS25	RSDS, Emulated, V _{CCIO} = 2.5 V	612	MHz		
BLVDS25	BLVDS, Emulated, V _{CCIO} = 2.5 V	300	MHz		
PPLVDS	Point-to-point LVDS	612	MHz		
LVPECL33	LVPECL, Emulated, V _{CCIO} = 3.3 V	612	MHz		
Mini-LVDS	Mini LVDS	612	MHz		
HSTL18 (all supported classes)	HSTL_18 class I, II, V _{CCIO} = 1.8 V	200	MHz		
HSTL15 (all supported classes)	HSTL_15 class I, V _{CCIO} = 1.5 V	200	MHz		
SSTL33 (all supported classes)	SSTL_3 class I, II, V _{CCIO} = 3.3 V	233	MHz		
SSTL25 (all supported classes)	SSTL_2 class I, II, V _{CCIO} = 2.5 V	233	MHz		
SSTL18 (all supported classes)	SSTL_18 class I, II, V _{CCIO} = 1.8 V	266	MHz		
LVTTL33	LVTTL, V _{CCIO} = 3.3 V	166	MHz		
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	166	MHz		
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	166	MHz		
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	166	MHz		
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	166	MHz		
LVCMOS12 (For all drives except 2 mA)	LVCMOS, V _{CCIO} = 1.2 V	166	MHz		
LVCMOS12 (2 mA drive)	LVCMOS, V _{CCIO} = 1.2 V	100	MHz		



Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Symbol	Description	Test Conditions	Min	Тур	Max	Units	
Transmit ¹							
UI	Unit interval		399.88	400	400.12	ps	
V _{TX-DIFF_P-P}	Differential peak-to-peak output voltage		0.8	1.0	1.2	V	
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio		-3	-3.5	-4	dB	
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage		—	_	20	mV	
V _{TX-RCV-DETECT}	Amount of voltage change allowed dur- ing receiver detection		—	_	600	mV	
V _{TX-DC-CM}	Tx DC common mode voltage		0		V _{CCOB} + 5%	V	
ITX-SHORT	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	—	_	90	mA	
Z _{TX-DIFF-DC}	Differential output impedance		80	100	120	Ohms	
RL _{TX-DIFF}	Differential return loss		10	_	—	dB	
RL _{TX-CM}	Common mode return loss		6.0	—	—	dB	
T _{TX-RISE}	Tx output rise time	20 to 80%	0.125	—	—	UI	
T _{TX-FALL}	Tx output fall time	20 to 80%	0.125		—	UI	
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link		—	_	1.3	ns	
T _{TX-EYE}	Transmitter eye width		0.75	—	—	UI	
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median		_	—	0.125	UI	
Receive ^{1, 2}		•			•		
UI	Unit Interval		399.88	400	400.12	ps	
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage		0.34 ³	_	1.2	V	
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage		65		340 ³	mV	
V _{RX-CM-AC_P}	Receiver common mode voltage for AC coupling		—	_	150	mV	
Z _{RX-DIFF-DC}	DC differential input impedance		80	100	120	Ohms	
Z _{RX-DC}	DC input impedance		40	50	60	Ohms	
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance		200K		—	Ohms	
RL _{RX-DIFF}	Differential return loss		10	_	—	dB	
RL _{RX-CM}	Common mode return loss		6.0	—	—	dB	
T _{RX-IDLE-DET-DIFF-ENTERTIME}	Maximum time required for receiver to recognize and signal an unexpected idle on link		_	_	_	ms	

1. Values are measured at 2.5 Gbps.

2. Measured with external AC-coupling on the receiver.

3.Not in compliance with PCI Express 1.1 standard.



HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-22. Transmit and Receive^{1, 2}

		Spec. Compliance		
Symbol	Description	Min. Spec.	Max. Spec.	Units
Transmit		•		
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive		•		
R _T	Termination Resistance	40	60	Ohms
V _{ICM}	Input AC Common Mode Voltage (50-Ohm Set- ting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.

2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.



Figure 3-19. Test Loads

Test Loads









LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t _{SSCL}	CCLK Minimum Low Pulse	5		ns
t _{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	_	ns
t _{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	_	ns
Master and	Slave SPI (Continued)			
t _{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	_	ns
t _{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	_	ns
t _{HLQZ}	HOLDN to Output High-Z	_	9	ns
t _{HHQX}	HOLDN to Output Low-Z	_	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle















Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Тур.	Max.	Units
Output driver supply $(1/-5\%)$	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
V _{OD}	Output voltage, differential, R _T = 100 Ohms	100	200	600	mV
V _{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I _{RSDS}	Differential driver output current	1	2	6	mA
V _{THD}	Input voltage differential	100	—	-	mV
V _{CM}	Input common mode voltage	0.3	—	1.5	V
T _R , T _F	Output rise and fall times, 20% to 80%	—	500		ps
T _{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.



Pin Information Summary (Cont.)

Pin Information Summary Pin Type			ECP3-95EA		ECP3-	150EA	
		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA	
	Bank 0	21	30	43	30	47	
	Bank 1	18	24	39	24	43	
Emulated	Bank 2	8	12	13	12	18	
Differential I/O	Bank 3	20	23	33	23	37	
per Bank	Bank 6	22	25	33	25	37	
	Bank 7	11	16	18	16	24	
	Bank 8	12	12	12	12	12	
	Bank 0	0	0	0	0	0	
	Bank 1	0	0	0	0	0	
Highspeed	Bank 2	6	9	9	9	15	
Differential I/O	Bank 3	9	12	16	12	21	
per Bank	Bank 6	11	14	16	14	21	
	Bank 7	9	12	13	12	18	
	Bank 8	0	0	0	0	0	
	Bank 0	42/21	60/30	86/43	60/30	94/47	
	Bank 1	36/18	48/24	78/39	48/24	86/43	
Total Single Ended/	Bank 2	28/14	42/21	44/22	42/21	66/33	
Total Differential	Bank 3	58/29	71/35	98/49	71/35	116/58	
I/O per Bank	Bank 6	67/33	78/39	98/49	78/39	116/58	
	Bank 7	40/20	56/28	62/31	56/28	84/42	
	Bank 8	24/12	24/12	24/12	24/12	24/12	
	Bank 0	3	5	7	5	7	
	Bank 1	3	4	7	4	7	
	Bank 2	2	3	3	3	4	
DDR Groups Bonded	Bank 3	3	4	5	4	7	
per Bank	Bank 6	4	4	5	4	7	
	Bank 7	3	4	4	4	6	
	Configuration Bank8	0	0	0	0	0	
SERDES Quads	1	1	2	3	2	4	

1. These pins must remain floating on the board.



Package Pinout Information

Package pinout information can be found under "Data Sheets" on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software



LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.