E. Lattice Semiconductor Corporation - <u>LFE3-70EA-7FN484I Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7fn484i

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LatticeECP3 Family Data Sheet Introduction

February 2012

Features

- Higher Logic Density for Increased System Integration
 - 17K to 149K LUTs
 - 116 to 586 I/Os
- Embedded SERDES
 - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
 - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
 - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

■ sysDSP[™]

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
 - -Half 36x36, two 18x18 or four 9x9 multipliers
 - Advanced 18x36 MAC and 18x18 Multiply-
 - Multiply-Accumulate (MMAC) operations

■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM[™] Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
 Two DLLs and up to ten PLLs per device
- Pre-Engineered Source Synchronous I/O
 - DDR registers in I/O cells

Table 1-1. LatticeECP3™ Family Selection Guide

• Dedicated read/write levelling functionality

Data Sheet DS1021

- Dedicated gearing logic
- Source synchronous standards support
 ADC/DAC, 7:1 LVDS, XGMII
 Link Speed ADC/DAC devices
 - -High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- Programmable sysl/O[™] Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - Optional equalization filter on inputs
 - LVTTL and LVCMOS 33/25/18/15/12
 - SSTL 33/25/18/15 I, II
 - HSTL15 I and HSTL18 I, II
 - PCI and Differential HSTL, SSTL
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- · On-chip oscillator for initialization & general use
- 1.2 V core power supply

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2/2	4/2	10/2	10 / 2	10/2
Packages and SERDES Channels	/ I/O Combinatio	ns		•	
328 csBGA (10 x 10 mm)	2/116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

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LatticeECP3 Family Data Sheet Architecture

June 2013

Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sys-DSP[™] Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG[™] port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.





Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element



To FPGA Core



Figure 2-34. Output and Tristate Block for Left and Right Edges



Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysl/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.



Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dualboot image support.

1. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. Dual-Boot Image Support

Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10 kOhm \pm 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/- 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.



sysl/O Single-Ended DC Electrical Characteristics

Input/Output		V _{IL}	V _{II}	4	Voi	Vou		
Standard	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	l _{OL} ¹ (mA)	I _{OH} ¹ (mA)
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2 V _{CCIO} - 0.2		0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2 V _{CCIO} - 0.2		0.1	-0.1
LVCMOS18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
	-03	0.35 Vacua	0.65 Vacia	36	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
	-0.5	0.33 VCCIO	0.03 VCCIO	5.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
	-0.3	0.35 Vaa	0.65 Vaa	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2
LVONICOTZ	-0.0	0.00 VCC	0.03 VCC	0.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V _{CCIO}	0.5 V _{CCIO}	3.6	0.1 V _{CCIO}	0.9 V _{CCIO}	1.5	-0.5
SSTL18_I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.6	0.4	V _{CCIO} - 0.4	6.7	-6.7
SSTL18_II	_0.3	V0 125	V + 0.125	3.6	0.28	V 0 28	8	-8
(DDR2 Memory)	-0.5	V _{REF} - 0.123	V _{REF} + 0.125	5.0	0.20	V CCIO - 0.20	11	-11
SSTI 2 1	_0.3	V0 18	V \ 0.18	3.6	0.54	V	7.6	-7.6
551L2_1	-0.5	V _{REF} - 0.10	V _{REF} + 0.10	5.0	0.54	V CCIO - 0.02	12	-12
SSTL2_II	_0.3	V0.18	V \ 0.18	3.6	0.35	V	15.2	-15.2
(DDR Memory)	-0.5	V _{REF} - 0.10	V _{REF} + 0.10	5.0	0.00	V CCIO - 0.43	20	-20
SSTL3_I	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.7	V _{CCIO} - 1.1	8	-8
SSTL3_II	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.5	V _{CCIO} - 0.9	16	-16
SSTL15	0.2	V 01	V + 0.1	2.6	0.2	V _{CCIO} - 0.3	7.5	-7.5
(DDR3 Memory)	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.0	0.5	V _{CCIO} * 0.8	9	-9
	_0.3	V01	V 101	3.6	0.4	V 0 4	4	-4
	-0.5	V _{REF} - 0.1	VREF + 0.1	5.0	0.4	V CCIO - 0.4	8	-8
	_0.3	V01	V 1 0 1	3.6	0.4	V04	8	-8
	-0.3	VREF - 0.1	VREF + 0.1	3.0	0.4	VCCIO - 0.4	12	-12
HSTL18_II	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	16	-16

1. For electromigration, the average DC current drawn by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed n * 8 mA, where n is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.



sysI/O Differential Electrical Characteristics LVDS25

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} ¹ , V _{INM} ¹	Input Voltage		0	_	2.4	V
V _{CM} ¹	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	_	mV
I _{IN}	Input Current	Power On or Power Off		_	+/-10	μΑ
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm		1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9 V	1.03	_	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L		_	_	50	mV
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

1, On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.



Units V

Ω

Ω

Ω

Ω

٧

٧

V

V

mΑ

BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS25 DC Conditions¹

V_{CCIO}

ZOUT

R_S

R_{TL}

 R_{TR} V_{OH}

VOL

VOD

V_{CM}

	-	-		
		Typical		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	
CCIO	Output Driver Supply (+/– 5%)	2.50	2.50	

10.00

90.00

45.00

45.00

1.38

1.12

0.25

1.25

11.24

10.00

90.00

90.00

90.00

1.48

1.02

0.46

1.25

10.20

Over Recommended Operating Conditions

 I_{DC} 1. For input buffer, see LVDS table.

Driver Impedance

Output High Voltage

Output Low Voltage

DC Output Current

Output Differential Voltage

Output Common Mode Voltage

Driver Series Resistor (+/- 1%)

Driver Parallel Resistor (+/- 1%)

Receiver Termination (+/- 1%)



LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL33



Table 3-3. LVPECL33 DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z _{OUT}	Driver Impedance	10	Ω
R _S	Driver Series Resistor (+/-1%)	93	Ω
R _P	Driver Parallel Resistor (+/-1%)	196	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	2.05	V
V _{OL}	Output Low Voltage	1.25	V
V _{OD}	Output Differential Voltage	0.80	V
V _{CM}	Output Common Mode Voltage	1.65	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

Register-to-Register Performance^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	500	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	400	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	260	MHz







Figure 3-7. DDR/DDR2/DDR3 Parameters





PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Symbol	Description	Test Conditions	Min	Тур	Max	Units
Transmit ¹						
UI	Unit interval		399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output voltage		0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio		-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage		—	_	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed dur- ing receiver detection		—	_	600	mV
V _{TX-DC-CM}	Tx DC common mode voltage		0		$V_{CCOB} + 5\%$	V
ITX-SHORT	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	—	_	90	mA
Z _{TX-DIFF-DC}	Differential output impedance		80	100	120	Ohms
RL _{TX-DIFF}	Differential return loss		10		—	dB
RL _{TX-CM}	Common mode return loss		6.0		—	dB
T _{TX-RISE}	Tx output rise time	20 to 80%	0.125		—	UI
T _{TX-FALL}	Tx output fall time	20 to 80%	0.125		—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link		—	_	1.3	ns
T _{TX-EYE}	Transmitter eye width		0.75		—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median		—	_	0.125	UI
Receive ^{1, 2}						
UI	Unit Interval		399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage		0.34 ³	_	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage		65	_	340 ³	mV
V _{RX-CM-AC_P}	Receiver common mode voltage for AC coupling		—	_	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance		80	100	120	Ohms
Z _{RX-DC}	DC input impedance		40	50	60	Ohms
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance		200K	_	—	Ohms
RL _{RX-DIFF}	Differential return loss		10		_	dB
RL _{RX-CM}	Common mode return loss		6.0	_	—	dB
T _{RX-IDLE-DET-DIFF-ENTERTIME}	Maximum time required for receiver to recognize and signal an unexpected idle on link		—		_	ms

1. Values are measured at 2.5 Gbps.

2. Measured with external AC-coupling on the receiver.

3.Not in compliance with PCI Express 1.1 standard.



XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF}	Differential rise/fall time	20%-80%	_	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{2, 3, 4}	Output data deterministic jitter		_	—	0.17	UI
J _{TX_TJ} ^{1, 2, 3, 4}	Total output data jitter		_	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.

2. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	_	_	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	_	_	dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{1, 2, 3}	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J _{RX_RJ} ^{1, 2, 3}	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J _{RX_SJ} ^{1, 2, 3}	Sinusoidal jitter tolerance (peak-to-peak)		—	_	0.10	UI
J _{RX_TJ} ^{1, 2, 3}	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T _{RX_EYE}	Receiver eye opening		0.35		_	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.



SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps		—	0.20	UI
T _{JALIGNMENT} ^{1, 2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	_	2.0	UI

Notes:

 Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.

2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.

3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.

4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDI}	Serial input data rate		270	_	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	_	_	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
F _{VCLK}	Video output clock frequency		27	-	74.25	MHz
DCV	Duty cycle, video clock		45	50	55	%



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins						
For Left and Right Edges of the Device								
D[Edgo] [n 2]	А	DQ						
	В	DQ						
P[Edge] [n-2]	А	DQ						
	В	DQ						
D[Edgo] [n 1]	A	DQ						
	В	DQ						
P[Edge] [n]	А	[Edge]DQSn						
	В	DQ						
P[Edge] [n 1]	А	DQ						
	В	DQ						
D[Edgo] [n 2]	A	DQ						
r[Euge][II+2]	В	DQ						
For Top Edge of the Devi	ce							
P[Edge] [n-3]	А	DQ						
	В	DQ						
P[Edge] [n-2]	А	DQ						
	В	DQ						
P[Edge] [n-1]	А	DQ						
	В	DQ						
P[Edge] [n]	А	[Edge]DQSn						
r [⊏uge] [n]	В	DQ						
P[Edge] [n+1]	А	DQ						
i [Euge] [iit i]	В	DQ						
P[Edge] [n 2]	А	DQ						
י נבטשכן נוידבן	В	DQ						

Note: "n" is a row PIC number.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break- down table.
		Pinout Information	"Logic Signal Connections" section heading renamed "Package Pinout Information". Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V _{CCA} signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for $\ensuremath{t_{RST}}$
		Ordering Information	Updated topside marks with new logos in the Ordering Information sec- tion.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 Exter- nal Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL TIming table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, $t_{J T}\!.$
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t _{SUWBEN EBB} and t _{HWBEN EBB} .
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications



Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t _{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t _{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t _{PFD} .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Out- put Jitter, Typical Building Block Function Performance, Register-to- Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	_	Initial release.