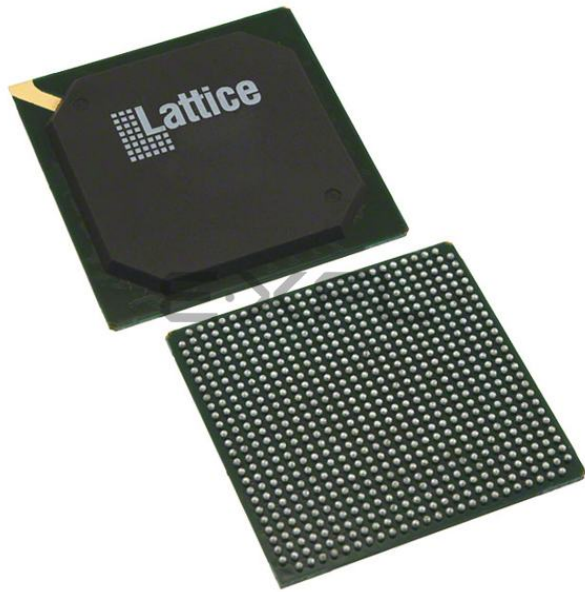




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7fn672i

Features

■ Higher Logic Density for Increased System Integration

- 17K to 149K LUTs
- 116 to 586 I/Os

■ Embedded SERDES

- 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
- Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
- Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

■ sysDSP™

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
 - Half 36x36, two 18x18 or four 9x9 multipliers
 - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations

■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM

■ sysCLOCK Analog PLLs and DLLs

- Two DLLs and up to ten PLLs per device

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells

- Dedicated read/write levelling functionality
- Dedicated gearing logic
- Source synchronous standards support
 - ADC/DAC, 7:1 LVDS, XGMII
 - High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs

■ Programmable sysI/O™ Buffer Supports Wide Range of Interfaces

- On-chip termination
- Optional equalization filter on inputs
- LVTTL and LVCMOS 33/25/18/15/12
- SSTL 33/25/18/15 I, II
- HSTL15 I and HSTL18 I, II
- PCI and Differential HSTL, SSTL
- LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

■ Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

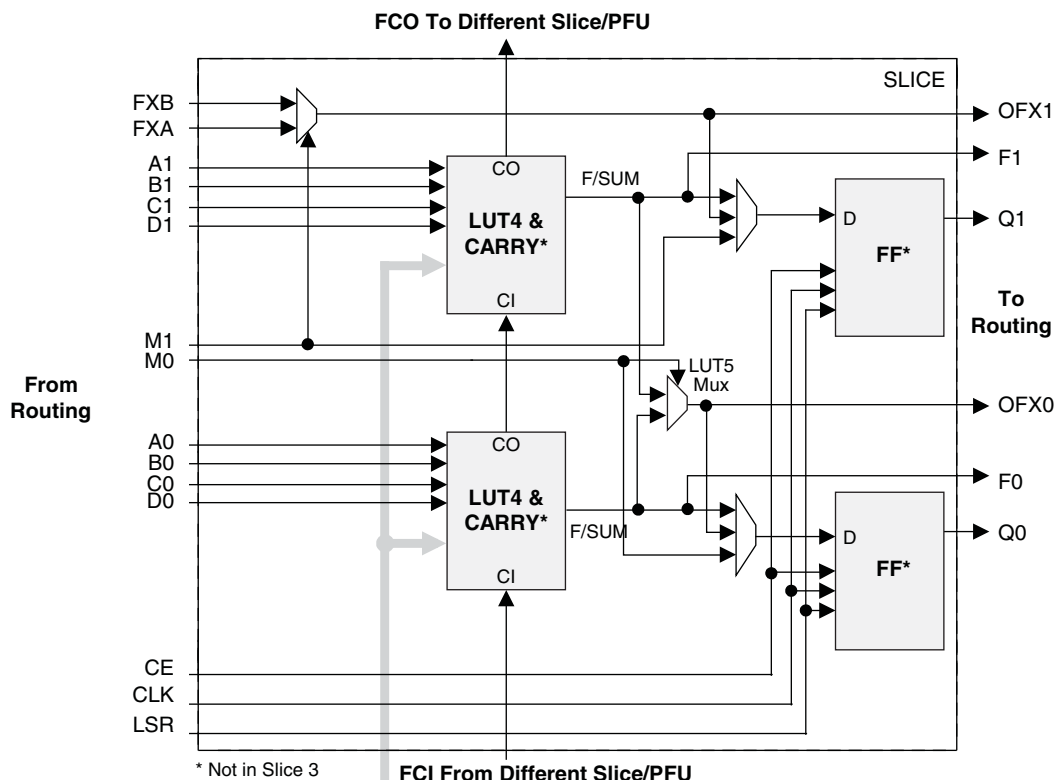
■ System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- On-chip oscillator for initialization & general use
- 1.2 V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

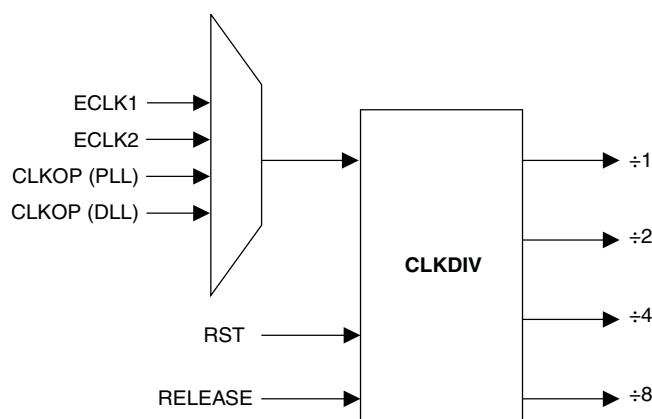
Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Figure 2-8. Clock Divider Connections



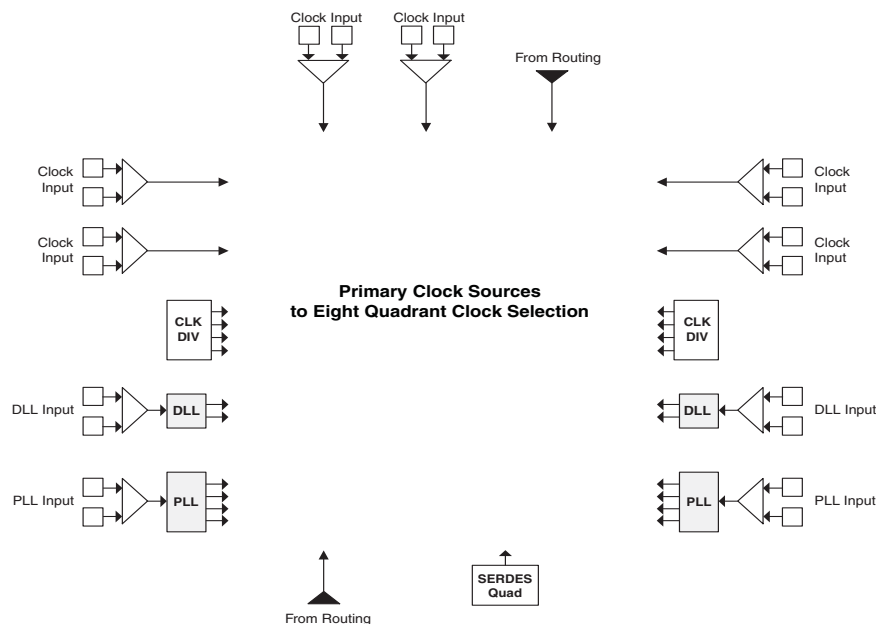
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17

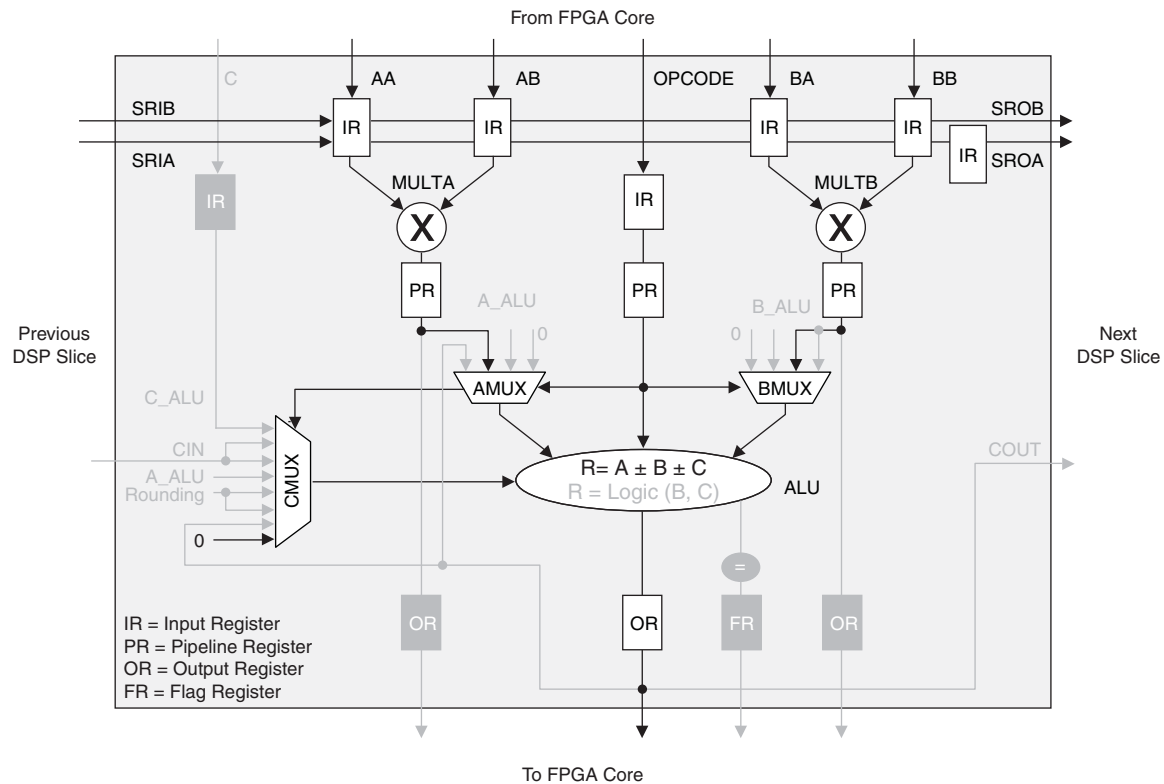


Note: Clock inputs can be configured in differential or single-ended mode.

MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB



ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

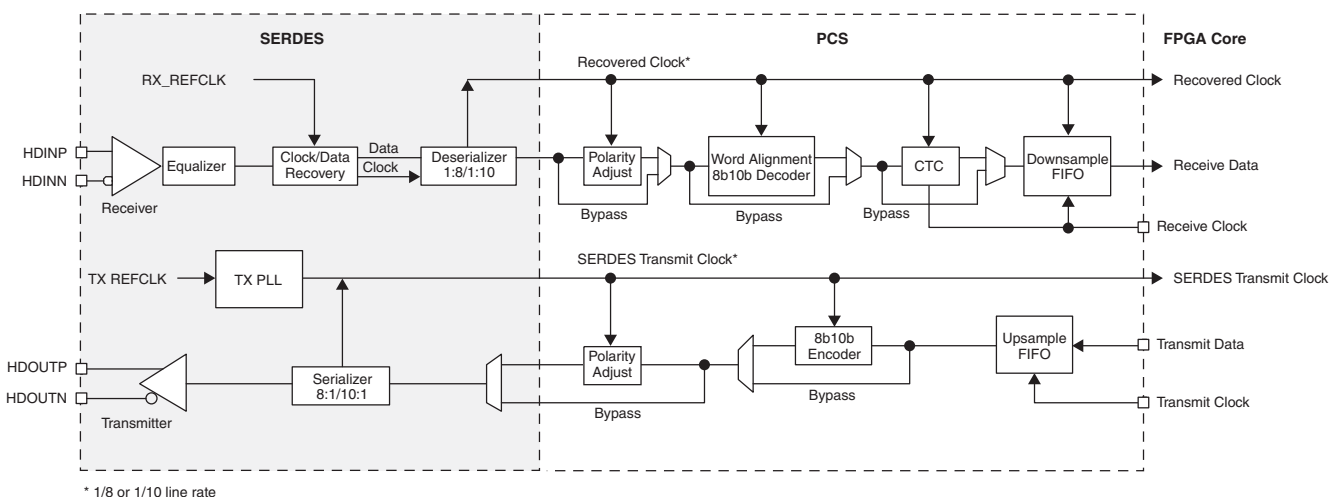
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS25 Multi-point Output Example

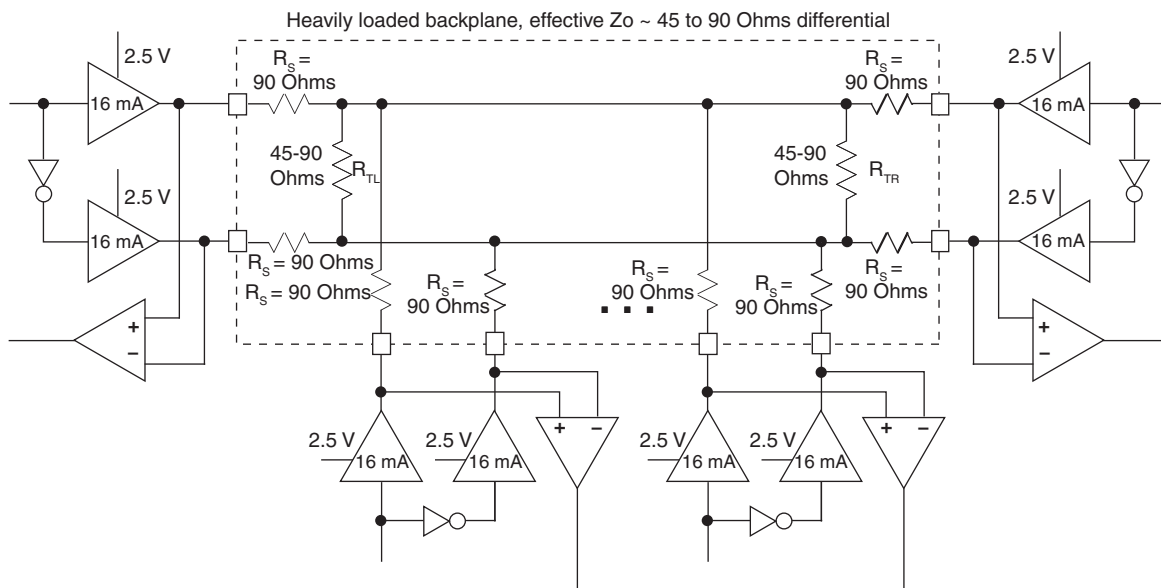


Table 3-2. BLVDS25 DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
VCCIO	Output Driver Supply (+/- 5%)	2.50	2.50	V
ZOUT	Driver Impedance	10.00	10.00	Ω
RS	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
RTL	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
RTR	Receiver Termination (+/- 1%)	45.00	90.00	Ω
VOH	Output High Voltage	1.38	1.48	V
VOL	Output Low Voltage	1.12	1.02	V
VOD	Output Differential Voltage	0.25	0.46	V
VCM	Output Common Mode Voltage	1.25	1.25	V
IDC	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

Register-to-Register Performance^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	500	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	400	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	260	MHz

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	—	4.1	—	4.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	—	1.4	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	—	1.5	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	—	500	—	420	—	375	MHz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting²									
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.3	—	3.6	—	3.9	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SU_DELP}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
t _{H_DELP}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.3	—	3.5	—	3.8	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.8	—	0.9	—	ns

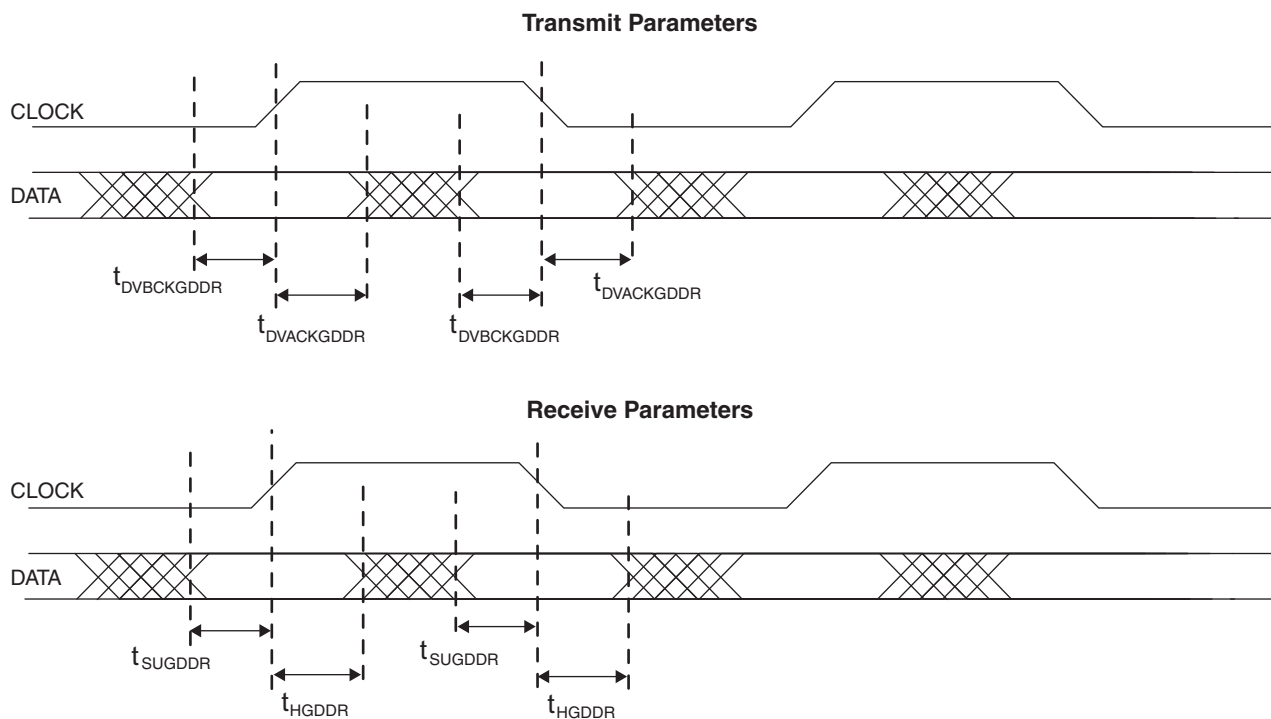
LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered) ¹⁰									
Left and Right Sides									
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered) ⁴									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing									
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	–90	90	–90	90	–90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jit-ter During DLL Locking Period	All ECP3 Devices	—	180	—	180	—	180	ps

- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
- General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
- Generic DDR timing numbers based on LVDS I/O.
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
- DDR3 timing numbers based on SSTL15.
- Uses LVDS I/O standard.
- The current version of software does not support per bank skew numbers; this will be supported in a future release.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- Using settings generated by IPexpress.
- These numbers are generated using best case PLL located in the center of the device.
- Uses SSTL25 Class II Differential I/O Standard.
- All numbers are generated with ispLEVER 8.1 software.
- For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Figure 3-8. Generic DDRX1/DDR2 (With Clock Center on Data Window)



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7}

Over Recommended Commercial Operating Conditions

Buffer Type	Description	–8	–7	–6	Units
Input Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	–0.01	–0.03	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	–0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	–0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	–0.04	ns
RS25	RS25, VCCIO = 2.5 V	0.03	–0.01	–0.03	ns
PPLVDS	Point-to-Point LVDS	0.03	–0.01	–0.03	ns
TRLVDS	Transition-Reduced LVDS	0.03	0.00	–0.04	ns
Mini MLVDS	Mini LVDS	0.03	–0.01	–0.03	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns
LVTTTL33	LVTTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC33	LVC33, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC25	LVC25, VCCIO = 2.5 V	0.00	0.00	0.00	ns
LVC18	LVC18, VCCIO = 1.8 V	–0.13	–0.13	–0.13	ns
LVC15	LVC15, VCCIO = 1.5 V	–0.07	–0.07	–0.07	ns
LVC12	LVC12, VCCIO = 1.2 V	–0.20	–0.19	–0.19	ns
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns
Output Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns
LVDS25	LVDS, VCCIO = 2.5 V	–0.11	–0.07	–0.03	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns

Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-14. Jitter Transfer – 3.125 Gbps

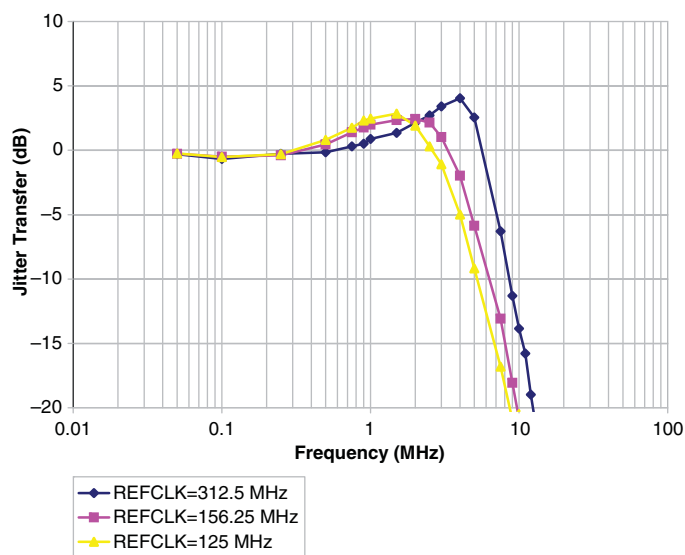


Figure 3-15. Jitter Transfer – 2.5 Gbps

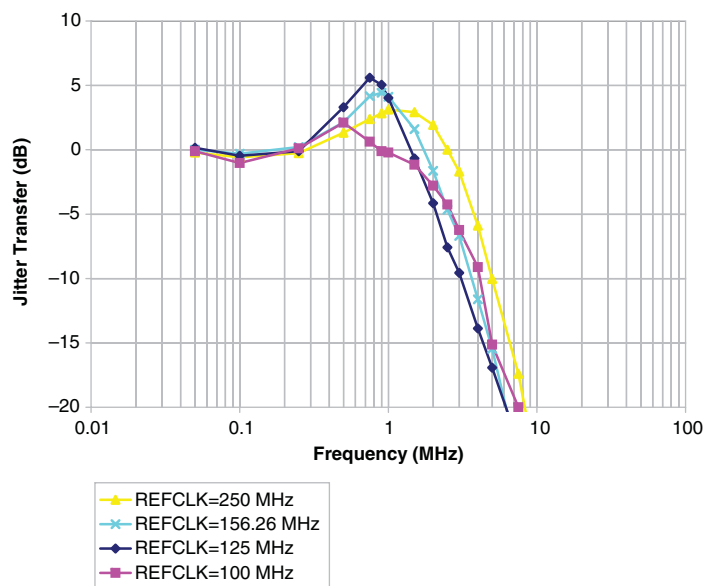
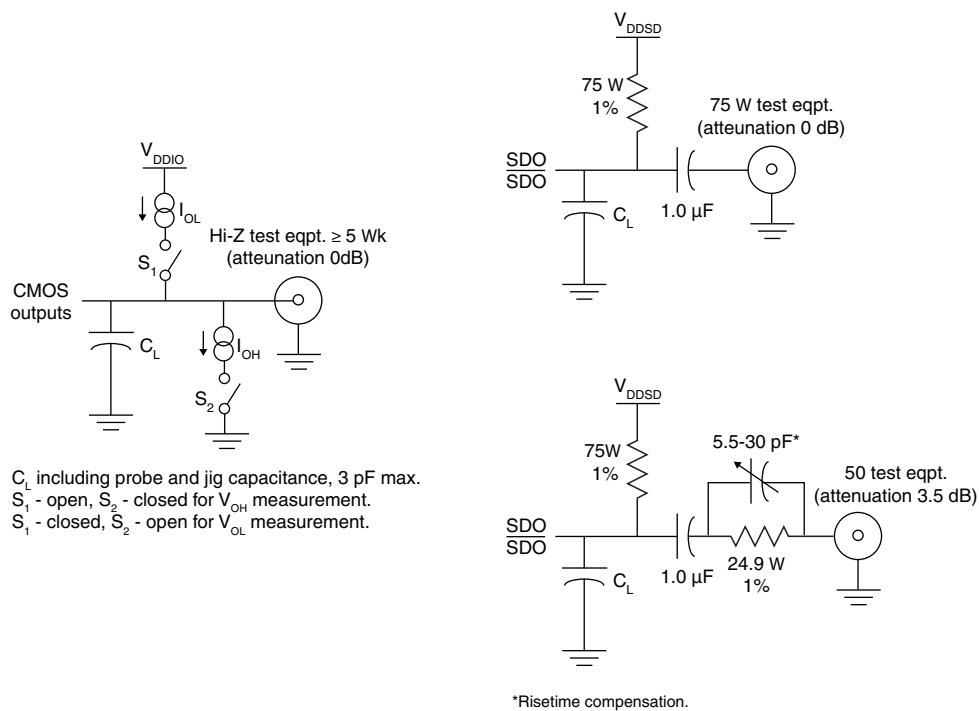


Figure 3-19. Test Loads

Test Loads



Timing Jitter Bandpass

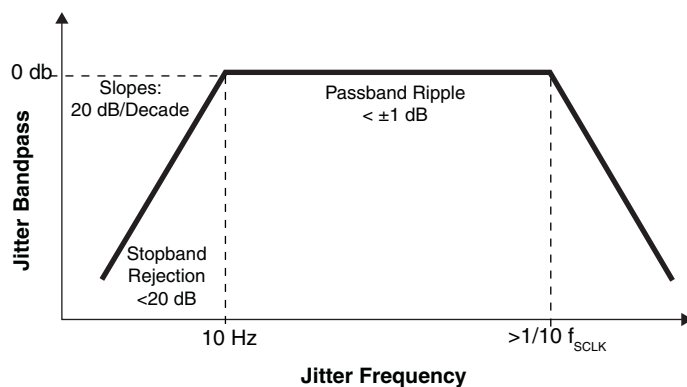
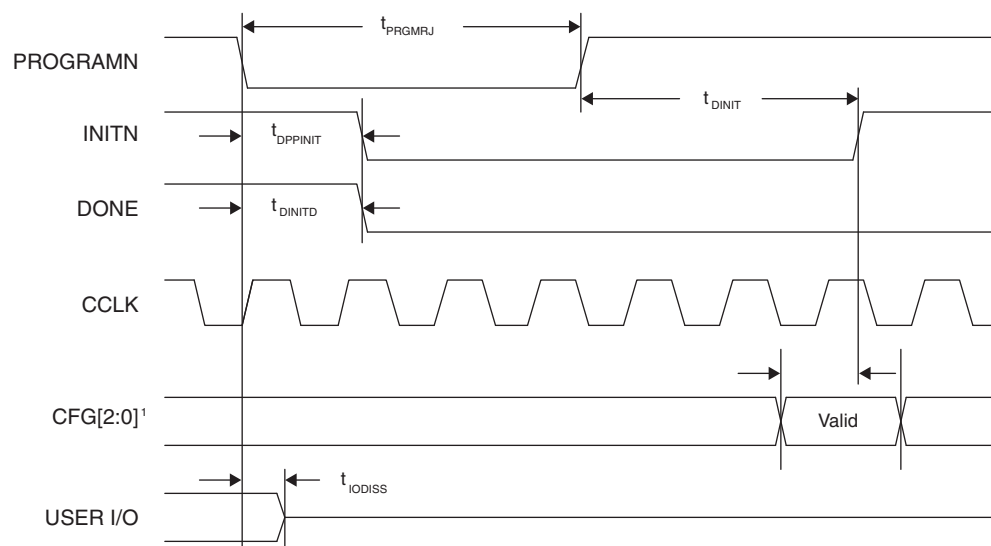
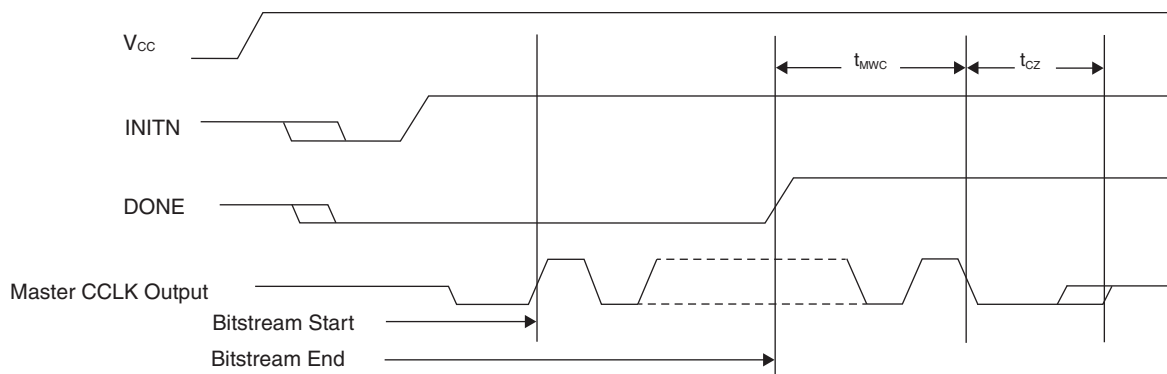


Figure 3-26. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-27. Wake-Up Timing

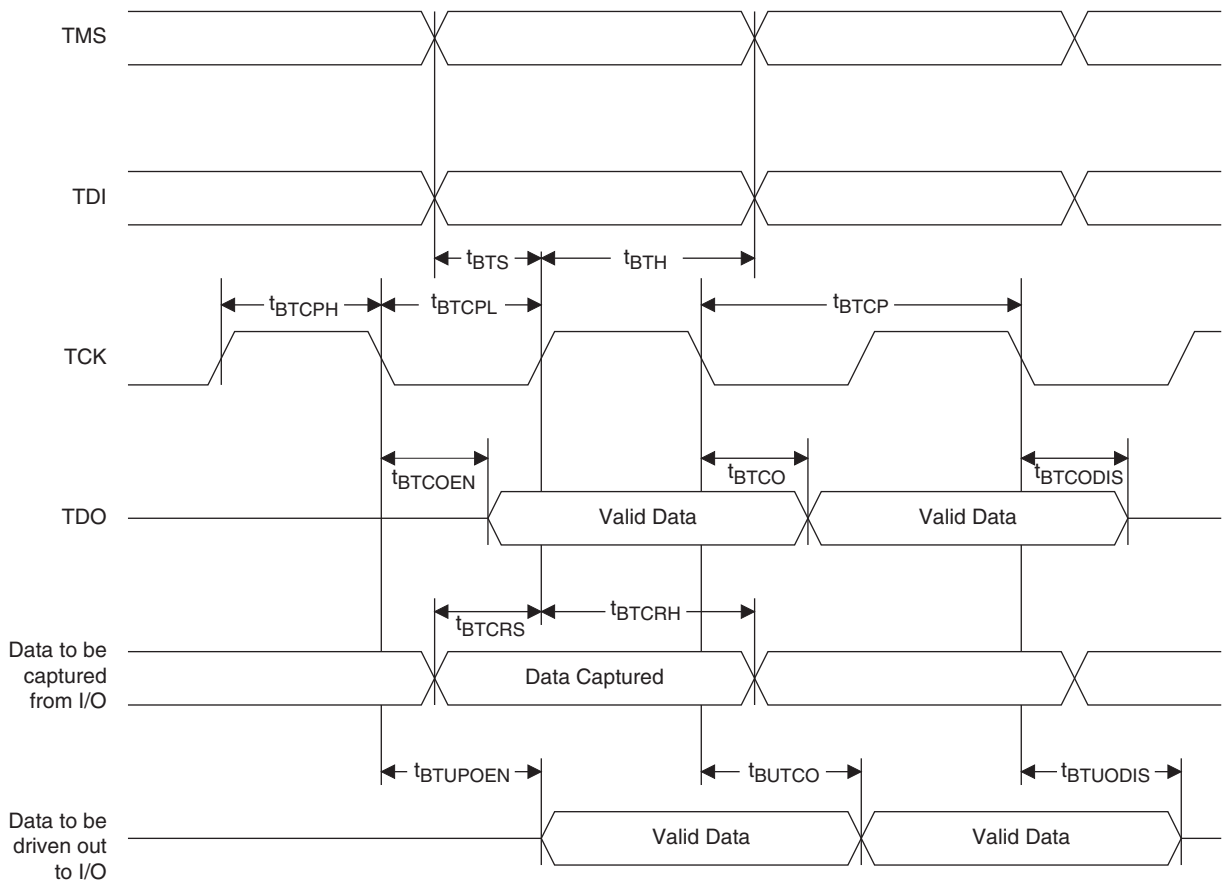


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-32. JTAG Port Timing Waveforms



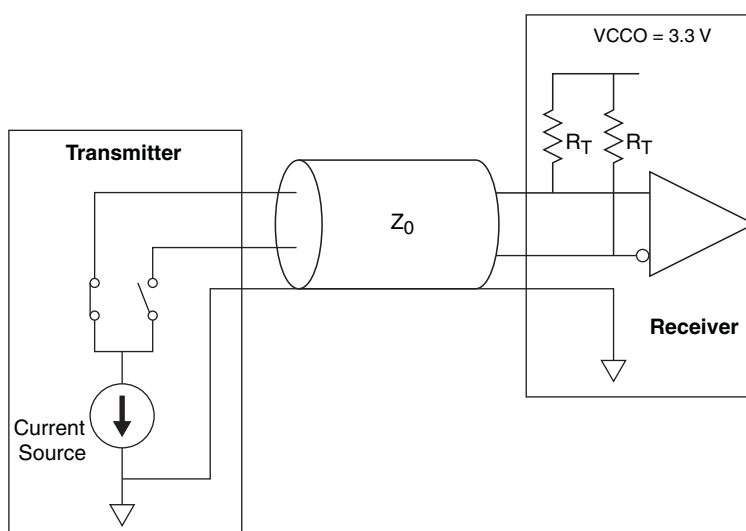
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $ V_{OP} - V_{OM} $	300	—	600	mV
V_{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD} , between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS} , between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $ V_{INP} - V_{INM} $	200	—	600	mV
V_{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	$0.3 + (V_{THD}/2)$	—	$2.1 - (V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank ²	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.

2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	–6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	–7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	–8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	–6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	–7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	–8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.