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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7lfn484i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7lfn484i</a>

## Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

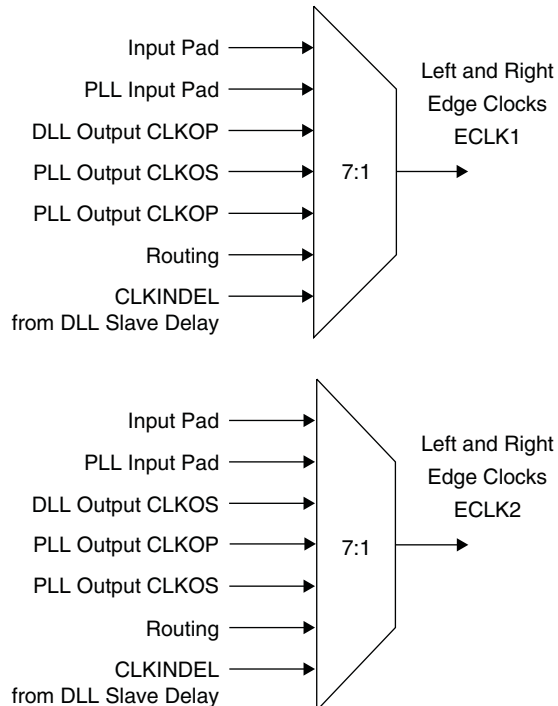
The LatticeECP3 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

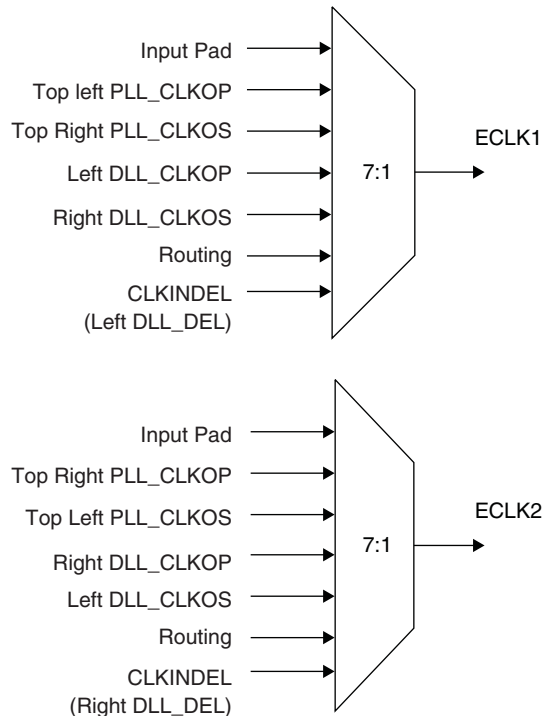
The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

**Figure 2-20. Sources of Edge Clock (Left and Right Edges)**



**Figure 2-21. Sources of Edge Clock (Top Edge)**



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

## Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

## DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

### Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

### Bottom Edge

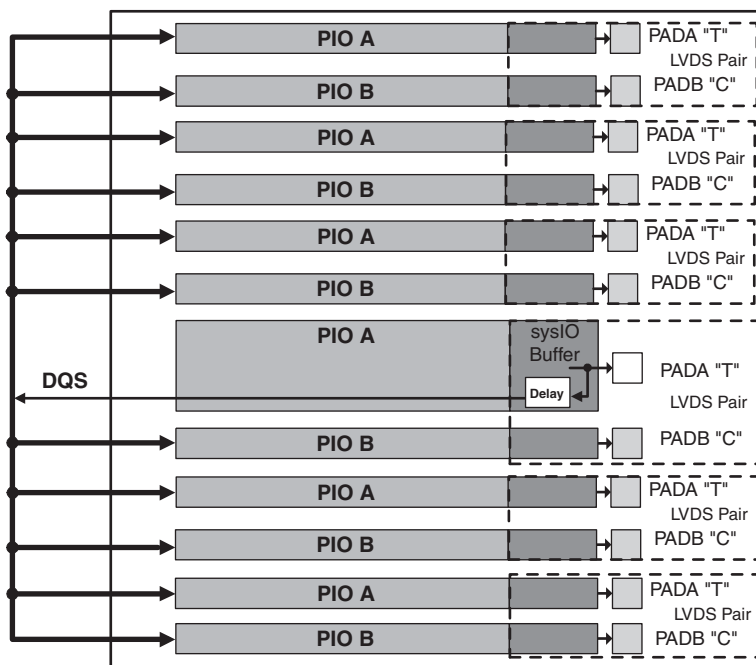
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

### Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

**Figure 2-35. DQS Grouping on the Left, Right and Top Edges**



## sysI/O Recommended Operating Conditions

Standard	V <sub>CCIO</sub>			V <sub>REF</sub> (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS33 <sup>2</sup>	3.135	3.3	3.465	—	—	—
LVC MOS33D	3.135	3.3	3.465	—	—	—
LVC MOS25 <sup>2</sup>	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 <sup>2</sup>	1.14	1.2	1.26	—	—	—
LV TTL33 <sup>2</sup>	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15 <sup>3</sup>	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II <sup>2</sup>	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II <sup>2</sup>	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II <sup>2</sup>	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I <sup>2</sup>	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II <sup>2</sup>	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 <sup>2</sup>	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
LVPECL33 <sup>1, 2</sup>	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
RSDS <sup>2</sup>	2.375	2.5	2.625	—	—	—
RSDSE <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D <sup>3</sup>	1.43	1.5	1.57	—	—	—
SSTL18D_I <sup>2, 3</sup> , II <sup>2, 3</sup>	1.71	1.8	1.89	—	—	—
SSTL25D_I <sup>2</sup> , II <sup>2</sup>	2.375	2.5	2.625	—	—	—
SSTL33D_I <sup>2</sup> , II <sup>2</sup>	3.135	3.3	3.465	—	—	—
HSTL15D_I <sup>2</sup>	1.425	1.5	1.575	—	—	—
HSTL18D_I <sup>2</sup> , II <sup>2</sup>	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. For input voltage compatibility, see TN1177, [LatticeECP3 sysIO Usage Guide](#).

3. VREF is required when using Differential SSTL to interface to DDR memory.

## sysI/O Differential Electrical Characteristics

### LVDS25

#### Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}^1, V_{INM}^1$	Input Voltage		0	—	2.4	V
$V_{CM}^1$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
$V_{THD}$	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
$I_{IN}$	Input Current	Power On or Power Off	—	—	+/-10	$\mu$ A
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100 \text{ Ohm}$	—	1.38	1.60	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100 \text{ Ohm}$	0.9 V	1.03	—	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100 \text{ Ohm}$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low		—	—	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100 \text{ Ohm}$	1.125	1.20	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between H and L		—	—	50	mV
$I_{SAB}$	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

1, On the left and right sides of the device, this specification is valid only for  $V_{CCIO} = 2.5 \text{ V}$  or  $3.3 \text{ V}$ .

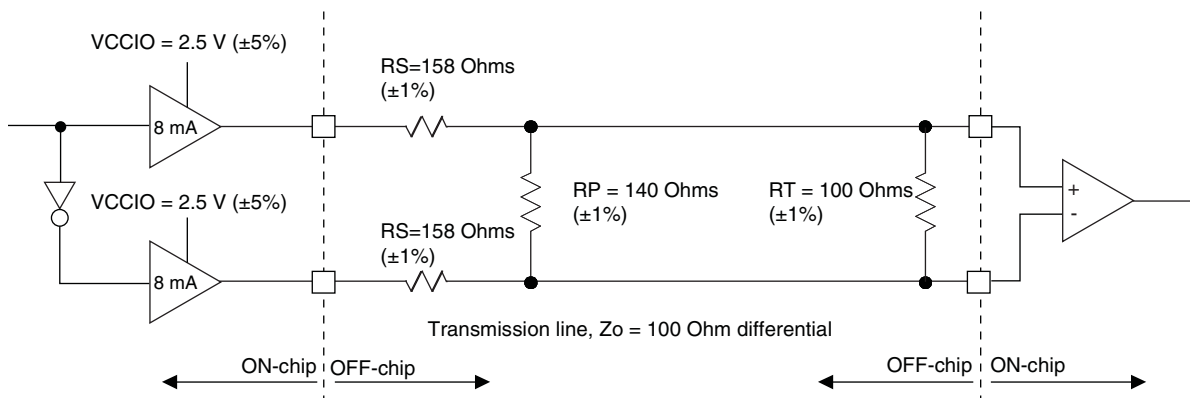
### Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

### LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

**Figure 3-1. LVDS25E Output Termination Example**



**Table 3-1. LVDS25E DC Conditions**

Parameter	Description	Typical	Units
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	V
Z <sub>OUT</sub>	Driver Impedance	20	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	158	Ω
R <sub>P</sub>	Driver Parallel Resistor (+/-1%)	140	Ω
R <sub>T</sub>	Receiver Termination (+/-1%)	100	Ω
V <sub>OH</sub>	Output High Voltage	1.43	V
V <sub>OL</sub>	Output Low Voltage	1.07	V
V <sub>OD</sub>	Output Differential Voltage	0.35	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	V
Z <sub>BACK</sub>	Back Impedance	100.5	Ω
I <sub>DC</sub>	DC Output Current	6.03	mA

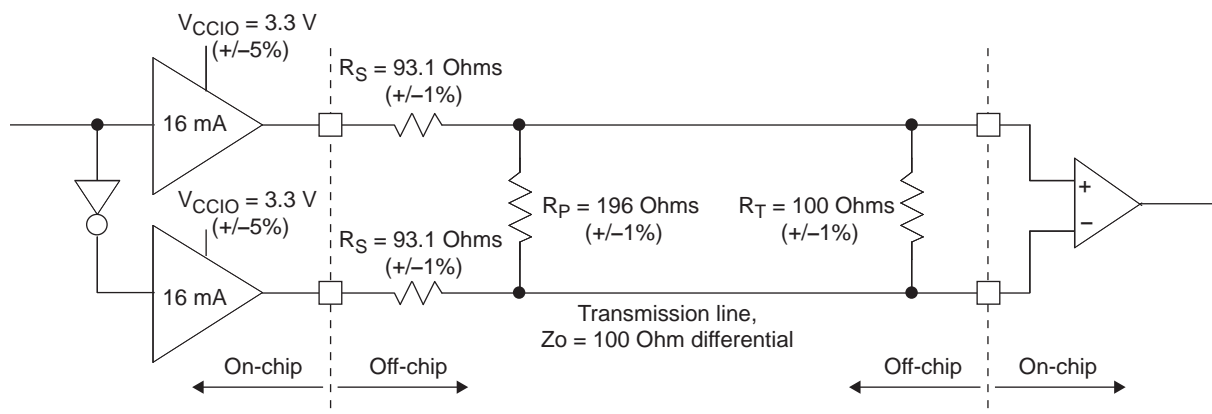
### LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V<sub>CCIO</sub>. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

### LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

**Figure 3-3. Differential LVPECL33**



**Table 3-3. LVPECL33 DC Conditions<sup>1</sup>**

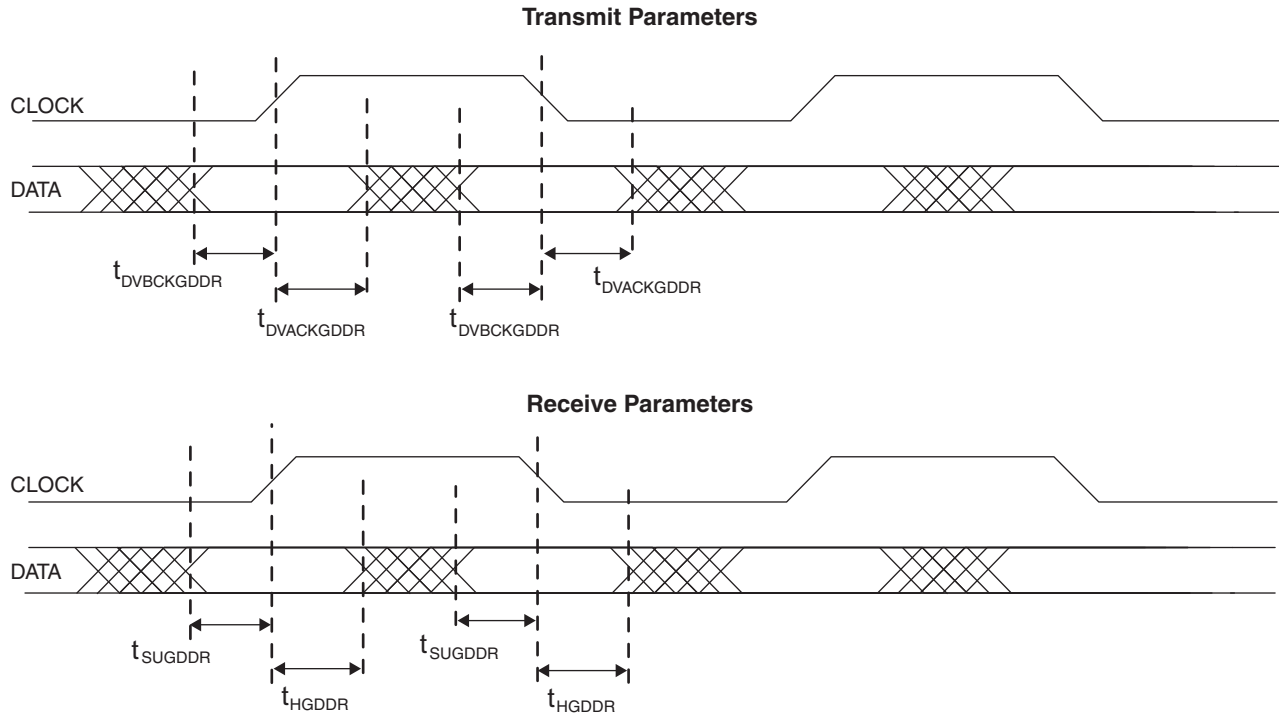
#### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
$V_{CCIO}$	Output Driver Supply (+/-5%)	3.30	V
$Z_{OUT}$	Driver Impedance	10	$\Omega$
$R_S$	Driver Series Resistor (+/-1%)	93	$\Omega$
$R_P$	Driver Parallel Resistor (+/-1%)	196	$\Omega$
$R_T$	Receiver Termination (+/-1%)	100	$\Omega$
$V_{OH}$	Output High Voltage	2.05	V
$V_{OL}$	Output Low Voltage	1.25	V
$V_{OD}$	Output Differential Voltage	0.80	V
$V_{CM}$	Output Common Mode Voltage	1.65	V
$Z_{BACK}$	Back Impedance	100.5	$\Omega$
$I_{DC}$	DC Output Current	12.11	mA

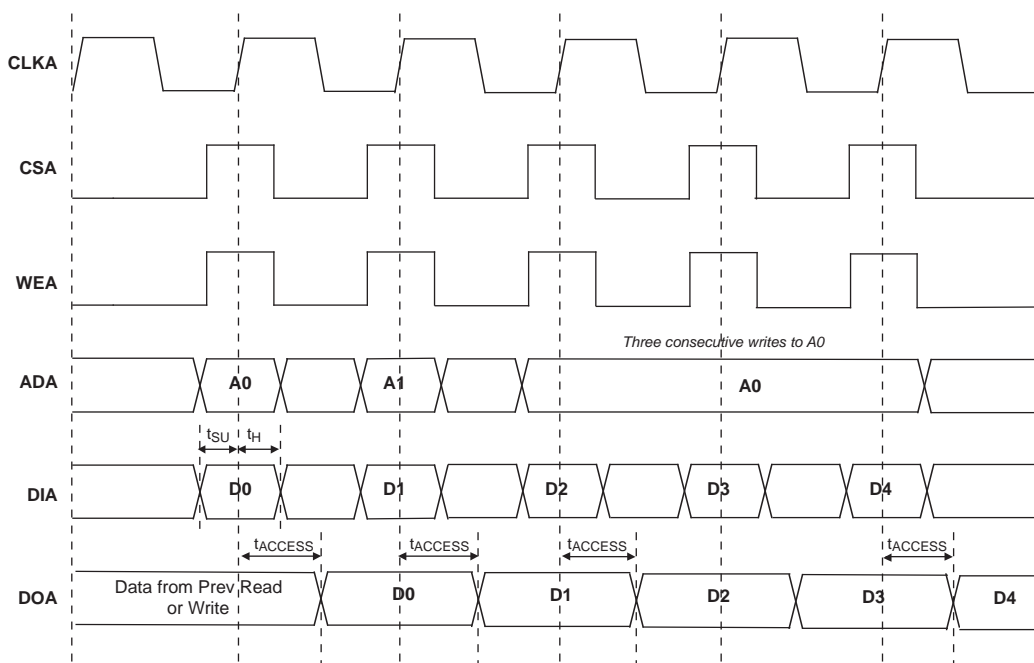
1. For input buffer, see LVDS table.



**Figure 3-8. Generic DDRX1/DDR2 (With Clock Center on Data Window)**



**Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)**



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

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**LatticeECP3 Maximum I/O Buffer Speed (Continued)<sup>1, 2, 3, 4, 5, 6</sup>****Over Recommended Operating Conditions**

Buffer	Description	Max.	Units
PCI33	PCI, $V_{CCIO} = 3.3\text{ V}$	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

### SERDES High Speed Data Receiver

**Table 3-9. Serial Input Data Specifications**

Symbol	Description	Min.	Typ.	Max.	Units
RX-CID <sub>S</sub>	Stream of nontransitions <sup>1</sup> (CID = Consecutive Identical Digits) @ 10 <sup>-12</sup> BER	3.125 G	—	136	Bits
		2.5 G	—	144	
		1.485 G	—	160	
		622 M	—	204	
		270 M	—	228	
		150 M	—	296	
V <sub>RX-DIFF-S</sub>	Differential input sensitivity	150	—	1760	mV, p-p
V <sub>RX-IN</sub>	Input levels	0	—	V <sub>CCA</sub> +0.5 <sup>4</sup>	V
V <sub>RX-CM-DC</sub>	Input common mode range (DC coupled)	0.6	—	V <sub>CCA</sub>	V
V <sub>RX-CM-AC</sub>	Input common mode range (AC coupled) <sup>3</sup>	0.1	—	V <sub>CCA</sub> +0.2	V
T <sub>RX-RELOCK</sub>	SCDR re-lock time <sup>2</sup>	—	1000	—	Bits
Z <sub>RX-TERM</sub>	Input termination 50/75 Ohm/High Z	-20%	50/75/HiZ	+20%	Ohms
RL <sub>RX-RL</sub>	Return loss (without package)	10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.

2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.

3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.

4. Up to 1.76 V.

### Input Data Jitter Tolerance

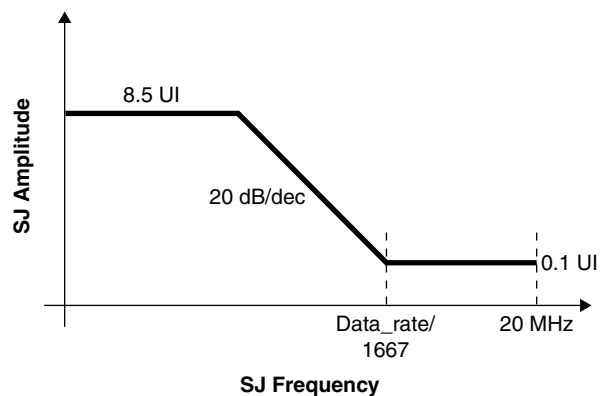
A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

**Table 3-10. Receiver Total Jitter Tolerance Specification**

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

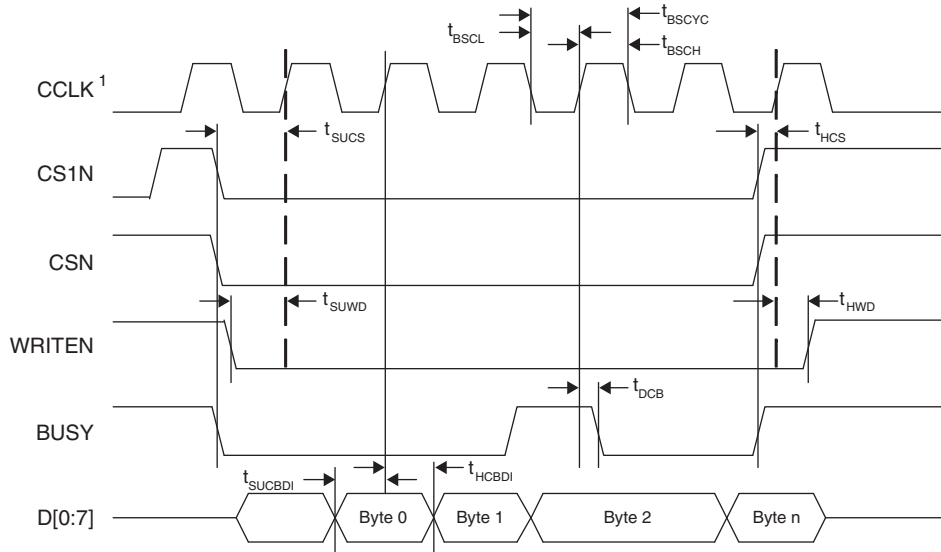
Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



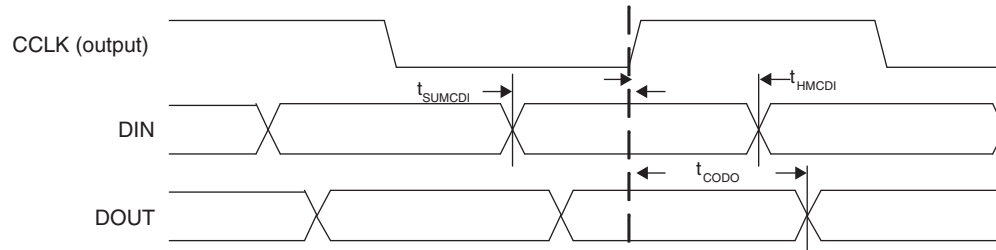
Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

**Figure 3-21. sysCONFIG Parallel Port Write Cycle**

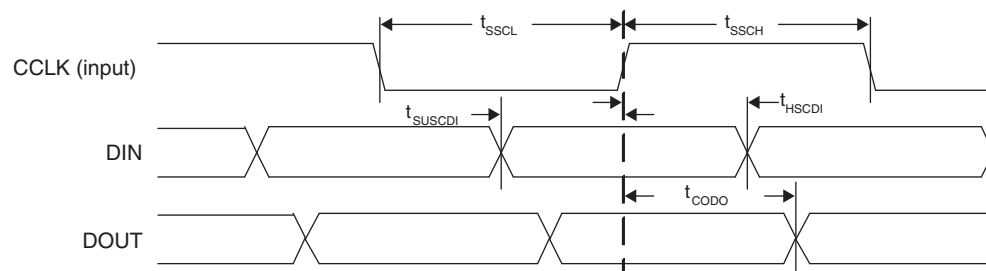


1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

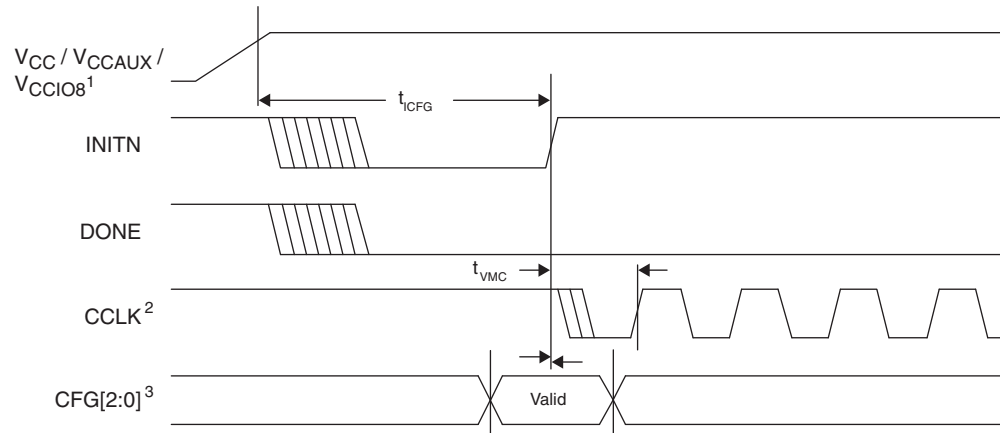
**Figure 3-22. sysCONFIG Master Serial Port Timing**



**Figure 3-23. sysCONFIG Slave Serial Port Timing**

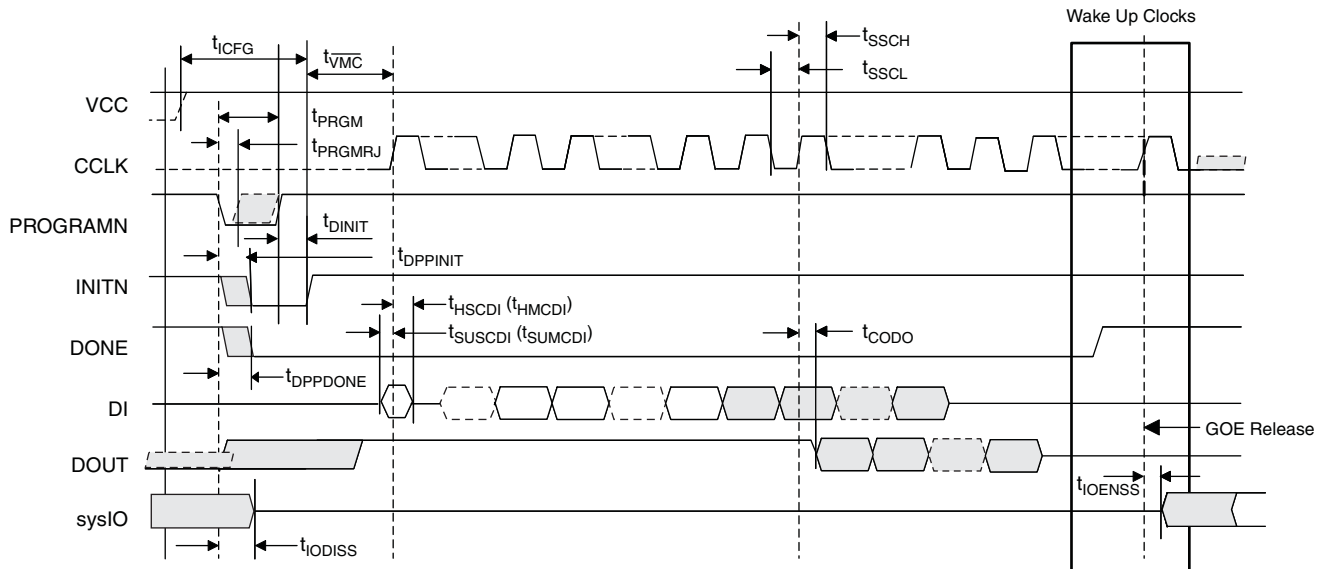


**Figure 3-24. Power-On-Reset (POR) Timing**

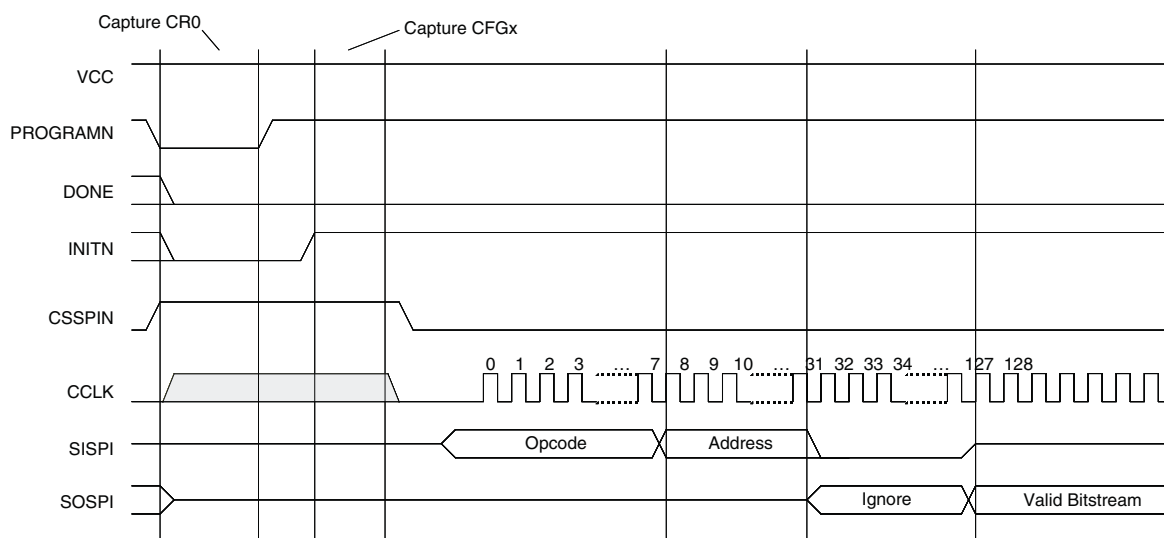


1. Time taken from  $V_{CC}$ ,  $V_{CCAUX}$  or  $V_{CCIO8}$ , whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPI<sub>m</sub>).
3. The CFG pins are normally static (hard wired).

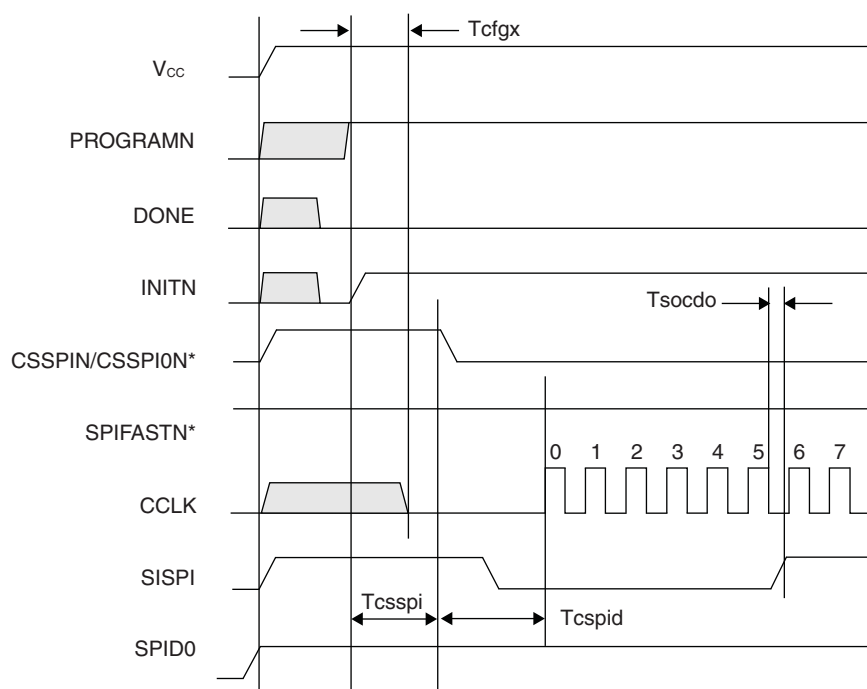
**Figure 3-25. sysCONFIG Port Timing**



**Figure 3-28. Master SPI Configuration Waveforms**



**Figure 3-29. Master SPI POR Waveforms**

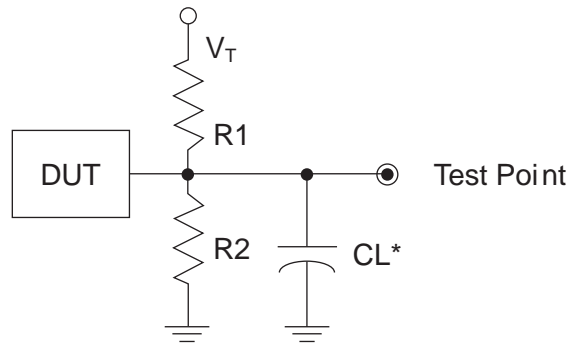




## Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

**Figure 3-33. Output Test Load, LVTTTL and LVCMOS Standards**



\*CL Includes Test Fixture and Probe Capacitance

**Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and other LVCMOS settings (L -> H, H -> L)	$\infty$	$\infty$	0 pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	$\infty$	1M $\Omega$	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1 M $\Omega$	$\infty$	0 pF	$V_{CCIO}/2$	$V_{CCIO}$
LVCMOS 2.5 I/O (H -> Z)	$\infty$	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L -> Z)	100	$\infty$	0 pF	$V_{OL} + 0.10$	$V_{CCIO}$

Note: Output test conditions for all other interfaces are determined by the respective standards.

### Signal Descriptions

Signal Name	I/O	Description
<b>General Purpose</b>		
P[Edge] [Row/Column Number]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Column Number. When Edge is L (Left) or R (Right), only need to specify Row Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
P[Edge][Row Number]E_[A/B/C/D]	I	These general purpose signals are input-only pins and are located near the PLLs.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V <sub>CC</sub>	—	Power supply pins for core logic. Dedicated pins.
V <sub>CCAUX</sub>	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V <sub>CCIOx</sub>	—	Dedicated power supply pins for I/O bank x.
V <sub>CCA</sub>	—	SERDES, transmit, receive, PLL and reference clock buffer power supply. All V <sub>CCA</sub> supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect V <sub>CCA</sub> to V <sub>CC</sub> .
V <sub>CCPLL</sub> _[LOC]	—	General purpose PLL supply pins where LOC=L (left) or R (right).
V <sub>REF1_x</sub> , V <sub>REF2_x</sub>	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V <sub>REF</sub> inputs. When not used, they may be used as I/O pins.
VTTx	—	Power supply for on-chip termination of I/Os.
XRES <sup>1</sup>	—	10 kOhm +/-1% resistor must be connected between this pad and ground.
<b>PLL, DLL and Clock Functions</b>		
[LOC][num]_GPLL[T, C]_IN_[index]	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_[index]	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC]0_GDLLT_IN_[index] <sup>2</sup>	I/O	General Purpose DLL (GDLL) input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
[LOC]0_GDLLT_FB_[index] <sup>2</sup>	I/O	Optional feedback GDLL input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
PCLK[T, C][n:0]_[3:0] <sup>2</sup>	I/O	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.

## Pin Information Summary

Pin Information Summary		ECP3-17EA			ECP3-35EA			ECP3-70EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	20	36	26	42	48	42	60	86
	Bank 1	14	10	24	14	36	36	36	48	78
	Bank 2	6	7	12	6	24	24	24	34	36
	Bank 3	18	12	44	16	54	59	54	59	86
	Bank 6	20	11	44	18	63	61	63	67	86
	Bank 7	19	26	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4	4	8	8
	Bank 3	0	0	0	2	4	4	4	12	12
	Bank 6	0	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0	0
General Purpose Out- puts per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310	295	380	490
VCC		6	16	16	6	16	32	16	32	32
VCCAUX		4	5	8	4	8	12	8	12	16
VTT		4	7	4	4	4	4	4	4	8
VCCA		4	6	4	4	4	8	4	8	16
VCCPLL		2	2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	3	2	2	2	4	2	4	4
	Bank 1	2	3	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	2	4	2	4	4
	Bank 3	2	3	2	2	2	4	2	4	4
	Bank 6	2	3	2	2	2	4	2	4	4
	Bank 7	2	3	2	2	2	4	2	4	4
	Bank 8	1	2	2	1	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139	98	139	233
NC		0	0	73	0	0	96	0	0	238
Reserved <sup>1</sup>		0	0	2	0	2	2	2	2	2
SERDES		26	18	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672	484	672	1156

Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break-down table.
		Pinout Information	“Logic Signal Connections” section heading renamed “Package Pinout Information”. Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V <sub>CCA</sub> signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for t <sub>RST</sub> .
		Ordering Information	Updated topside marks with new logos in the Ordering Information section.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL Timing table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, t <sub>JIT</sub> .
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t <sub>SUWREN_EBR</sub> and t <sub>HWREN_EBR</sub> .
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications

Date	Version	Section	Change Summary
February 2009	01.0		Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for $t_{\text{SKEW\_PRIB}}$ to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{\text{DINIT}}$ information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{\text{RX-DIFF-S}}$ .
			Added footnote 4 to sysCLOCK PLL Timing table for $t_{\text{PFD}}$ .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	—	Initial release.