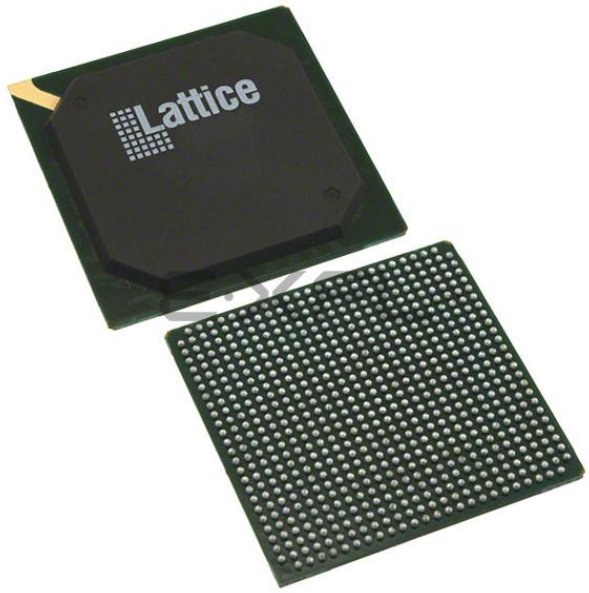
# Lattice Semiconductor Corporation - LFE3-70EA-7LFN672C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 8375 |
| Number of Logic Elements/Cells | 67000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 380 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-7lfn672c |

# LatticeECP3 Family Data Sheet Introduction

February 2012 Data Sheet DS1021

## Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

***Table 1-1. LatticeECP3™ Family Selection Guide***

| Device | ECP3-17 | ECP3-35 | ECP3-70 | ECP3-95 | ECP3-150 |
|---|---|---|---|---|---|
| LUTs (K) | 17 | 33 | 67 | 92 | 149 |
| sysMEM Blocks (18 Kbits) | 38 | 72 | 240 | 240 | 372 |
| Embedded Memory (Kbits) | 700 | 1327 | 4420 | 4420 | 6850 |
| Distributed RAM Bits (Kbits) | 36 | 68 | 145 | 188 | 303 |
| 18 x 18 Multipliers | 24 | 64 | 128 | 128 | 320 |
| SERDES (Quad) | 1 | 1 | 3 | 3 | 4 |
| PLLs/DLLs | 2 / 2 | 4 / 2 | 10 / 2 | 10 / 2 | 10 / 2 |
| **Packages and SERDES Channels/ I/O Combinations** | | | | | |
| 328 csBGA (10 x 10 mm) | 2 / 116 | | | | |
| 256 ftBGA (17 x 17 mm) | 4 / 133 | 4 / 133 | | | |
| 484 fpBGA (23 x 23 mm) | 4 / 222 | 4 / 295 | 4 / 295 | 4 / 295 | |
| 672 fpBGA (27 x 27 mm) | | 4 / 310 | 8 / 380 | 8 / 380 | 8 / 380 |
| 1156 fpBGA (35 x 35 mm) | | | 12 / 490 | 12 / 490 | 16 / 586 |

# Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

### Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

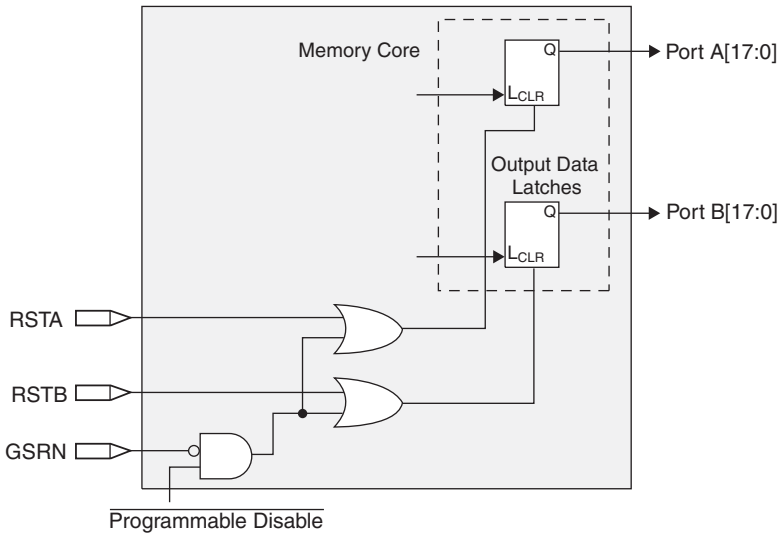
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

### Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

***Figure 2-22. Memory Core Reset***




For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

## sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

## Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO8}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

## Supported sysI/O Standards

The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

## Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

## External Resistor

LatticeECP3 devices require a single external, 10 kOhm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

## On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/– 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

## LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical | | Units |
|---|---|---|---|---|---|
| | | | –6L, –7L, –8L | –6, –7, –8 | |
| $I_{CC}$ | Core Power Supply Current | ECP-17EA | 29.8 | 49.4 | mA |
| | | ECP3-35EA | 53.7 | 89.4 | mA |
| | | ECP3-70EA | 137.3 | 230.7 | mA |
| | | ECP3-95EA | 137.3 | 230.7 | mA |
| | | ECP3-150EA | 219.5 | 370.9 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP-17EA | 18.3 | 19.4 | mA |
| | | ECP3-35EA | 19.6 | 23.1 | mA |
| | | ECP3-70EA | 26.5 | 32.4 | mA |
| | | ECP3-95EA | 26.5 | 32.4 | mA |
| | | ECP3-150EA | 37.0 | 45.7 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (Per PLL) | ECP-17EA | 0.0 | 0.0 | mA |
| | | ECP3-35EA | 0.1 | 0.1 | mA |
| | | ECP3-70EA | 0.1 | 0.1 | mA |
| | | ECP3-95EA | 0.1 | 0.1 | mA |
| | | ECP3-150EA | 0.1 | 0.1 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP-17EA | 1.3 | 1.4 | mA |
| | | ECP3-35EA | 1.3 | 1.4 | mA |
| | | ECP3-70EA | 1.4 | 1.5 | mA |
| | | ECP3-95EA | 1.4 | 1.5 | mA |
| | | ECP3-150EA | 1.4 | 1.5 | mA |
| $I_{CCJ}$ | JTAG Power Supply Current | All Devices | 2.5 | 2.5 | mA |
| $I_{CCA}$ | Transmit, Receive, PLL and Reference Clock Buffer Power Supply | ECP-17EA | 6.1 | 6.1 | mA |
| | | ECP3-35EA | 6.1 | 6.1 | mA |
| | | ECP3-70EA | 18.3 | 18.3 | mA |
| | | ECP3-95EA | 18.3 | 18.3 | mA |
| | | ECP3-150EA | 24.4 | 24.4 | mA |

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

# LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | All ECP3EA Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-150EA | 321 | — | 403 | — | 471 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-150EA | 321 | — | 403 | — | 471 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | 405 | — | 325 | — | 280 | MHz |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-70EA/95EA | 321 | — | 403 | — | 535 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-70EA/95EA | 321 | — | 403 | — | 535 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-70EA/95EA | — | 405 | — | 325 | — | 250 | MHz |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-35EA | 335 | — | 425 | — | 535 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-35EA | 335 | — | 425 | — | 535 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-35EA | — | 405 | — | 325 | — | 250 | MHz |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-17EA | 335 | — | 425 | — | 535 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-17EA | 335 | — | 425 | — | 535 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-17EA | — | 405 | — | 325 | — | 250 | MHz |
| **Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_RX.ECLK.Aligned)** | | | | | | | | | |
| **Left and Right Side Using DLLCLKIN Pin for Clock Input** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | 460 | — | 385 | — | 345 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70EA/95EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70EA/95EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-70EA/95EA | — | 460 | — | 385 | — | 311 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-35EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-35EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-35EA | — | 460 | — | 385 | — | 311 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-17EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-17EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-17EA | — | 460 | — | 385 | — | 311 | MHz |
| **Top Side Using PCLK Pin for Clock Input** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70EA/95EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70EA/95EA | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-70EA/95EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-35EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-35EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-35EA | — | 235 | — | 170 | — | 130 | MHz |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-17EA | — | 0.210 | — | 0.210 | — | 0.210 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-17EA | 0.790 | — | 0.790 | — | 0.790 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-17EA | — | 235 | — | 170 | — | 130 | MHz |

# LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-35EA | 683 | — | 688 | — | 690 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-35EA | 683 | — | 688 | — | 690 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-17EA | 683 | — | 688 | — | 690 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-17EA | 683 | — | 688 | — | 690 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Output with Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned)[10]** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-150EA | — | 335 | — | 338 | — | 341 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-150EA | — | 335 | — | 338 | — | 341 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-70EA/95EA | — | 339 | — | 343 | — | 347 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-70EA/95EA | — | 339 | — | 343 | — | 347 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-35EA | — | 322 | — | 320 | — | 321 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-35EA | — | 322 | — | 320 | — | 321 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-17EA | — | 322 | — | 320 | — | 321 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-17EA | — | 322 | — | 320 | — | 321 | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_TX.DQS.Centered)[10]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | 670 | — | 670 | — | 670 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-70EA/95EA | 657 | — | 652 | — | 650 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-70EA/95EA | 657 | — | 652 | — | 650 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70EA/95EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-35EA | 670 | — | 675 | — | 676 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-35EA | 670 | — | 675 | — | 676 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-35EA | — | 250 | — | 250 | — | 250 | MHz |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-17EA | 670 | — | 670 | — | 670 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-17EA | 670 | — | 670 | — | 670 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-17EA | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_TX.Aligned)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | All ECP3EA Devices | — | 200 | — | 210 | — | 220 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | All ECP3EA Devices | — | 200 | — | 210 | — | 220 | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 500 | — | 420 | — | 375 | MHz |
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQSDLL.Centered)[11]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | All ECP3EA Devices | 400 | — | 400 | — | 431 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | All ECP3EA Devices | 400 | — | 400 | — | 432 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 400 | — | 400 | — | 375 | MHz |

# LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)[10]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | All ECP3EA Devices | 285 | — | 370 | — | 431 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | All ECP3EA Devices | 285 | — | 370 | — | 432 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 500 | — | 420 | — | 375 | MHz |
| **Memory Interface** | | | | | | | | | |
| **DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | All ECP3 Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | All ECP3 Devices | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | All ECP3 Devices | 95 | 200 | 95 | 200 | 95 | 166 | MHz |
| $f_{MAX\_DDR2}$ | DDR2 clock frequency | All ECP3 Devices | 125 | 266 | 125 | 200 | 125 | 166 | MHz |
| **DDR3 (Using PLL for SCLK) I/O Pin Parameters** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | All ECP3 Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | All ECP3 Devices | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR3}$ | DDR3 clock frequency | All ECP3 Devices | 300 | 400 | 266 | 333 | 266 | 300 | MHz |
| **DDR3 Clock Timing** | | | | | | | | | |
| $t_{CH}$ (avg)[9] | Average High Pulse Width | All ECP3 Devices | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | UI |
| $t_{CL}$ (avg)[9] | Average Low Pulse Width | All ECP3 Devices | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | UI |
| $t_{JIT}$ (per, lck)[9] | Output Clock Period Jitter During DLL Locking Period | All ECP3 Devices | –90 | 90 | –90 | 90 | –90 | 90 | ps |
| $t_{JIT}$ (cc, lck)[9] | Output Cycle-to-Cycle Period Jitter During DLL Locking Period | All ECP3 Devices | — | 180 | — | 180 | — | 180 | ps |

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
9. Using settings generated by IPexpress.
10. These numbers are generated using best case PLL located in the center of the device.
11. Uses SSTL25 Class II Differential I/O Standard.
12. All numbers are generated with ispLEVER 8.1 software.
13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

## sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Clock | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (CLKI, CLKFB) | | Edge clock | 2 | — | 500 | MHz |
| | | | Primary clock[4] | 2 | — | 420 | MHz |
| $f_{OUT}$ | Output clock frequency (CLKOP, CLKOS) | | Edge clock | 4 | — | 500 | MHz |
| | | | Primary clock[4] | 4 | — | 420 | MHz |
| $f_{OUT1}$ | K-Divider output frequency | CLKOK | | 0.03125 | — | 250 | MHz |
| $f_{OUT2}$ | K2-Divider output frequency | CLKOK2 | | 0.667 | — | 166 | MHz |
| $f_{VCO}$ | PLL VCO frequency | | | 500 | — | 1000 | MHz |
| $f_{PFD}$[3] | Phase detector input frequency | | Edge clock | 2 | — | 500 | MHz |
| | | | Primary clock[4] | 2 | — | 420 | MHz |
| **AC Characteristics** | | | | | | | |
| $t_{PA}$ | Programmable delay unit | | | 65 | 130 | 260 | ps |
| $t_{DT}$ | Output clock duty cycle (CLKOS, at 50% setting) | | Edge clock | 45 | 50 | 55 | % |
| | | $f_{OUT} \leq 250$ MHz | Primary clock | 45 | 50 | 55 | % |
| | | $f_{OUT} > 250$ MHz | Primary clock | 30 | 50 | 70 | % |
| $t_{CPA}$ | Coarse phase shift error (CLKOS, at all settings) | | | -5 | 0 | +5 | % of period |
| $t_{OPW}$ | Output clock pulse width high or low (CLKOS) | | | 1.8 | — | — | ns |
| $t_{OPJIT}$[1] | Output clock period jitter | $f_{OUT} \geq 420$ MHz | | — | — | 200 | ps |
| | | 420 MHz > $f_{OUT} \geq 100$ MHz | | — | — | 250 | ps |
| | | $f_{OUT} < 100$ MHz | | — | — | 0.025 | UIPP |
| $t_{SK}$ | Input clock to output clock skew when N/M = integer | | | — | — | 500 | ps |
| $t_{LOCK}$[2] | Lock time | 2 to 25 MHz | | — | — | 200 | us |
| | | 25 to 500 MHz | | — | — | 50 | us |
| $t_{UNLOCK}$ | Reset to PLL unlock time to ensure fast reset | | | — | — | 50 | ns |
| $t_{HI}$ | Input clock high time | 90% to 90% | | 0.5 | — | — | ns |
| $t_{LO}$ | Input clock low time | 10% to 10% | | 0.5 | — | — | ns |
| $t_{IPJIT}$ | Input clock period jitter | | | — | — | 400 | ps |
| $t_{RST}$ | Reset signal pulse width high, RSTK | | | 10 | — | — | ns |
| | Reset signal pulse width high, RST | | | 500 | — | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

## SERDES High Speed Data Receiver

***Table 3-9. Serial Input Data Specifications***

| Symbol | Description | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RX\text{-}CID_S$ | Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ $10^{-12}$ BER | 3.125 G | — | — | 136 | Bits |
| | | 2.5 G | — | — | 144 | |
| | | 1.485 G | — | — | 160 | |
| | | 622 M | — | — | 204 | |
| | | 270 M | — | — | 228 | |
| | | 150 M | — | — | 296 | |
| $V_{RX\text{-}DIFF\text{-}S}$ | Differential input sensitivity | | 150 | — | 1760 | mV, p-p |
| $V_{RX\text{-}IN}$ | Input levels | | 0 | — | $V_{CCA}$ +0.5[4] | V |
| $V_{RX\text{-}CM\text{-}DC}$ | Input common mode range (DC coupled) | | 0.6 | — | $V_{CCA}$ | V |
| $V_{RX\text{-}CM\text{-}AC}$ | Input common mode range (AC coupled)[3] | | 0.1 | — | $V_{CCA}$ +0.2 | V |
| $T_{RX\text{-}RELOCK}$ | SCDR re-lock time[2] | | — | 1000 | — | Bits |
| $Z_{RX\text{-}TERM}$ | Input termination 50/75 Ohm/High Z | | –20% | 50/75/HiZ | +20% | Ohms |
| $RL_{RX\text{-}RL}$ | Return loss (without package) | | 10 | — | — | dB |

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/– 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

### Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

***Table 3-10. Receiver Total Jitter Tolerance Specification***

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 2.5 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 1.25 Gbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |
| Deterministic | 622 Mbps | 600 mV differential eye | — | — | 0.47 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.18 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.65 | UI, p-p |

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

*Figure 3-16. Jitter Transfer – 1.25 Gbps*

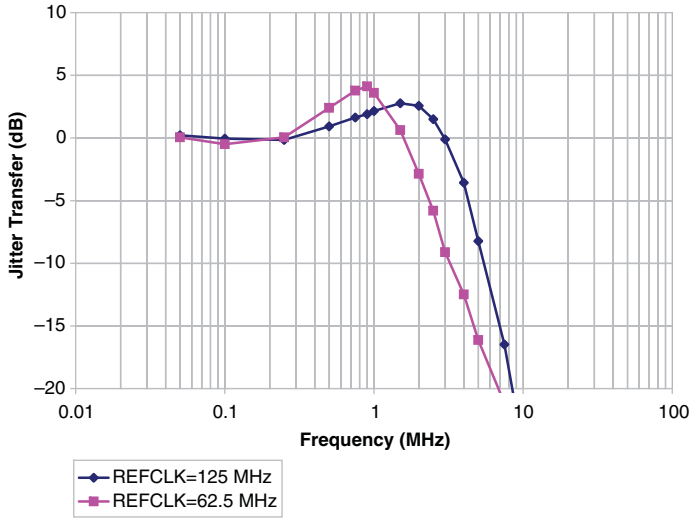
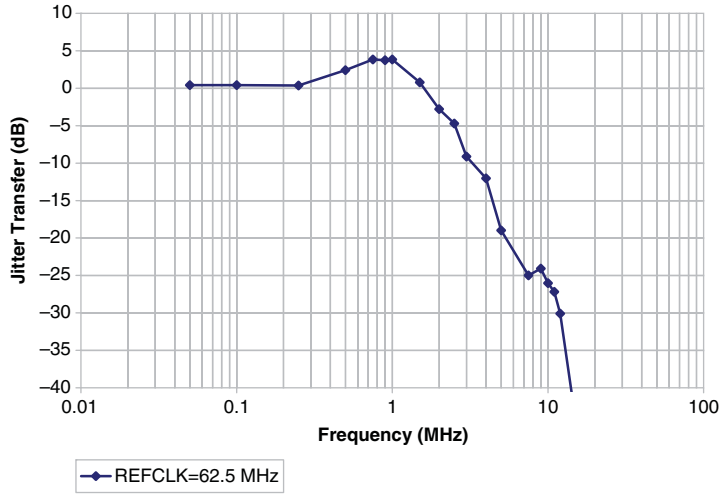



*Figure 3-17. Jitter Transfer – 622 Mbps*



# SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-19. Transmit***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDO}$ | Serial data rate | | 270 | — | 2975 | Mbps |
| $T_{JALIGNMENT}$ [2] | Serial output jitter, alignment | 270 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}$ [2] | Serial output jitter, alignment | 1485 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}$ [1, 2] | Serial output jitter, alignment | 2970Mbps | — | — | 0.30 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 270 Mbps | — | — | 0.20 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 1485 Mbps | — | — | 1.0 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 2970 Mbps | — | — | 2.0 | UI |

Notes:
1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of $f_{SCLK}$ is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

***Table 3-20. Receive***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDI}$ | Serial input data rate | | 270 | — | 2970 | Mbps |
| CID | Stream of non-transitions (=Consecutive Identical Digits) | | 7(3G)/26(SMPTE Triple rates) @ 10-12 BER | — | — | Bits |

***Table 3-21. Reference Clock***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{VCLK}$ | Video output clock frequency | | 27 | — | 74.25 | MHz |
| $DC_V$ | Duty cycle, video clock | | 45 | 50 | 55 | % |

# LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

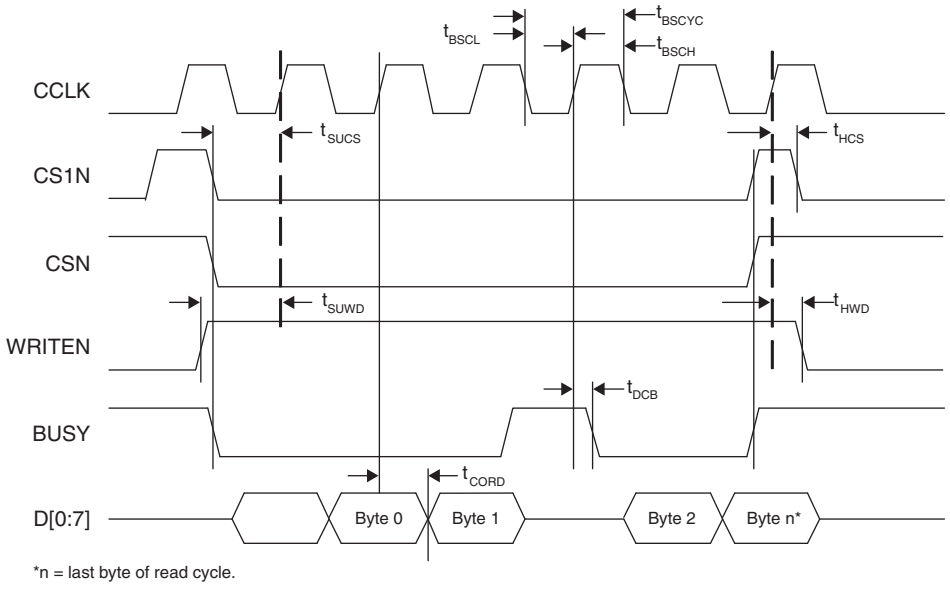
**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{SSCL}$ | CCLK Minimum Low Pulse | 5 | — | ns |
| $t_{HLCH}$ | HOLDN Low Setup Time (Relative to CCLK) | 5 | — | ns |
| $t_{CHHH}$ | HOLDN Low Hold Time (Relative to CCLK) | 5 | — | ns |
| **Master and Slave SPI (Continued)** | | | | |
| $t_{CHHL}$ | HOLDN High Hold Time (Relative to CCLK) | 5 | — | ns |
| $t_{HHCH}$ | HOLDN High Setup Time (Relative to CCLK) | 5 | — | ns |
| $t_{HLQZ}$ | HOLDN to Output High-Z | — | 9 | ns |
| $t_{HHQX}$ | HOLDN to Output Low-Z | — | 9 | ns |

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

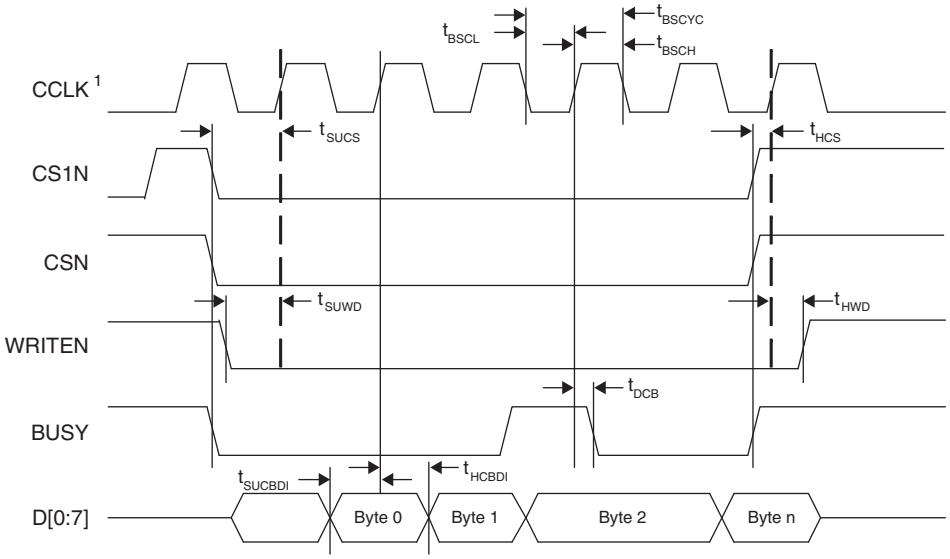
| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Master Clock Frequency | Selected value - 15% | Selected value + 15% | MHz |
| Duty Cycle | 40 | 60 | % |

***Figure 3-20. sysCONFIG Parallel Port Read Cycle***




*n = last byte of read cycle.

*Figure 3-21. sysCONFIG Parallel Port Write Cycle*




1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

*Figure 3-22. sysCONFIG Master Serial Port Timing*

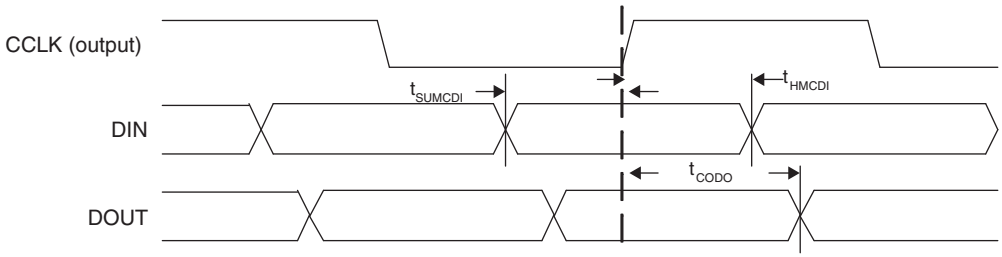
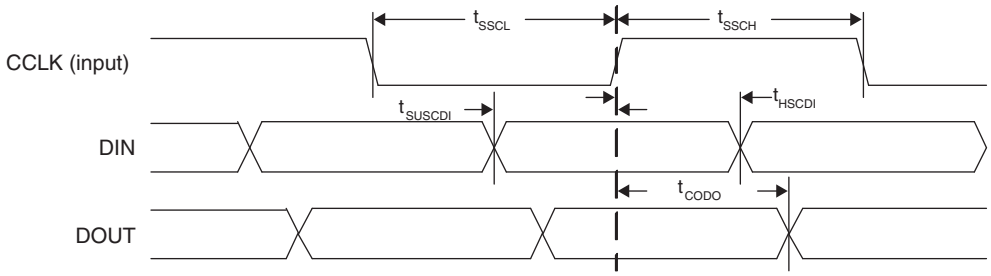


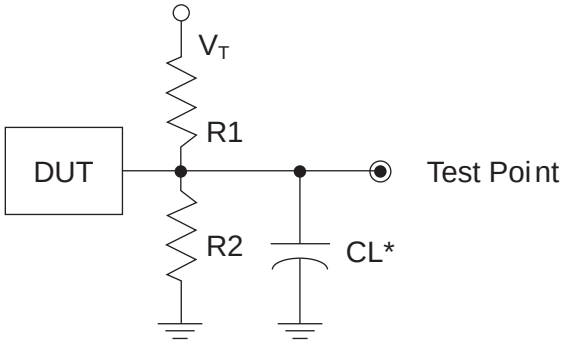

*Figure 3-23. sysCONFIG Slave Serial Port Timing*



## Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

***Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards***




*CL Includes Test Fixture and Probe Capacitance

***Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $R_2$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | ∞ | 0 pF | LVCMOS 3.3 = 1.5V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | ∞ | 1MΩ | 0 pF | $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> L) | 1 MΩ | ∞ | 0 pF | $V_{CCIO}/2$ | $V_{CCIO}$ |
| LVCMOS 2.5 I/O (H -> Z) | ∞ | 100 | 0 pF | $V_{OH}$ - 0.10 | — |
| LVCMOS 2.5 I/O (L -> Z) | 100 | ∞ | 0 pF | $V_{OL}$ + 0.10 | $V_{CCIO}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

## Pin Information Summary (Cont.)

| Pin Information Summary | | ECP3-17EA | | | ECP3-35EA | | |
|---|---|---|---|---|---|---|---|
| Pin Type | | 256 ftBGA | 328 csBGA | 484 fpBGA | 256 ftBGA | 484 fpBGA | 672 fpBGA |
| Emulated Differential I/O per Bank | Bank 0 | 13 | 10 | 18 | 13 | 21 | 24 |
| | Bank 1 | 7 | 5 | 12 | 7 | 18 | 18 |
| | Bank 2 | 2 | 2 | 4 | 1 | 8 | 8 |
| | Bank 3 | 4 | 2 | 13 | 5 | 20 | 19 |
| | Bank 6 | 5 | 1 | 13 | 6 | 22 | 20 |
| | Bank 7 | 6 | 9 | 10 | 6 | 11 | 13 |
| | Bank 8 | 12 | 12 | 12 | 12 | 12 | 12 |
| Highspeed Differential I/O per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 2 | 2 | 3 | 3 | 6 | 6 |
| | Bank 3 | 5 | 4 | 9 | 4 | 9 | 12 |
| | Bank 6 | 5 | 4 | 9 | 4 | 11 | 12 |
| | Bank 7 | 5 | 6 | 8 | 5 | 9 | 10 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Single Ended/ Total Differential I/O per Bank | Bank 0 | 26/13 | 20/10 | 36/18 | 26/13 | 42/21 | 48/24 |
| | Bank 1 | 14/7 | 10/5 | 24/12 | 14/7 | 36/18 | 36/18 |
| | Bank 2 | 8/4 | 9/4 | 14/7 | 8/4 | 28/14 | 28/14 |
| | Bank 3 | 18/9 | 12/6 | 44/22 | 18/9 | 58/29 | 63/31 |
| | Bank 6 | 20/10 | 11/5 | 44/22 | 20/10 | 67/33 | 65/32 |
| | Bank 7 | 23/11 | 30/15 | 36/18 | 23/11 | 40/20 | 46/23 |
| | Bank 8 | 24/12 | 24/12 | 24/12 | 24/12 | 24/12 | 24/12 |
| DDR Groups Bonded per Bank[2] | Bank 0 | 2 | 1 | 3 | 2 | 3 | 4 |
| | Bank 1 | 1 | 0 | 2 | 1 | 3 | 3 |
| | Bank 2 | 0 | 0 | 1 | 0 | 2 | 2 |
| | Bank 3 | 1 | 0 | 3 | 1 | 3 | 4 |
| | Bank 6 | 1 | 0 | 3 | 1 | 4 | 4 |
| | Bank 7 | 1 | 2 | 2 | 1 | 3 | 3 |
| | Configuration Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 |
| SERDES Quads | | 1 | 1 | 1 | 1 | 1 | 1 |

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672I | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-7FN672I | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-8FN672I | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-6LFN672I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-7LFN672I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-8LFN672I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-6FN1156I | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-7FN1156I | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-8FN1156I | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-6LFN1156I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-7LFN1156I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-8LFN1156I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | IND | 149 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672ITW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-7FN672ITW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-8FN672ITW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 149 |
| LFE3-150EA-6FN1156ITW[1] | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-7FN1156ITW[1] | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 149 |
| LFE3-150EA-8FN1156ITW[1] | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 149 |

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250V.

# LatticeECP3 Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist
- TN1215, LatticeECP2MS and LatticeECP2S Devices
- TN1216, LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3
- TN1222, LatticeECP3 Slave SPI Port User's Guide

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

| Date | Version | Section | Change Summary |
|---|---|---|---|
| | | | Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification |
| December 2010 | 01.7EA | Multiple | Data sheet made final. Removed “preliminary” headings. |
| | | | Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices. |
| | | | Updated for Lattice Diamond design software. |
| | | Introduction | Corrected number of user I/Os |
| | | Architecture | Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices. |
| | | | Updated description of General Purpose PLL |
| | | | Added additional information in the Flexible Quad SERDES Architecture section. |
| | | | Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal). |
| | | | Updated Figure 2-16, Per Region Secondary Clock Selection. |
| | | | Updated description for On-Chip Programmable Termination. |
| | | | Added information about number of rows of DSP slices. |
| | | | Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes. |
| | | | Updated information for sysIO buffer pairs. |
| | | | Corrected minimum number of General Purpose PLLs (was 4, now 2). |
| | | DC and Switching Characteristics | Regenerated sysCONFIG Port Timing figure. |
| | | | Added $t_W$ (clock pulse width) in External Switching Characteristics table. |
| | | | Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table. |
| | | | Added Jitter Transfer figures in SERDES External Reference Clock section. |
| | | | Corrected capacitance information in the DC Electrical Characteristics table. |
| | | | Corrected data in the Register-to-Register Performance table. |
| | | | Corrected GDDR Parameter name HOGDDR. |
| | | | Corrected RSDS25 -7 data in Family Timing Adders table. |
| | | | Added footnotes 10-12 to DDR data information in the External Switching Characteristics table. |
| | | | Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDRX2 Parameters). |
| | | | Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differential Signaling)) and 3-6 (Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)). |
| | | | Updated Supply Current table. |
| | | | Added GDDR interface information to the External Switching and Characteristics table. |
| | | | Added footnote to sysIO Recommended Operating Conditions table. |
| | | | Added footnote to LVDS25 table. |
| | | | Corrected DDR section footnotes and references. |
| | | | Corrected Hot Socketing support from “top and bottom banks” to “top and bottom I/O pins”. |
| | | Pinout Information | Updated description for VTTx. |