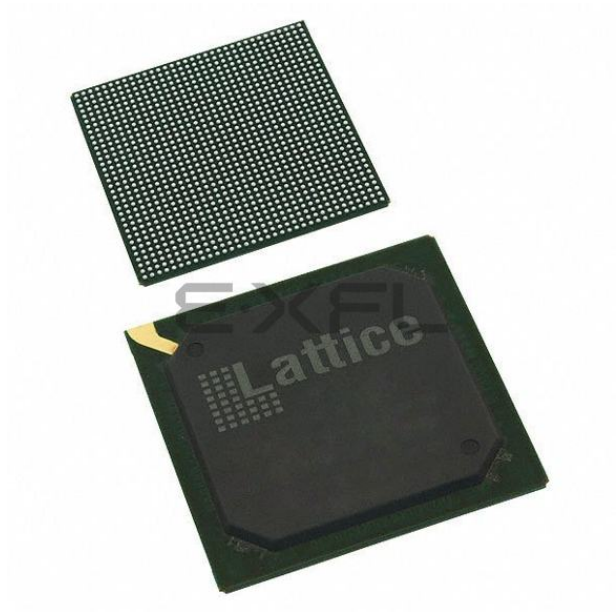
Lattice Semiconductor Corporation - LFE3-70EA-8FN1156C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-8fn1156c

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

ROM Mode
ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

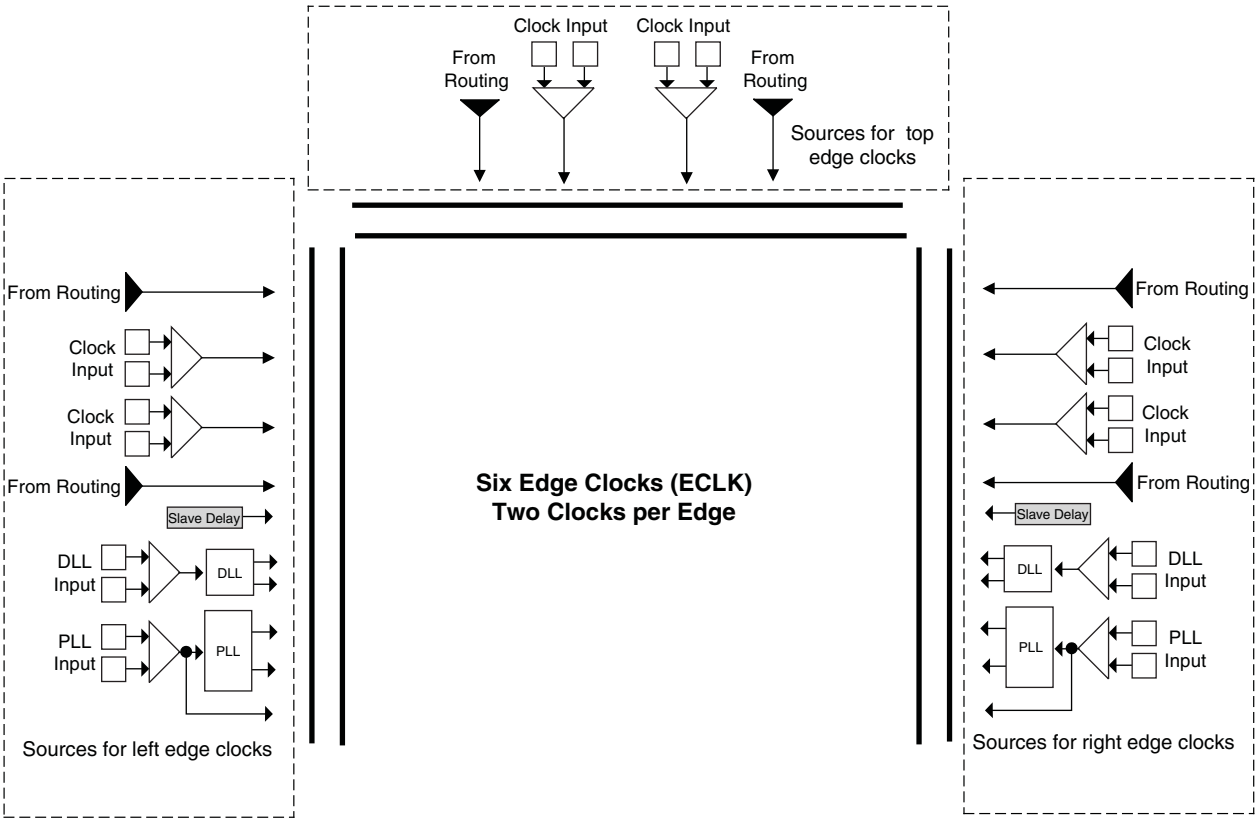
The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

Figure 2-19. Edge Clock Sources



Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

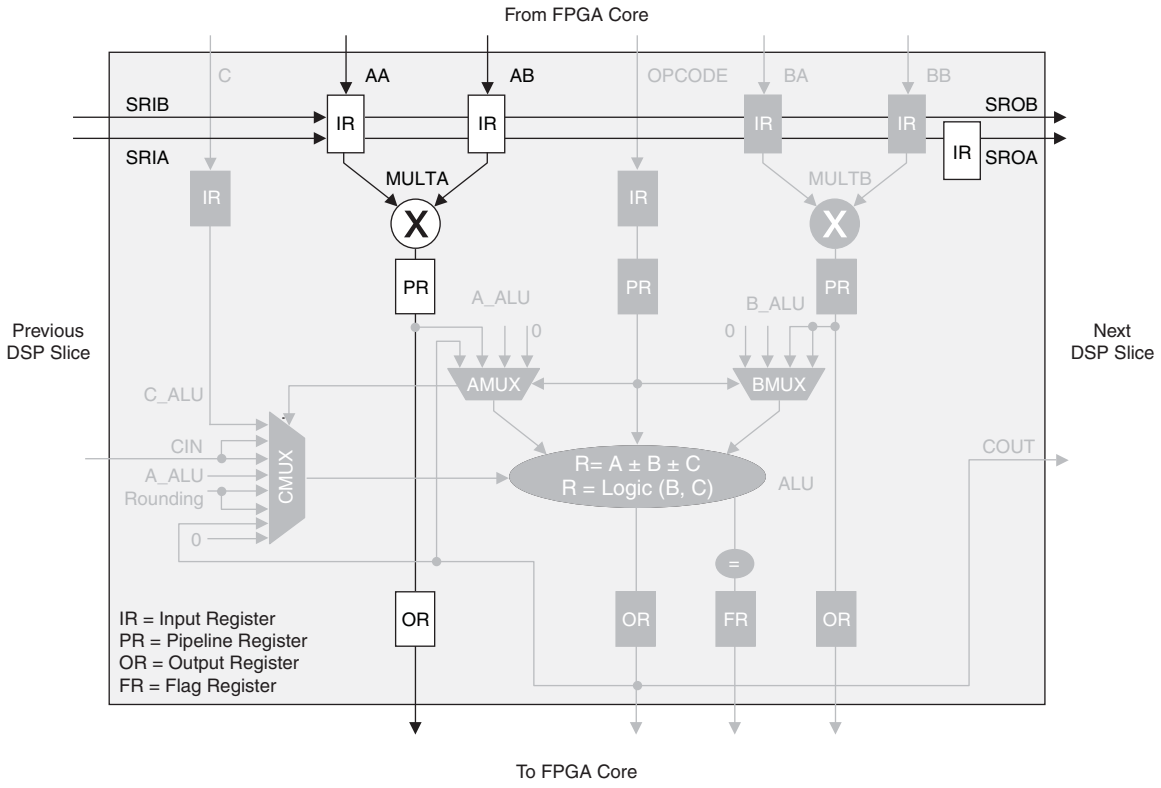
LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

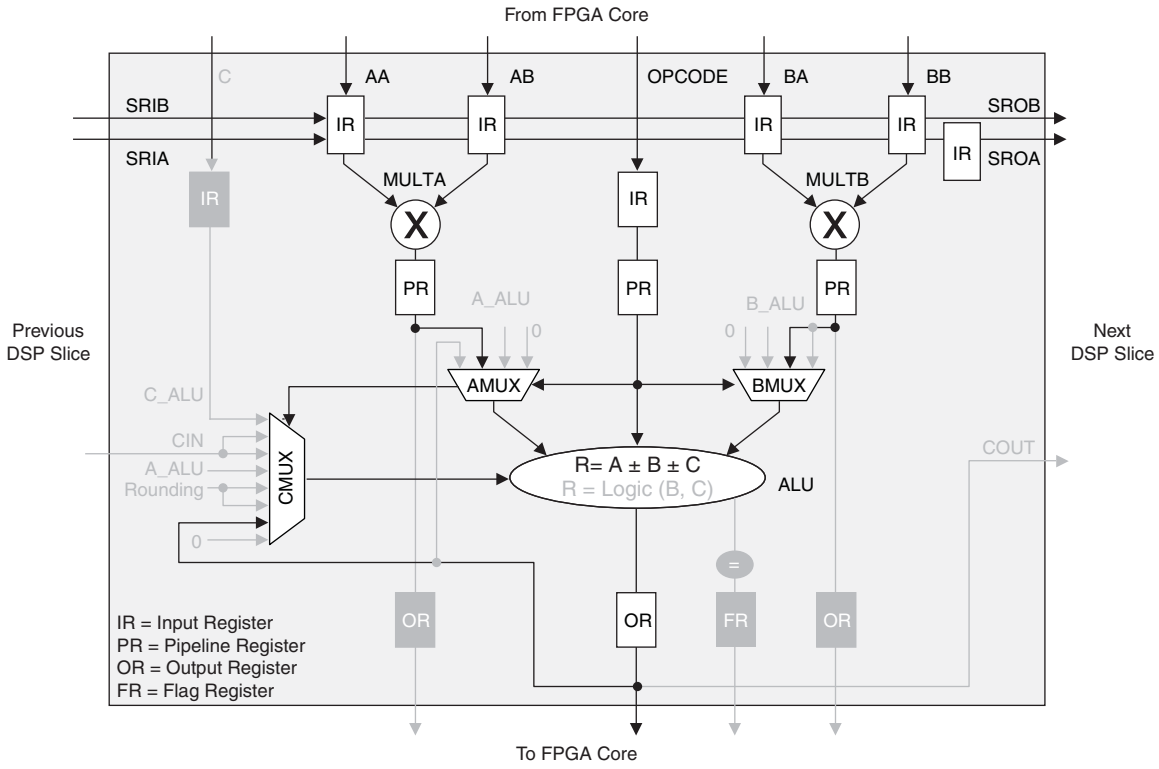
Figure 2-26. MULT sysDSP Element



MMAC DSP Element

The LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-28 shows the MMAC sysDSP element.

Figure 2-28. MMAC sysDSP Element



ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

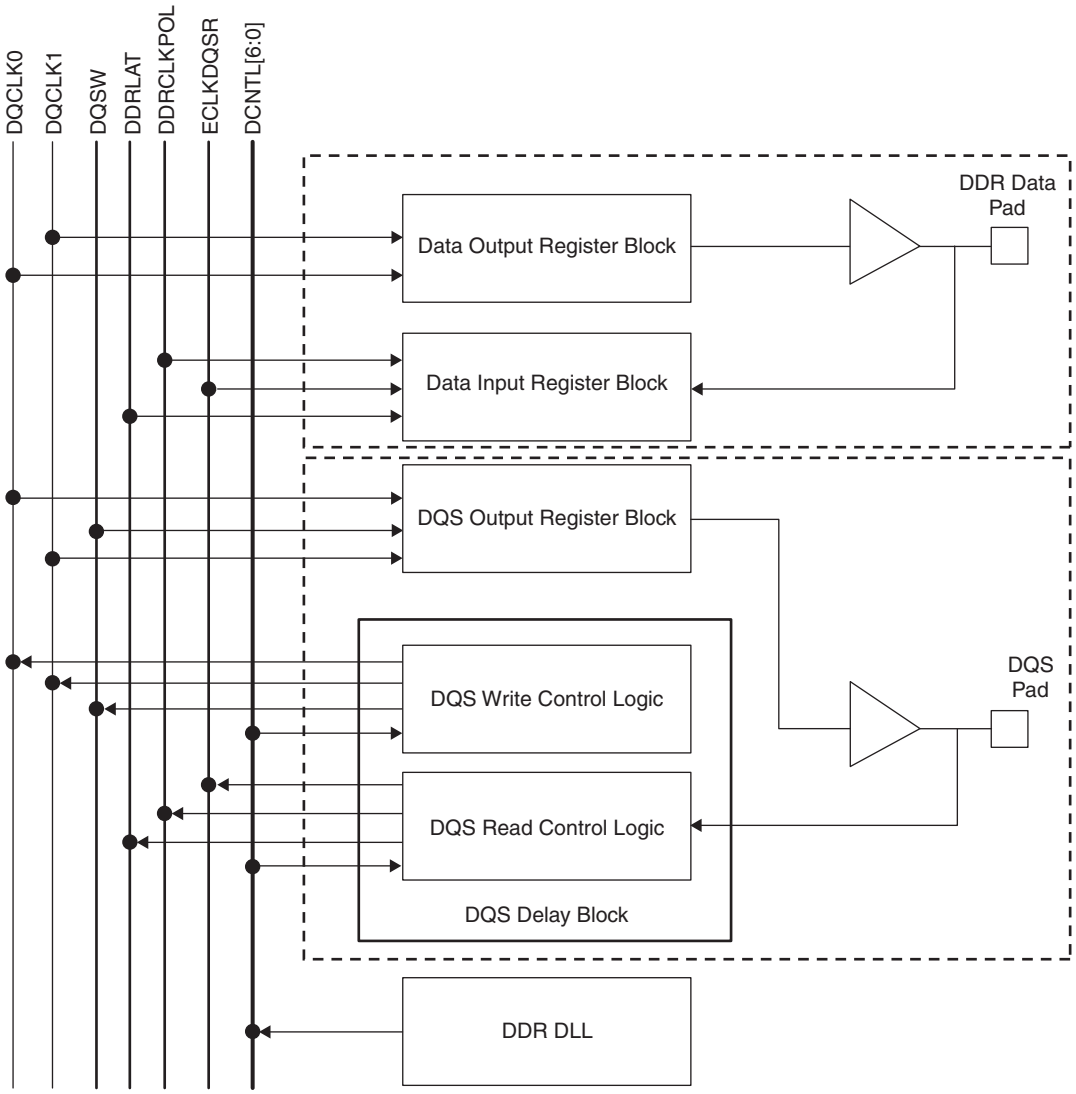
The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Figure 2-37. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

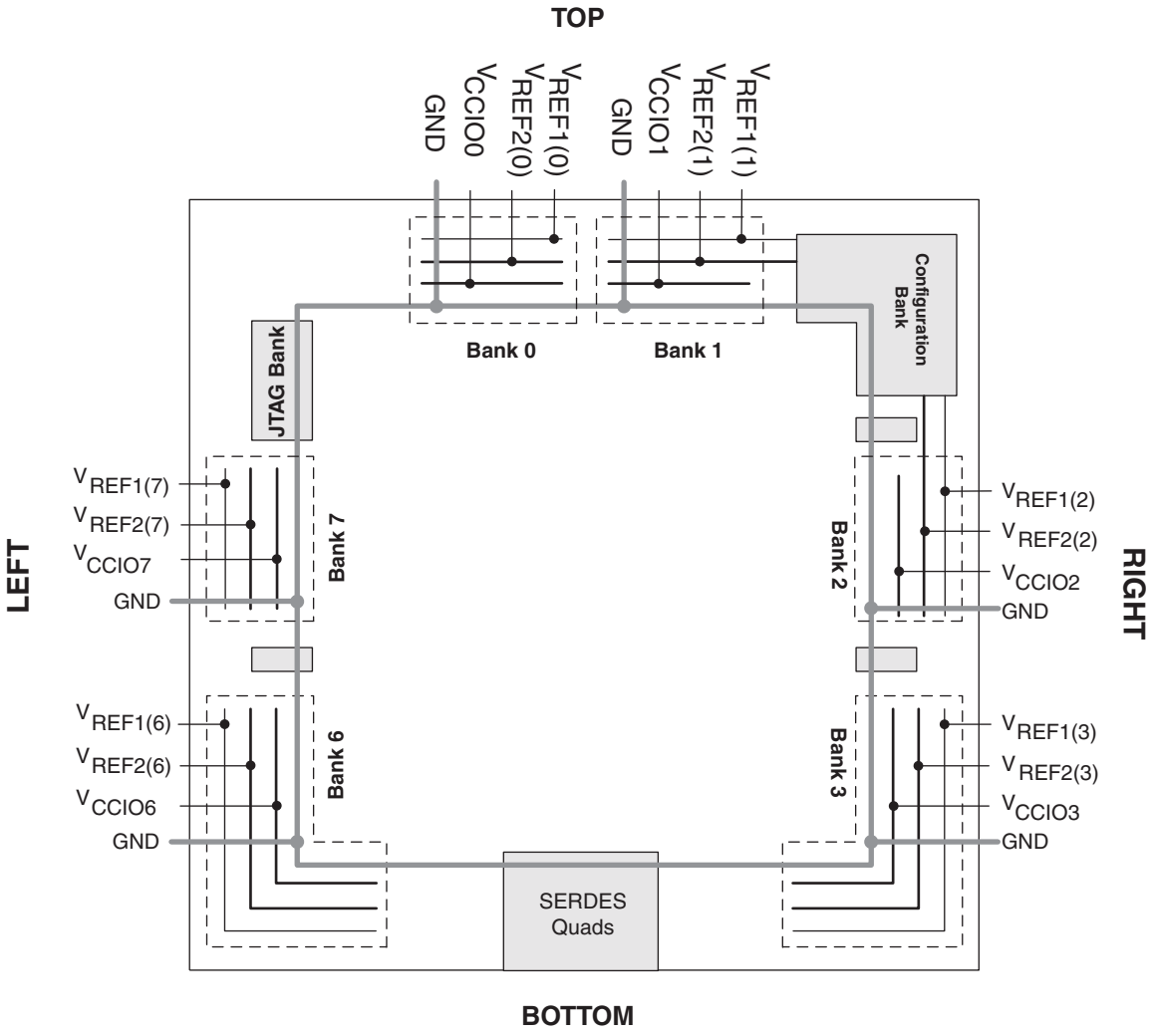
sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

   The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[4]	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)	—	—	+/–1	mA
IDK[5]	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$	—	—	+/–1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5V	—	18	—	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
3. LVCMOS and LVTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the LatticeECP3 Product Family Qualification Summary for complete qualification data, including ESD performance.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS33D	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15[3]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[2]	2.375	2.5	2.625	—	—	—
RSDSE[1, 2]	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D[3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[2, 3], II[2, 3]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. For input voltage compatibility, see TN1177, LatticeECP3 sysIO Usage Guide.
3. VREF is required when using Differential SSTL to interface to DDR memory.

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDRX2_RX.ECLK.Aligned) (No CLKDIV)									
Left and Right Sides Using DLLCLKPIN for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t_{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)[10]									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

LatticeECP3 Internal Switching Characteristics[1, 2, 5]

Over Recommended Commercial Operating Conditions

Parameter	Description	–8		–7		–6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t_{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	–0.097	—	–0.103	—	–0.109	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t_{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t_{SUDATA_PFU}	Data Setup Time	–0.137	—	–0.155	—	–0.174	—	ns
t_{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t_{SUADDR_PFU}	Address Setup Time	–0.227	—	–0.257	—	–0.286	—	ns
t_{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	–0.055	—	–0.055	—	–0.063	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay[4]	-	1.09	-	1.16	-	1.23	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	–0.085	—	–0.072	—	–0.058	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	–0.107	—	–0.094	—	–0.081	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	–0.218	—	–0.227	—	–0.237	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	–0.071	—	–0.070	—	–0.068	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	–0.107	—	–0.106	—	–0.106	—	ns

Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2^7–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}[1]	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[3, 4, 5]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[2, 3, 4, 5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[2, 3, 4, 5]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[2, 3, 4, 5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4, 5]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals[3]		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	O	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	O	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
For Top Edge of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ

Note: “n” is a row PIC number.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank[2]	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250V.