E. Lattice Semiconductor Corporation - <u>LFE3-70EA-8FN1156I Datasheet</u>



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Details

Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-8fn1156i

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LatticeECP3 Family Data Sheet Architecture

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Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sys-DSP[™] Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG[™] port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.



Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.





Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.



Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysl/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysl/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.

** Signals are available on the left and right sides only

*** Selected PIO.



Input signals are fed from the sysl/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-30 provides further information on the use of the gearbox function.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-37 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.



To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysl/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

sysl/O Buffer Banks

LatticeECP3 devices have six sysl/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysl/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysl/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2} , which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.



Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)



Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143 ¹ , 177 ¹ , 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3 ²	155.52	x1	N/A
SONET-STS-12 ²	622.08	x1	N/A
SONET-STS-48 ²	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.

2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

- 1. JTAG
- 2. Standard Serial Peripheral Interface (SPI and SPIm modes) interface to boot PROM memory
- 3. System microprocessor to drive a x8 CPU port (PCM mode)
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Generic byte wide flash with a MachXO[™] device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.



LatticeECP3 Supply Current (Standby)^{1, 2, 3, 4, 5, 6}

			Typical		
Symbol	Parameter	Device	-6L, -7L, -8L	-6, -7, -8	Units
		ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
I _{CC}	Core Power Supply Current	ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
		ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
I _{CCAUX}	Auxiliary Power Supply Current	ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
		ECP-17EA	0.0	0.0	mA
	PLL Power Supply Current (Per PLL)	ECP3-35EA	0.1	0.1	mA
I _{CCPLL}		ECP3-70EA	0.1	0.1	mA
I _{CCAUX} Au I _{CCPLL} PL I _{CCIO} Ba I _{CCJ} JT		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
		ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I _{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
		ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
I _{CCA}	Iransmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{\mbox{CCIO}}$ or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 85$ °C, power supplies at nominal voltage.

6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.



LVPECL33

The LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL33



Table 3-3. LVPECL33 DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z _{OUT}	Driver Impedance	10	Ω
R _S	Driver Series Resistor (+/-1%)	93	Ω
R _P	Driver Parallel Resistor (+/-1%)	196	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	2.05	V
V _{OL}	Output Low Voltage	1.25	V
V _{OD}	Output Differential Voltage	0.80	V
V _{CM}	Output Common Mode Voltage	1.65	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial	Operating Conditions
------------------------------------	-----------------------------

			-	-8	-	-7	-	-6	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 Ou	tput with Clock and Data (>10 Bits	Wide) Centered at Pir	n Using I	PLL (GDI	DRX2_TX	.PLL.Cer	ntered) ¹⁰		
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	_	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	_	432	_	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	—	420	—	375	MHz
Memory Interface		•							
DDR/DDR2 I/O Pin	Parameters (Input Data are Strobe	Edge Aligned, Output	ut Strobe	e Edge is	Data Ce	ntered)4			
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL f	or SCLK) I/O Pin Parameters	•							
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	_	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	_	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing	9								
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	-90	90	-90	90	-90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jit- ter During DLL Locking Period	All ECP3 Devices	_	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.

3. Generic DDR timing numbers based on LVDS I/O.

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.

5. DDR3 timing numbers based on SSTL15.

6. Uses LVDS I/O standard.

7. The current version of software does not support per bank skew numbers; this will be supported in a future release.

8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

9. Using settings generated by IPexpress.

10. These numbers are generated using best case PLL located in the center of the device.

11. Uses SSTL25 Class II Differential I/O Standard.

12. All numbers are generated with ispLEVER 8.1 software.

13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



LatticeECP3 Internal Switching Characteristics^{1, 2, 5} (Continued)

		_	8	-	7	_		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141		0.145		0.149		ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118	_	0.098	_	0.077	_	ns
DSP Block Tin	ning ³							
t _{SUI_DSP}	Input Register Setup Time	0.32	_	0.36	_	0.39	_	ns
t _{HI_DSP}	Input Register Hold Time	-0.17	_	-0.19	_	-0.21	_	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.23	_	2.30	_	2.37	_	ns
t _{HP_DSP}	Pipeline Register Hold Time	-1.02	_	-1.09	_	-1.15	_	ns
t _{SUO_DSP}	Output Register Setup Time	3.09	_	3.22	_	3.34	_	ns
t _{HO_DSP}	Output Register Hold Time	-1.67	_	-1.76	_	-1.84	_	ns
t _{COI_DSP}	Input Register Clock to Output Time	_	3.05	_	3.35	_	3.73	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	_	1.30	_	1.47	_	1.64	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t _{SUOPT_DSP}	Opcode Register Setup Time	0.31	_	0.35	_	0.39	_	ns
t _{HOPT_DSP}	Opcode Register Hold Time	-0.20	_	-0.24		-0.27	_	ns
t _{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69		1.94		2.14		ns
t _{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.58		-0.80		-0.97		ns

Over Recommended Commercial Operating Conditions

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2		500	MHz
'IN	CLKFB)		Primary clock ⁴	2		420	MHz
f	Output clock frequency (CLKOP,		Edge clock	4		500	MHz
OUT	CLKOS)		Primary clock ⁴	4		420	MHz
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125		250	MHz
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	_	166	MHz
f _{VCO}	PLL VCO frequency			500	_	1000	MHz
f _{PFD} ³	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock ⁴	2		420	MHz
AC Charac	teristics					-	
t _{PA}	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t _{DT}	CLKOS at 50% setting)	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
		$f_{OUT} \ge 420 \text{ MHz}$		—	_	200	ps
t _{OPJIT} 1	Output clock period jitter	420 MHz > $f_{OUT} \ge 100$ MHz		_	_	250	ps
		f _{OUT} < 100 MHz		—	_	0.025	UIPP
t _{SK}	Input clock to output clock skew when N/M = integer			_		500	ps
+ 2	Look time	2 to 25 MHz		—	_	200	us
LOCK		25 to 500 MHz		—		50	us
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			_		50	ns
t _{HI}	Input clock high time	90% to 90%		0.5	_	—	ns
t _{LO}	Input clock low time	10% to 10%		0.5	_	—	ns
t _{IPJIT}	Input clock period jitter			—	_	400	ps
+	Reset signal pulse width high, RSTK			10	_	_	ns
'RST	Reset signal pulse width high, RST			500	_	_	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.

4. When using internal feedback, maximum can be up to 500 MHz.



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F _{REF}	Frequency range	15	_	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	_	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ²	200	_	V _{CCA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	_	2*V _{CCA}	mV, p-p differential
V _{REF-IN}	Input levels	0	_	V _{CCA} + 0.3	V
D _{REF}	Duty cycle ³	40	_	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-20%	100/2K	+20%	Ohms
C _{REF-IN-CAP}	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms





Figure 3-14. Jitter Transfer – 3.125 Gbps



Figure 3-15. Jitter Transfer – 2.5 Gbps





Figure 3-30. SPI Configuration Waveforms



Figure 3-31. Slave SPI HOLDN Waveforms





Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



LatticeECP3 Family Data Sheet Supplemental Information

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Data Sheet DS1021

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at <u>www.latticesemi.com</u>.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist
- TN1215, LatticeECP2MS and LatticeECP2S Devices
- TN1216, LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3
- TN1222, LatticeECP3 Slave SPI Port User's Guide

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

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