Lattice Semiconductor Corporation - LFE3-70EA-8FN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-8fn484c

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

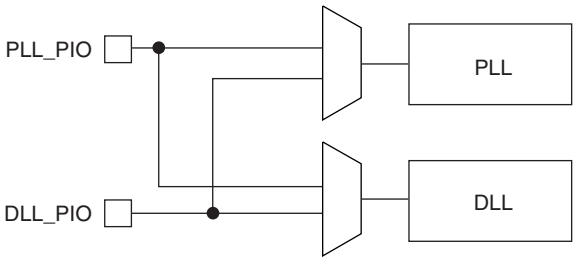
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices

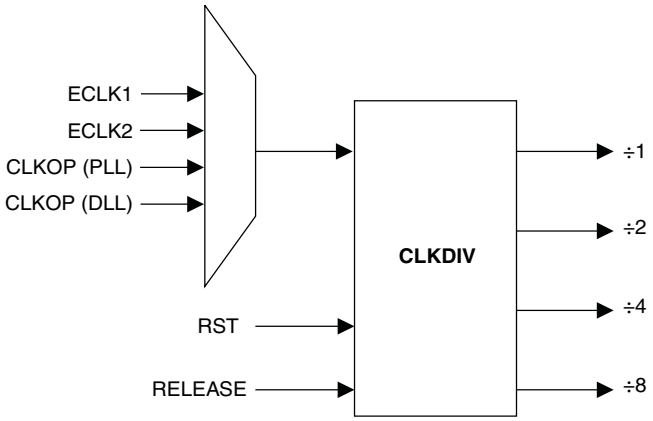


Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.

Figure 2-8. Clock Divider Connections



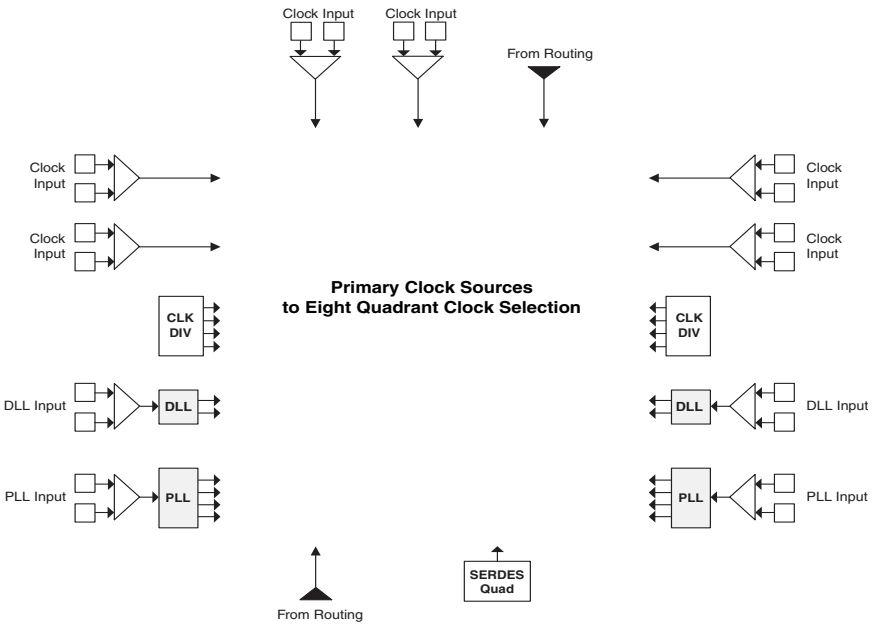
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17

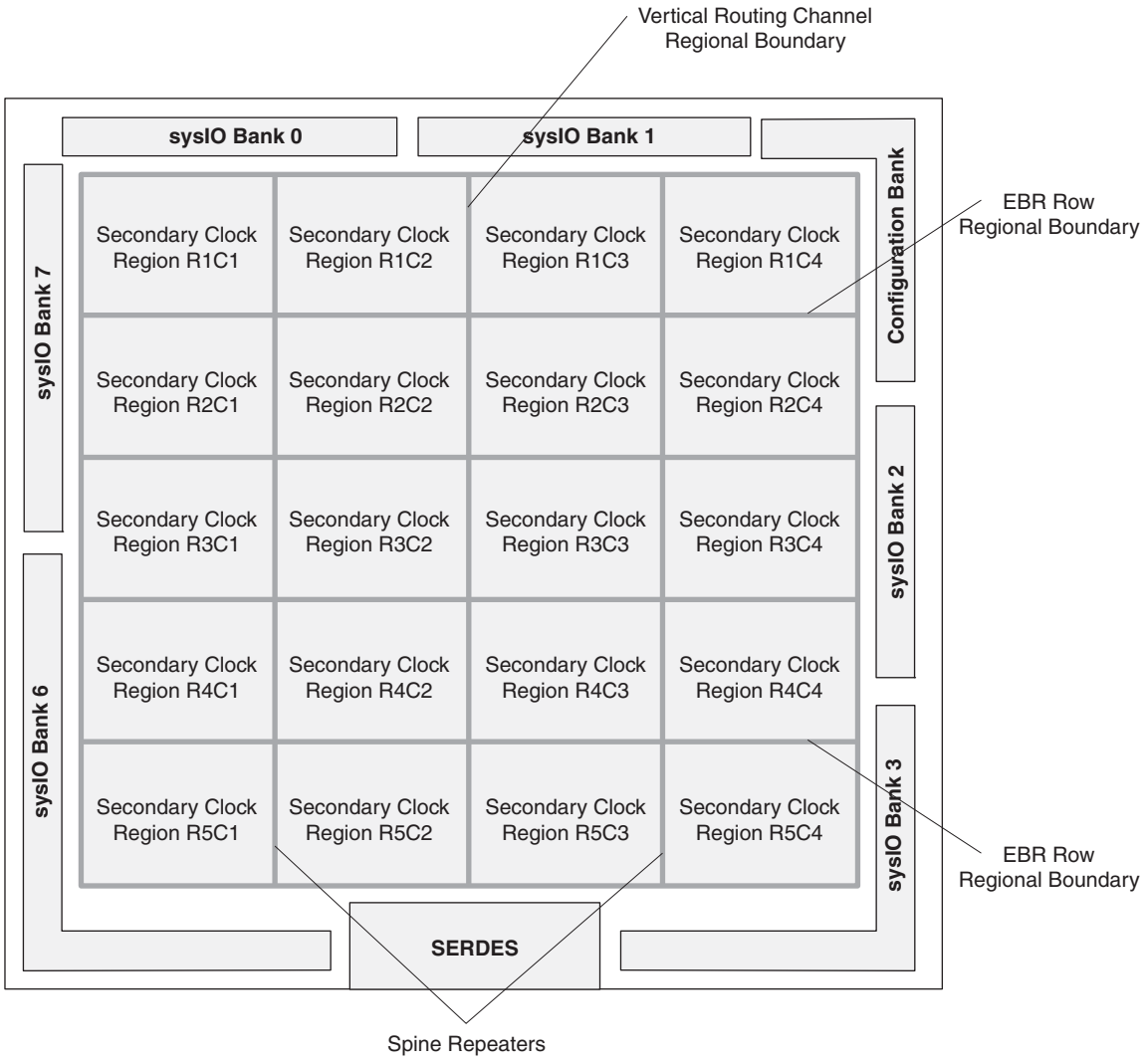


Note: Clock inputs can be configured in differential or single-ended mode.

Table 2-6. Secondary Clock Regions

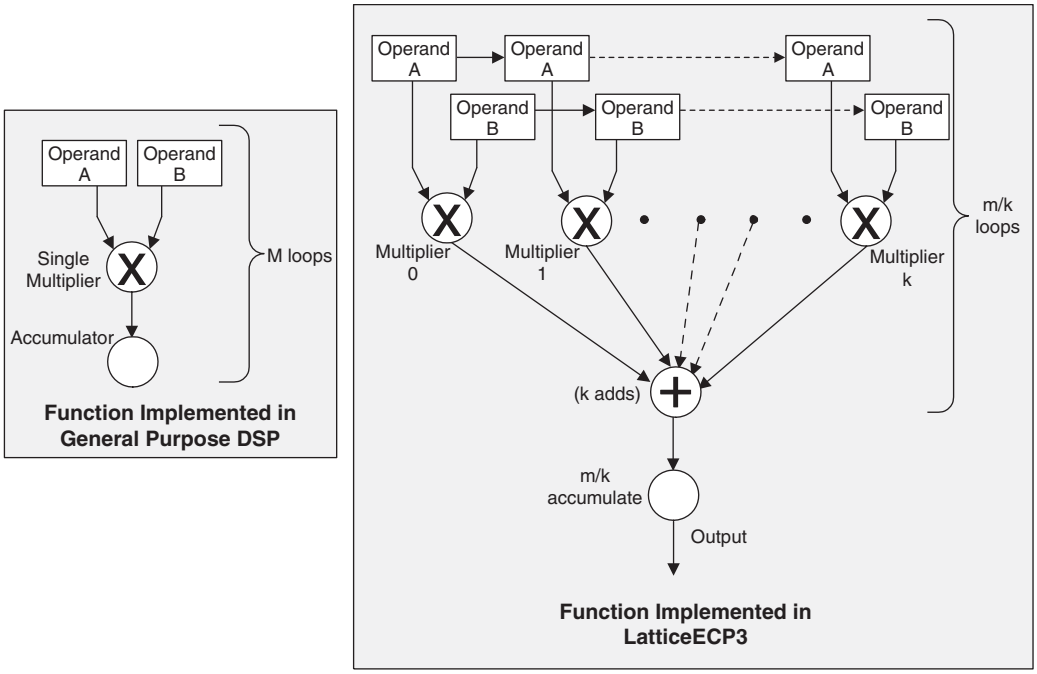
Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches



LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

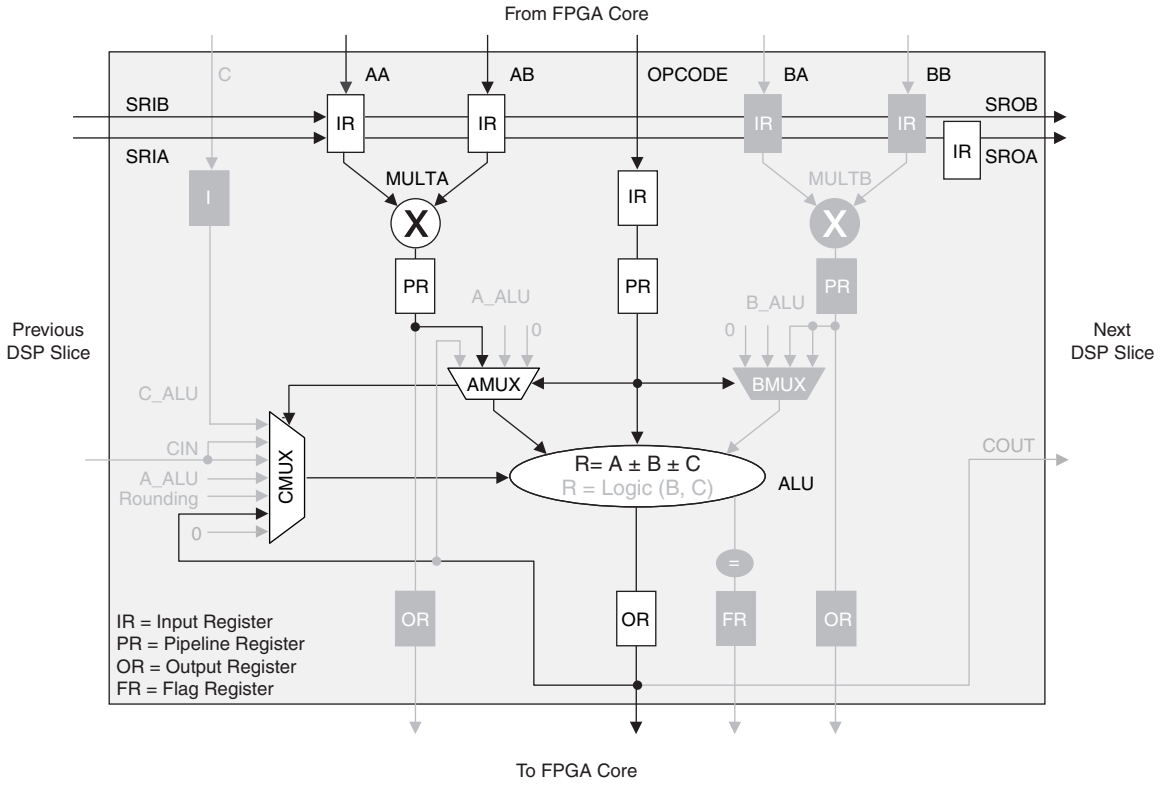
The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

Figure 2-27. MAC DSP Element



To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10 kOhm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/– 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

LatticeECP3 Maximum I/O Buffer Speed (Continued)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
PCI33	PCI, V_{CCIO} = 3.3 V	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram

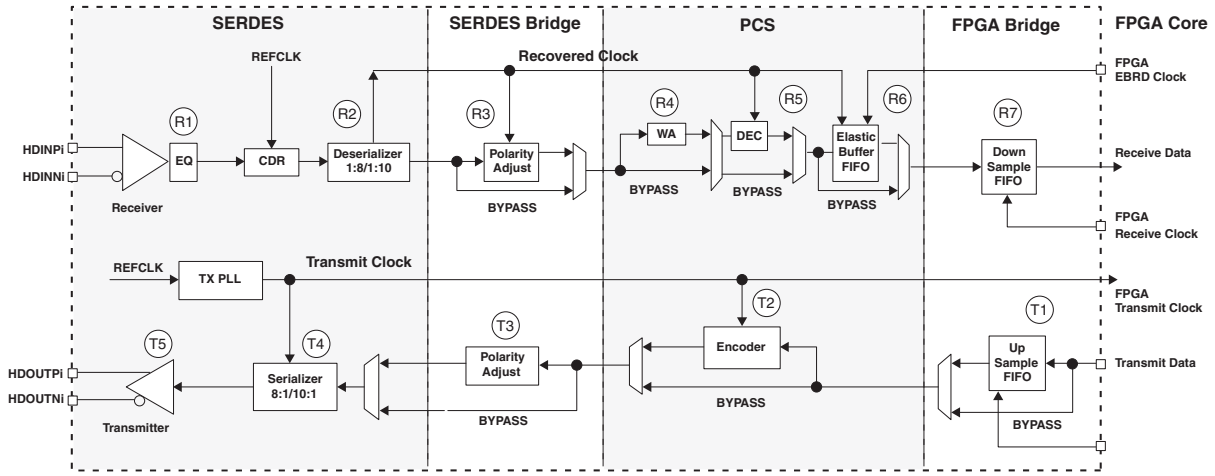


Figure 3-14. Jitter Transfer – 3.125 Gbps

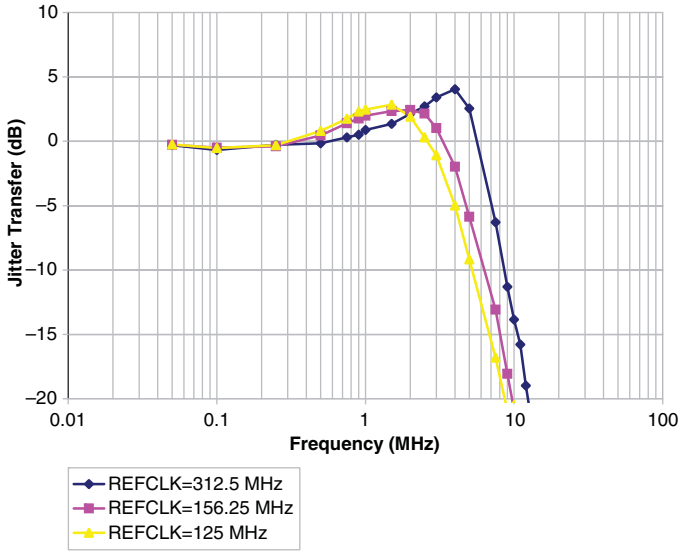


Figure 3-15. Jitter Transfer – 2.5 Gbps

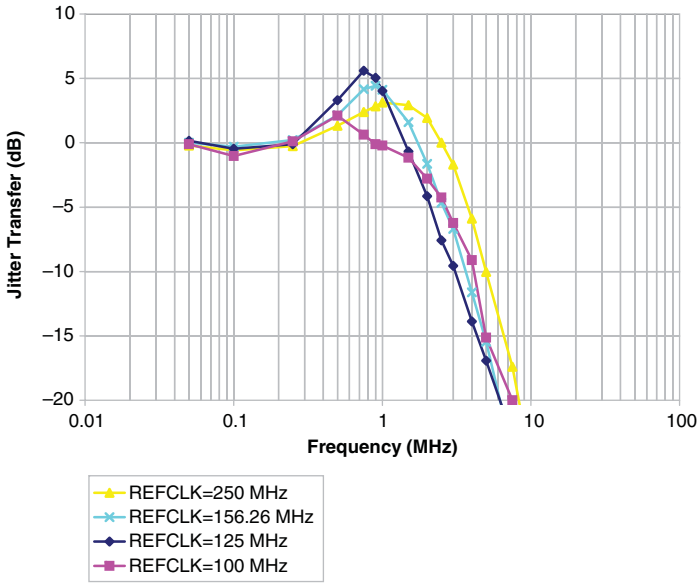
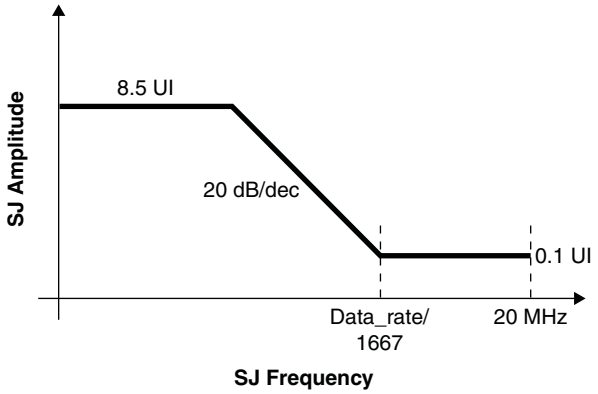
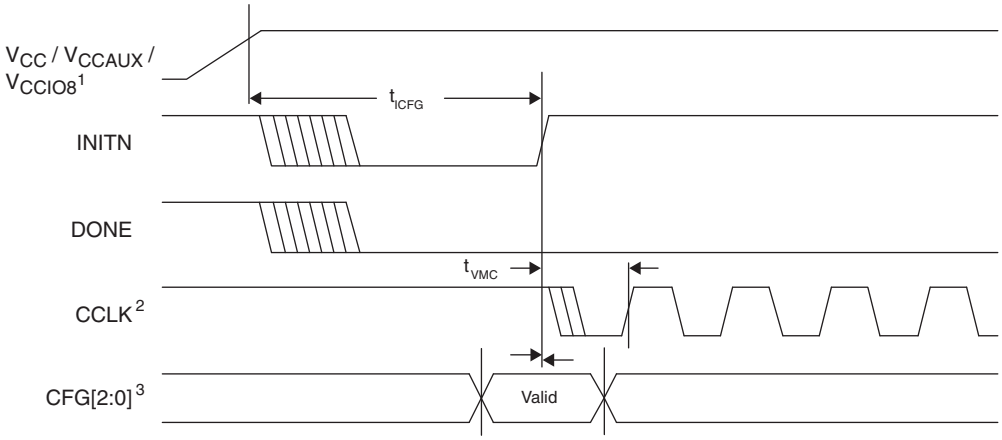


Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

Figure 3-24. Power-On-Reset (POR) Timing



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

Figure 3-25. sysCONFIG Port Timing

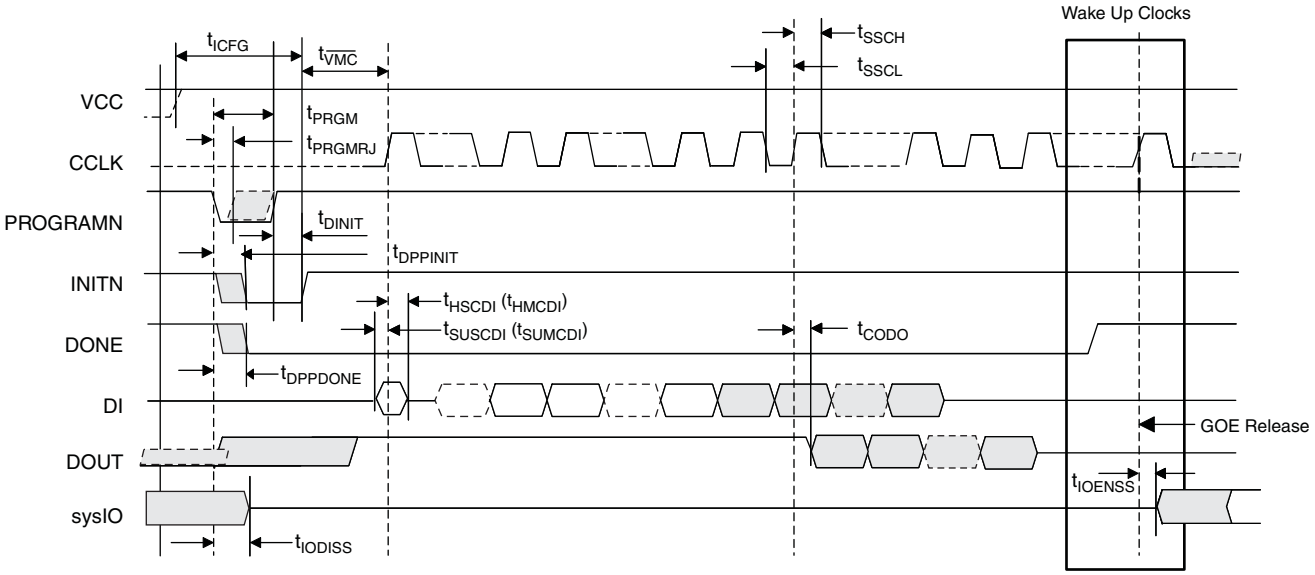


Figure 3-28. Master SPI Configuration Waveforms

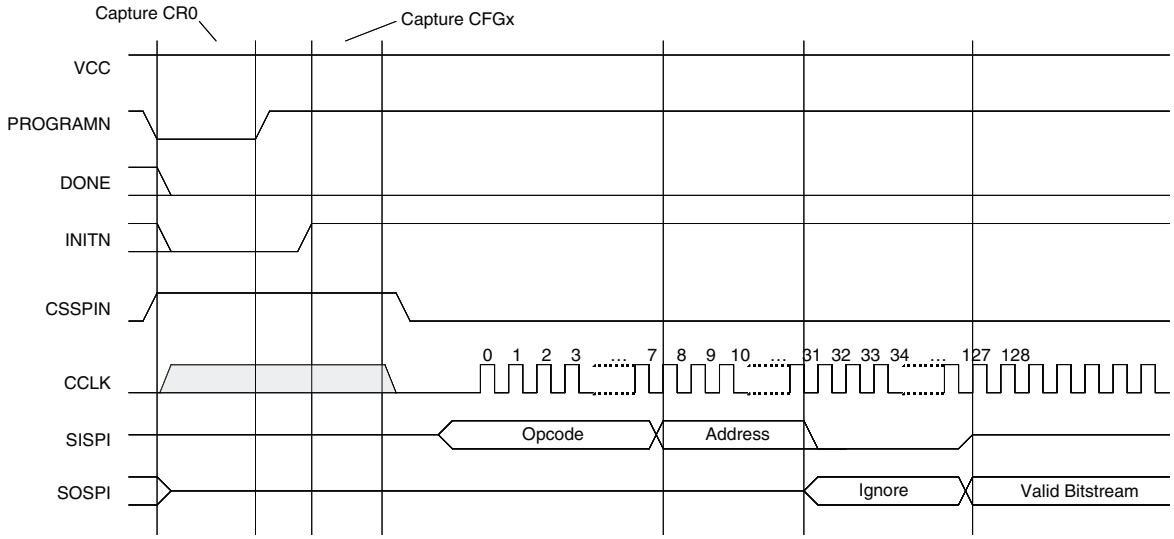
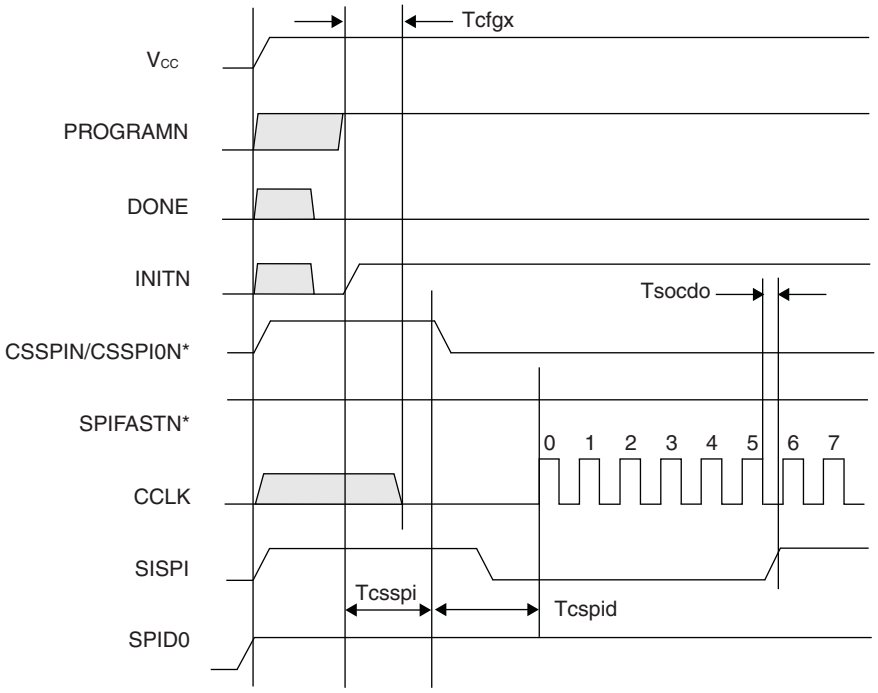


Figure 3-29. Master SPI POR Waveforms

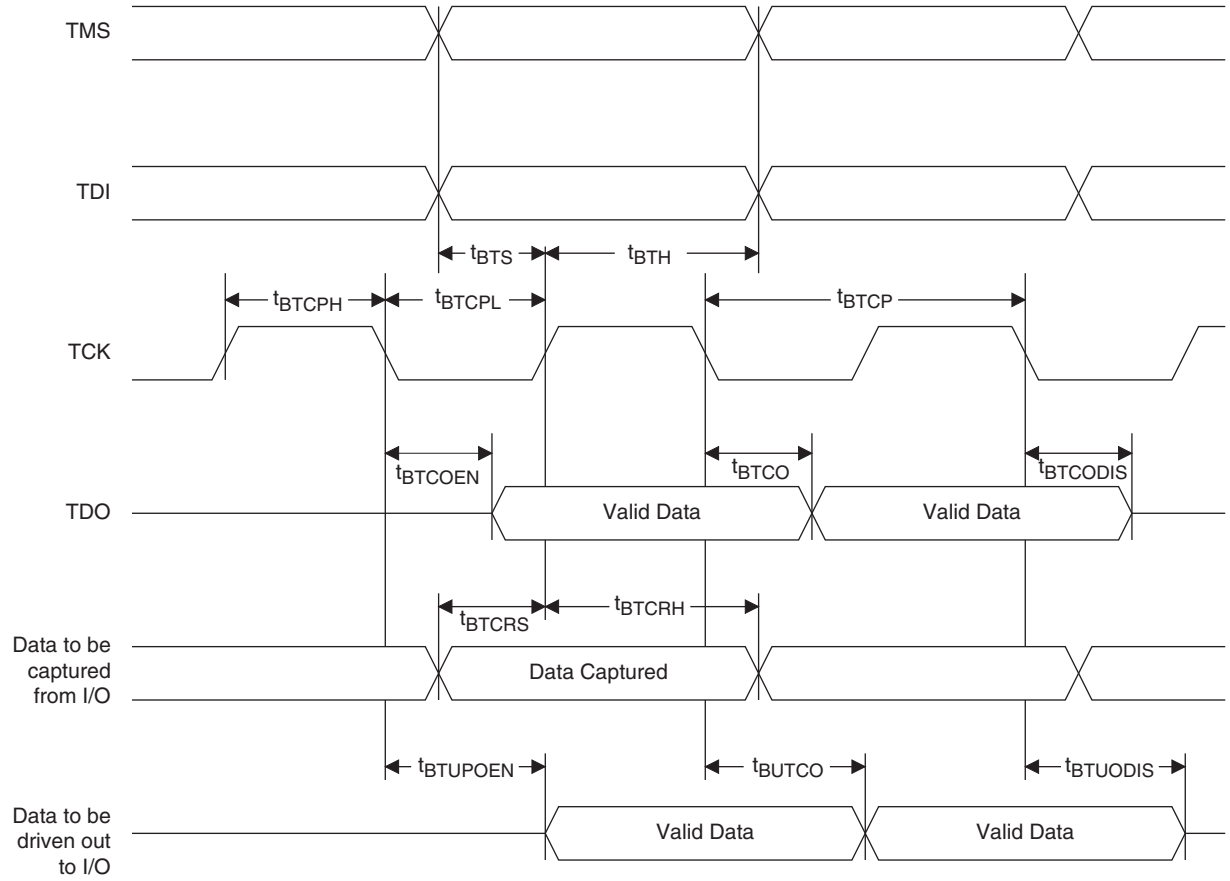


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-32. JTAG Port Timing Waveforms



LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Commercial

Part Number	Voltage	Grade	Power	Package[1]	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	–6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	–7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	–8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	–6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	–7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	–8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	–6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	–7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	–8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	–6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	–7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	–8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	–6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	–7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	–8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	–6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	–7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	–8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	–6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	–7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	–8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	–6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	–7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	–8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW[1]	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW[1]	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW[1]	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW[1]	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW[1]	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW[1]	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250 V.

LatticeECP3 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist
- TN1215, LatticeECP2MS and LatticeECP2S Devices
- TN1216, LatticeECP2/M and LatticeECP3 Dual Boot Feature Advanced Security Encryption Key Programming Guide for LatticeECP3
- TN1222, LatticeECP3 Slave SPI Port User's Guide

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break-down table.
		Pinout Information	"Logic Signal Connections" section heading renamed "Package Pinout Information". Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V_{CCA} signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for t_{RST}.
		Ordering Information	Updated topside marks with new logos in the Ordering Information section.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL TIming table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, t_{JIT}.
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t_{SUWREN_EBR} and t_{HWREN_EBR}.
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications