E. Lattice Semiconductor Corporation - LFE3-70EA-9FN1156C Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Not For New Designs
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-9fn1156c

Email: info@E-XFL.COM

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Figure 2-10. Primary Clock Sources for LatticeECP3-35



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150



Note: Clock inputs can be configured in differential or single-ended mode.



Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-12. Per Quadrant Primary Clock Selection



Dynamic Clock Control (DCC)

The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.



Figure 2-13. DCS Waveforms



Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.



Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dualboot image support.

1. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. Dual-Boot Image Support

Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10 kOhm \pm 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/- 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.



sysI/O Differential Electrical Characteristics LVDS25

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} ¹ , V _{INM} ¹	Input Voltage		0	_	2.4	V
V _{CM} ¹	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	_	mV
I _{IN}	Input Current	Power On or Power Off		_	+/-10	μΑ
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm		1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9 V	1.03	_	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L		_	_	50	mV
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

1, On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.



RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

Table 3-4. RSDS25E DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/–1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.35	V
V _{OL}	Output Low Voltage	1.15	V
V _{OD}	Output Differential Voltage	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeECP3 External Switching Characteristics ^{1, 2, 3, 13}

			-	·8	-7		-6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Clocks				1			1		1
Primary Clock ⁶									
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-150EA	—	500	—	420	—	375	MHz
t _{w_PRI}	Clock Pulse Width for Primary Clock	ECP3-150EA	0.8	—	0.9		1.0		ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-150EA	_	300	_	330	—	360	ps
tskew_prib	Primary Clock Skew Within a Bank	ECP3-150EA	—	250	_	280	—	300	ps
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-70EA/95EA	—	500	_	420	—	375	MHz
t _{W_PRI}	Pulse Width for Primary Clock	ECP3-70EA/95EA	0.8	—	0.9		1.0		ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-70EA/95EA	—	360	_	370	—	380	ps
t _{SKEW_PRIB}	Primary Clock Skew Within a Bank	ECP3-70EA/95EA	—	310		320	—	330	ps
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-35EA	—	500	_	420	—	375	MHz
tw_pri	Pulse Width for Primary Clock	ECP3-35EA	0.8	_	0.9		1.0	_	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-35EA	_	300	_	330	—	360	ps
tskew_prib	Primary Clock Skew Within a Bank	ECP3-35EA	—	250	_	280	—	300	ps
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-17EA	—	500	_	420		375	MHz
t _{W_PRI}	Pulse Width for Primary Clock	ECP3-17EA	0.8	—	0.9	_	1.0		ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-17EA	_	310		340	_	370	ps
tskew_prib	Primary Clock Skew Within a Bank	ECP3-17EA	—	220	_	230	—	240	ps
Edge Clock ⁶									
fMAX_EDGE	Frequency for Edge Clock	ECP3-150EA	—	500	—	420	_	375	MHz
tw_edge	Clock Pulse Width for Edge Clock	ECP3-150EA	0.9	—	1.0	—	1.2	_	ns
tskew_edge_dqs	Edge Clock Skew Within an Edge of the Device	ECP3-150EA	_	200	_	210	—	220	ps
fMAX_EDGE	Frequency for Edge Clock	ECP3-70EA/95EA	—	500	_	420	—	375	MHz
tw_edge	Clock Pulse Width for Edge Clock	ECP3-70EA/95EA	0.9	—	1.0	—	1.2	-	ns
tskew_edge_dqs	Edge Clock Skew Within an Edge of the Device	ECP3-70EA/95EA	_	200	_	210	—	220	ps
fMAX_EDGE	Frequency for Edge Clock	ECP3-35EA	—	500	_	420	—	375	MHz
tw_edge	Clock Pulse Width for Edge Clock	ECP3-35EA	0.9	—	1.0	—	1.2	_	ns
tskew_edge_dqs	Edge Clock Skew Within an Edge of the Device	ECP3-35EA	_	200	_	210	—	220	ps
fMAX_EDGE	Frequency for Edge Clock	ECP3-17EA	—	500	_	420	—	375	MHz
tw_edge	Clock Pulse Width for Edge Clock	ECP3-17EA	0.9	—	1.0	_	1.2	_	ns
t _{SKEW_EDGE_DQS}	Edge Clock Skew Within an Edge of the Device	ECP3-17EA	—	200	_	210	—	220	ps
Generic SDR									
General I/O Pin Par	ameters Using Dedicated Clock In	put Primary Clock W	Vithout Pl	LL ²					
t _{co}	Clock to Output - PIO Output Register	ECP3-150EA	_	3.9	_	4.3	—	4.7	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.0	_	0.0		0.0		ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-150EA	1.5	—	1.7	_	2.0	_	ns
	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.3	—	1.5	_	1.7	_	ns

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-	-8	-7		-6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered) ¹⁰									
Left and Right Side	Left and Right Sides								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	_	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	_	432	_	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	—	420	—	375	MHz
Memory Interface		•							
DDR/DDR2 I/O Pin	Parameters (Input Data are Strobe	Edge Aligned, Output	ut Strobe	e Edge is	Data Ce	ntered)4			
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL f	or SCLK) I/O Pin Parameters	•							
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	_	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	_	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing	9								
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	-90	90	-90	90	-90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jit- ter During DLL Locking Period	All ECP3 Devices	_	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.

3. Generic DDR timing numbers based on LVDS I/O.

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.

5. DDR3 timing numbers based on SSTL15.

6. Uses LVDS I/O standard.

7. The current version of software does not support per bank skew numbers; this will be supported in a future release.

8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

9. Using settings generated by IPexpress.

10. These numbers are generated using best case PLL located in the center of the device.

11. Uses SSTL25 Class II Differential I/O Standard.

12. All numbers are generated with ispLEVER 8.1 software.

13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5 V	-0.07	-0.04	-0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	-0.22	-0.19	-0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.3V	-0.06	-0.06	-0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.3V	-0.01	-0.02	-0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.3V	-0.07	-0.07	-0.08	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.3V	-0.12	-0.13	-0.14	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	-0.06	-0.06	-0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	-0.01	-0.02	-0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	-0.07	-0.07	-0.08	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	-0.05	-0.06	-0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns

Over Recommended Commercial Operating Conditions



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Over Recommended Commer	cial Operating Conditions
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Buffer Type	Description	-8	-7	-6	Units
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	-0.12	-0.13	-0.14	ns

1. Timing adders are characterized but not tested on every device.

2. LVCMOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.

5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

6. This data does not apply to the LatticeECP3-17EA device.

7. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



LatticeECP3 Maximum I/O Buffer Speed (Continued)^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Buffer Description		Max.	Units	
PCI33	PCI, V _{CCIO} = 3.3 V	66	MHz	

1. These maximum speeds are characterized but not tested on every device.

2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.

3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.

4. All speeds are measured at fast slew.

5. Actual system operation may vary depending on user logic implementation.

6. Maximum data rate equals 2 times the clock rate when utilizing DDR.



DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Тур.	Max.	Units
f _{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{CLKOP} 1	Output clock frequency, CLKOP		133	—	500	MHz
f _{CLKOS²}	Output clock frequency, CLKOS		33.3	—	500	MHz
t _{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
	Output clock duty cycle (at 50% levels, 50% duty	Edge Clock	40		60	%
t _{DUTY}	off, time reference delay mode)	Primary Clock	30		70	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	45		55	%
t _{DUTYTRD}	duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
t _{DUTYCIR}	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250 MHz	40		60	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
t _{SKEW} ³	Output clock to clock skew between two outputs with the same phase setting		_	—	100	ps
t _{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		_	—	+/-400	ps
t _{PWH}	Input clock minimum pulse width high (at 80% level)		550	_		ps
t _{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	_	ps
t _{INSTB}	Input clock period jitter			—	500	ps
t _{LOCK}	DLL lock time		8	—	8200	cycles
t _{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t _{DEL}	Delay step size		27	45	70	ps
t _{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t _{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a "path-matching" design guideline and is not a measurable specification.



Figure 3-16. Jitter Transfer – 1.25 Gbps



Figure 3-17. Jitter Transfer – 622 Mbps





PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Symbol	Description	Test Conditions	Min	Тур	Max	Units
Transmit ¹		•				
UI	Unit interval		399.88	400	400.12	ps
V _{TX-DIFF_P-P}	Differential peak-to-peak output voltage		0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis differential output voltage ratio		-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC peak common-mode output voltage		_	_	20	mV
V _{TX-RCV-DETECT}	Amount of voltage change allowed dur- ing receiver detection		_	_	600	mV
V _{TX-DC-CM}	Tx DC common mode voltage		0	_	$V_{CCOB} + 5\%$	V
ITX-SHORT	Output short circuit current	V _{TX-D+} =0.0 V V _{TX-D-} =0.0 V	_	_	90	mA
Z _{TX-DIFF-DC}	Differential output impedance		80	100	120	Ohms
RL _{TX-DIFF}	Differential return loss		10		—	dB
RL _{TX-CM}	Common mode return loss		6.0		—	dB
T _{TX-RISE}	Tx output rise time	20 to 80%	0.125	_	—	UI
T _{TX-FALL}	Tx output fall time	20 to 80%	0.125		—	UI
L _{TX-SKEW}	Lane-to-lane static output skew for all lanes in port/link		_	_	1.3	ns
T _{TX-EYE}	Transmitter eye width		0.75		—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum time between jitter median and maximum deviation from median		_	_	0.125	UI
Receive ^{1, 2}						
UI	Unit Interval		399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential peak-to-peak input voltage		0.34 ³	—	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle detect threshold voltage		65	_	340 ³	mV
V _{RX-CM-AC_P}	Receiver common mode voltage for AC coupling			_	150	mV
Z _{RX-DIFF-DC}	DC differential input impedance		80	100	120	Ohms
Z _{RX-DC}	DC input impedance		40	50	60	Ohms
Z _{RX-HIGH-IMP-DC}	Power-down DC input impedance		200K	_	—	Ohms
RL _{RX-DIFF}	Differential return loss		10	—	_	dB
RL _{RX-CM}	Common mode return loss		6.0	_	—	dB
T _{RX-IDLE-DET-DIFF-ENTERTIME}	Maximum time required for receiver to recognize and signal an unexpected idle on link		_		_	ms

1. Values are measured at 2.5 Gbps.

2. Measured with external AC-coupling on the receiver.

3.Not in compliance with PCI Express 1.1 standard.



HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-22. Transmit and Receive^{1, 2}

		Spec. Co		
Symbol	Description	Min. Spec.	Max. Spec.	Units
Transmit		•		
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive		•		
R _T	Termination Resistance	40	60	Ohms
V _{ICM}	Input AC Common Mode Voltage (50-Ohm Set- ting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.

2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.



Pin Information Summary

Pin Information	ECP3-17EA			ECP3-35EA			ECP3-70EA			
Pin Tyr	256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA	
	Bank 0	26	20	36	26	42	48	42	60	86
	Bank 1	14	10	24	14	36	36	36	48	78
	Bank 2	6	7	12	6	24	24	24	34	36
General Purpose	Bank 3	18	12	44	16	54	59	54	59	86
	Bank 6	20	11	44	18	63	61	63	67	86
	Bank 7	19	26	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24	24
	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4	4	8	8
General Purpose Inputs	Bank 3	0	0	0	2	4	4	4	12	12
per bank	Bank 6	0	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0	0
	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
General Purpose Out-	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310	295	380	490
VCC		6	16	16	6	16	32	16	32	32
VCCAUX		4	5	8	4	8	12	8	12	16
VTT		4	7	4	4	4	4	4	4	8
VCCA		4	6	4	4	4	8	4	8	16
VCCPLL		2	2	4	2	4	4	4	4	4
	Bank 0	2	3	2	2	2	4	2	4	4
	Bank 1	2	3	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	2	4	2	4	4
VCCIO	Bank 3	2	3	2	2	2	4	2	4	4
	Bank 6	2	3	2	2	2	4	2	4	4
	Bank 7	2	3	2	2	2	4	2	4	4
	Bank 8	1	2	2	1	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1	1
ТАР		4	4	4	4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139	98	139	233
NC		0	0	73	0	0	96	0	0	238
Reserved ¹		0	0	2	0	2	2	2	2	2
SERDES		26	18	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672	484	672	1156



LatticeECP3 Family Data Sheet Ordering Information

April 2014

Data Sheet DS1021

LatticeECP3 Part Number Description



1. Green = Halogen free and lead free.

Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:



Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

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Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW1	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW1	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250 V.



LatticeECP3 Family Data Sheet Revision History

March 2015

Data Sheet DS1021

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information All	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3.
			Minor style/formatting changes.
April 2014	02.7EA	DC and Switching	Updated LatticeECP3 Supply Current (Standby) table power numbers.
		Characteristics	Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysl/O Single-Ended DC Electrical Character- istics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed ${\rm I}_{Pw}$ to ${\rm I}_{PD}$ in footnote 3.
			Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching	Updated the Wake-Up Timing Diagram
		Characteristics	Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms
			Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysl/O Buffer Banks text section – Updated description of "Top (Bank 0 and Bank 1) and Bottom syslO Buffer Pairs (Single-Ended Outputs Only)" for hot socketing information.
			sysl/O Buffer Banks text section – Updated description of "Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)" for PCI clamp information.
			On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysl/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard.
			sysl/O Single-Ended DC Electrical Characteristics table – Modified foot- note 1.
			Added Oscillator Output Frequency table.
			LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t _{CODO} parameter.
			LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.

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