Lattice Semiconductor Corporation - LFE3-70EA-9FN672I Datasheet



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Details

Product Status	Not For New Designs
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70ea-9fn672i

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LatticeECP3 Family Data Sheet Architecture

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Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sys-DSP[™] Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG[™] port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Figure 2-8. Clock Divider Connections



Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.



as, overflow, underflow and convergent rounding, etc.

- Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-24, the LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2[™] sysDSP block, such that, legacy applications can be targeted to the LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LatticeECP3 sysDSP slices, as shown in Figure 2-25.



Figure 2-24. Simplified sysDSP Slice Block Diagram



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA ¹ , OPOSB, ONEGB ¹	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR ¹	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL ¹	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT ¹	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 ¹ , DQCLK1 ¹	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW ²	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID ¹	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.



SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI



Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
IDK_HS⁴	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)		_	+/—1	mA
IDK⁵	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$		_	+/—1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO} + 0.5V$	_	18		mA

1. $V_{CC},\,V_{CCAUX}$ and V_{CCIO} should rise/fall monotonically.

2. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

3. LVCMOS and LVTTL only.

4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.

5. Applicable to general purpose I/O pins located on the left and right sides of the device.

Hot Socketing Requirements^{1, 2}

Description	Min.	Тур.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	_	-	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.

2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8 mA*16 channels *2 input pins per channel = 256 mA

ESD Performance

Please refer to the LatticeECP3 Product Family Qualification Summary for complete qualification data, including ESD performance.



SERDES Power Supply Requirements^{1, 2, 3}

Symbol	Description	Тур.	Max.	Units
Standby (Power Do	own)	•		1
I _{CCA-SB}	V _{CCA} current (per channel)	3	5	mA
I _{CCIB-SB}	Input buffer current (per channel)		—	mA
I _{CCOB-SB}	Output buffer current (per channel)	—	_	mA
Operating (Data Ra	ite = 3.2 Gbps)		•	•
I _{CCA-OP}	V _{CCA} current (per channel)	68	77	mA
I _{CCIB-OP}	Input buffer current (per channel)	5	7	mA
I _{CCOB-OP}	Output buffer current (per channel)	utput buffer current (per channel) 19 25		mA
Operating (Data Ra	ite = 2.5 Gbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	66	76	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel) 15 18		18	mA
Operating (Data Ra	te = 1.25 Gbps)			·
I _{CCA-OP}	V _{CCA} current (per channel)	62	72	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Ra	ite = 250 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA
Operating (Data Ra	ite = 150 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.

2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

3. Pre-emphasis adds 20 mA to ICCA-OP data.



sysl/O Recommended Operating Conditions

		V _{CCIO}		V _{REF} (V)				
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.		
LVCMOS33 ²	3.135	3.3	3.465	—	—	—		
LVCMOS33D	3.135	3.3	3.465	—	—	—		
LVCMOS25 ²	2.375	2.5	2.625	—	—	—		
LVCMOS18	1.71	1.8	1.89	—	—	—		
LVCMOS15	1.425	1.5	1.575	—	—	—		
LVCMOS12 ²	1.14	1.2	1.26	—	—	—		
LVTTL33 ²	3.135	3.3	3.465	—	—	—		
PCI33	3.135	3.3	3.465	—	—	—		
SSTL15 ³	1.43	1.5	1.57	0.68	0.75	0.9		
SSTL18_I, II ²	1.71	1.8	1.89	0.833	0.9	0.969		
SSTL25_I, II ²	2.375	2.5	2.625	1.15	1.25	1.35		
SSTL33_I, II ²	3.135	3.3	3.465	1.3	1.5	1.7		
HSTL15_l ²	1.425	1.5	1.575	0.68	0.75	0.9		
HSTL18_I, II ²	1.71	1.8	1.89	0.816	0.9	1.08		
LVDS25 ²	2.375	2.5	2.625	—	—	—		
LVDS25E	2.375	2.5	2.625	—	—	—		
MLVDS ¹	2.375	2.5	2.625	—	—	—		
LVPECL33 ^{1, 2}	3.135	3.3	3.465	—	—	—		
Mini LVDS	2.375	2.5	2.625	—	—	—		
BLVDS25 ^{1, 2}	2.375	2.5	2.625		—	—		
RSDS ²	2.375	2.5	2.625	—	—	—		
RSDSE ^{1, 2}	2.375	2.5	2.625	—	—	—		
TRLVDS	3.14	3.3	3.47	—	—	—		
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—		
SSTL15D ³	1.43	1.5	1.57		—	—		
SSTL18D_I ^{2, 3} , II ^{2, 3}	1.71	1.8	1.89		—	—		
SSTL25D_ I ² , II ²	2.375	2.5	2.625	—	—	—		
SSTL33D_ I ² , II ²	3.135	3.3	3.465	—	—	—		
HSTL15D_ I ²	1.425	1.5	1.575	_	—	—		
HSTL18D_ I ² , II ²	1.71	1.8	1.89	—	—	—		

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. For input voltage compatibility, see TN1177, LatticeECP3 sysIO Usage Guide.

3. VREF is required when using Differential SSTL to interface to DDR memory.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-	-8 -7		-6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	_	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA		500		420		375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	_	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	_	4.1	—	4.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	-	0.0	-	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	_	1.4	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	_	1.5	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	_	500	_	420	_	375	MHz
General I/O Pin Pa	rameters Using Dedicated Clock	nput Primary Clock w	ith PLL v	vith Cloc	k Injectio	on Remo	val Settir	וg²	
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	_	3.3	_	3.6	—	39	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
^t H_DELPLL	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	_	3.3	_	3.5	_	3.8	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7		0.8	_	0.9	_	ns

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-	-8	-	-7	-	-6	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 In	puts with Clock and Data (>10bits	s wide) are Aligned at I	Pin (GDD	RX2_RX	.ECLK.A	ligned)	1		
(No CLKDIV)									
Left and Right Side	es Using DLLCLKPIN for Clock Ir			0.005	1	0.005	1	0.005	
^t DVACLKGDDR	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225	
	Data Hold After CLK	ECP3-150EA	0.775	-	0.775		0.775		
^T MAX_GDDR	DDRX2 Clock Frequency	ECP3-150EA	_	460	_	385	_	345	MHZ
^t DVACLKGDDR	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI
^t DVECLKGDDR	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775		0.775	—	UI
fMAX_GDDR	DDRX2 Clock Frequency	ECP3-70EA/95EA		460		385		311	MHZ
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	_	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	—	0.790	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	460	_	385	_	311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	_	0.210	_	0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA		460		385		311	MHz
Top Side Using PC	LK Pin for Clock Input								
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	235	—	170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	235		170	—	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	_	0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA		235		170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA		0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790		0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	235		170		130	MHz
Generic DDRX2 In Input	puts with Clock and Data (<10 Bit	ts Wide) Centered at P	in (GDDF	RX2_RX.I	DQS.Cen	tered) U	sing DQ	S Pin for	Clock
Left and Right Side	es								
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	_	330		352		ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	_	ps
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	_	375	MHz
Generic DDRX2 In	puts with Clock and Data (<10 Bit	ts Wide) Aligned at Pin	(GDDR)	(2_RX.D	QS.Align	ed) Using	g DQS Pi	n for Clo	ck Input
Left and Right Side	es								
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	_	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	_	UI
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz
Generic DDRX1 O	utput with Clock and Data (>10 B	its Wide) Centered at P	in (GDD	RX1_TX.	SCLK.Ce	ntered)10)		
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670		670		ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665		664	—	ps
	Data Valid After CLK	ECP3-70EA/95EA	666		665		664		ps
BIAGDDIT	1	1		I		l			· ·

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

							6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units	
fMAX GDDB	DDRX1 Clock Frequency	ECP3-70EA/95EA		250		250	—	250	MHz	
	Data Valid Before CLK	ECP3-35EA	683	—	688	_	690	_	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	_	688	_	690	_	ps	
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	_	250	MHz	
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	—	688	_	690	_	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	—	ps	
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz	
Generic DDRX1 Ou	Generic DDRX1 Output with Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) ¹⁰									
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps	
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA		335	_	338	—	341	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA		250	_	250	—	250	MHz	
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-70EA/95EA	_	339	_	343	—	347	ps	
t _{DIAGDDR}	Data Invalid After Clock	ECP3-70EA/95EA	_	339	_	343	—	347	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	—	250	MHz	
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-35EA	_	322	_	320	—	321	ps	
t _{DIAGDDR}	Data Invalid After Clock	ECP3-35EA	_	322	_	320	—	321	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	_	250	MHz	
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-17EA	_	322	_	320	_	321	ps	
t _{DIAGDDR}	Data Invalid After Clock	ECP3-17EA	_	322	_	320	_	321	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA		250	_	250	—	250	MHz	
Generic DDRX1 Ou	itput with Clock and Data (<10 Bi	ts Wide) Centered at P	in (GDD	RX1_TX.	DQS.Cen	tered) ¹⁰				
Left and Right Side	es									
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	_	670	—	670	—	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	_	250		250	—	250	MHz	
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	—	652	_	650	_	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	—	250	MHz	
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	670	—	675	—	676	—	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	_	676	_	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	—	250	MHz	
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	—	ps	
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	—	670	—	670	—	ps	
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz	
Generic DDRX2 Ou	itput with Clock and Data (>10 Bi	ts Wide) Aligned at Pir	n (GDDR	X2_TX.A	igned)					
Left and Right Side	es									
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices		200		210		220	ps	
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	_	200	_	210	_	220	ps	
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	_	420	—	375	MHz	
Generic DDRX2 Ou	Itput with Clock and Data (>10 Bi	ts Wide) Centered at P	in Using		L (GDDF	X2_TX.D	QSDLL.	Centered)11	
Left and Right Side	es									
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400		400		431		ps	
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400		400		432		ps	
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz	

Over Recommended Commercial Operating Conditions



LatticeECP3 Internal Switching Characteristics^{1, 2, 5} (Continued)

		-8		-	7	-6		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141		0.145		0.149		ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register		_	0.098	_	0.077	_	ns
DSP Block Tin	ning ³							
t _{SUI_DSP}	Input Register Setup Time	0.32	_	0.36	_	0.39	_	ns
t _{HI_DSP}	Input Register Hold Time	-0.17	_	-0.19	_	-0.21	_	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.23	_	2.30	_	2.37	_	ns
t _{HP_DSP}	Pipeline Register Hold Time		_	-1.09	_	-1.15	_	ns
t _{SUO_DSP}	Output Register Setup Time	3.09	_	3.22	_	3.34	_	ns
t _{HO_DSP}	Output Register Hold Time	-1.67	_	-1.76	_	-1.84	_	ns
t _{COI_DSP}	Input Register Clock to Output Time	_	3.05	—	3.35	_	3.73	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	_	1.30	—	1.47	_	1.64	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t _{SUOPT_DSP}	Opcode Register Setup Time	0.31	_	0.35	_	0.39	_	ns
t _{HOPT_DSP}	Opcode Register Hold Time	-0.20	_	-0.24		-0.27	_	ns
t _{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69		1.94		2.14		ns
t _{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.58		-0.80		-0.97		ns

Over Recommended Commercial Operating Conditions

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Тур.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	_	_	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	_	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	_	_	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	_		0.5	UI, p-p

Note: Values are measured with PRBS 2⁷–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.



SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ^{1, 2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

 Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.

2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.

3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.

4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	_	_	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
F _{VCLK}	Video output clock frequency		27	_	74.25	MHz
DCV	Duty cycle, video clock		45	50	55	%



Figure 3-21. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3-22. sysCONFIG Master Serial Port Timing









Figure 3-26. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-27. Wake-Up Timing





Pin Information Summary (Cont.)

Pin Information Summary			ECP3-17EA		ECP3-35EA			
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	
	Bank 0	13	10	18	13	21	24	
	Bank 1	7	5	12	7	18	18	
	Bank 2	2	2	4	1	8	8	
Emulated Differential I/O per	Bank 3	4	2	13	5	20	19	
Dank	Bank 6	5	1	13	6	22	20	
	Bank 7	6	9	10	6	11	13	
	Bank 8	12	12	12	12	12	12	
	Bank 0	0	0	0	0	0	0	
	Bank 1	0	0	0	0	0	0	
	Bank 2	2	2	3	3	6	6	
Highspeed Differential I/O per	Bank 3	5	4	9	4	9	12	
Dank	Bank 6	5	4	9	4	11	12	
	Bank 7	5	6	8	5	9	10	
	Bank 8	0	0	0	0	0	0	
	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24	
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18	
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14	
Differential I/O per Bank	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31	
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32	
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23	
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12	
	Bank 0	2	1	3	2	3	4	
	Bank 1	1	0	2	1	3	3	
	Bank 2	0	0	1	0	2	2	
DDR Groups Bonded per	Bank 3	1	0	3	1	3	4	
Bank [∠]	Bank 6	1	0	3	1	4	4	
	Bank 7	1	2	2	1	3	3	
	Configuration Bank 8	0	0	0	0	0	0	
SERDES Quads		1	1	1	1	1	1	

These pins must remain floating on the board.
 Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.