E. Lattice Semiconductor Corporation - <u>LFE3-95EA-6FN1156C Datasheet</u>



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-6fn1156c

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Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.



Figure 2-5. Delay Locked Loop Diagram (DLL)

* This signal is not user accessible. This can only be used to feed the slave delay line.



Figure 2-8. Clock Divider Connections



Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.



Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)

The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

Figure 2-25. Detailed sysDSP Slice Diagram

Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

 Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	_

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

Figure 2-27. MAC DSP Element

MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution

DQS Strobe and Transition Detect Logic

I/O Ring

*Includes shared configuration I/Os and dedicated configuration I/Os.

To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysl/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

sysl/O Buffer Banks

LatticeECP3 devices have six sysl/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysl/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysl/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2} , which allow it to be completely independent from the others. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-8 -7		-	-6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	_	250	_	250	MHz
Generic DDRX2 In Input	puts with Clock and Data (>10	Bits Wide) Centered at P	in (GDDF	RX2_RX.E	CLK.Ce	ntered) L	Ising PC	LK Pin fo	or Clock
Left and Right Sid	les								
t _{SUGDDR}	Data Setup Before CLK	ECP3-150EA	321		403		471		ps
t _{HOGDDR}	Data Hold After CLK	ECP3-150EA	321	_	403	—	471	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA		405	_	325	_	280	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	321		403		535		ps
t _{HOGDDR}	Data Hold After CLK	ECP3-70EA/95EA	321	_	403		535	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA		405	_	325	_	250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-35EA	335		425		535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-35EA	335		425		535	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	405	_	325		250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-17EA	335		425		535		ps
t _{HOGDDR}	Data Hold After CLK	ECP3-17EA	335		425		535		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	405		325		250	MHz
Generic DDRX2 In	puts with Clock and Data (>10	Bits Wide) Aligned at Pin	(GDDR)	(2_RX.EC	CLK.Alig	ned)	•		
Left and Right Sid	le Using DLLCLKIN Pin for Cloo	ck Input							
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775		0.775	_	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	460	_	385		345	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	—	0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	_	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	460	—	385	_	311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	_	0.210	_	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	_	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	460	—	385		311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210	_	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	_	0.790	—	0.790	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA		460		385	_	311	MHz
Top Side Using P	CLK Pin for Clock Input								
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA		0.225	_	0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775		0.775	_	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA		235		170	—	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	_	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA		235		170	_	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA		0.210	_	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	_	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA		235		170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA		0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790		0.790		0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz

Over Recommended Commercial Operating Conditions

Figure 3-7. DDR/DDR2/DDR3 Parameters

LatticeECP3 Internal Switching Characteristics^{1, 2, 5} (Continued)

		_	8	-7		-6		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.141		0.145		0.149		ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118	_	0.098	_	0.077	_	ns
DSP Block Tin	ning ³							
t _{SUI_DSP}	Input Register Setup Time	0.32	_	0.36	_	0.39	_	ns
t _{HI_DSP}	Input Register Hold Time	-0.17	_	-0.19	_	-0.21	_	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.23	_	2.30	_	2.37	_	ns
t _{HP_DSP}	Pipeline Register Hold Time	-1.02	_	-1.09	_	-1.15	_	ns
t _{SUO_DSP}	Output Register Setup Time	3.09	_	3.22	_	3.34	_	ns
t _{HO_DSP}	Output Register Hold Time	-1.67	_	-1.76	_	-1.84	_	ns
t _{COI_DSP}	Input Register Clock to Output Time	_	3.05	_	3.35	_	3.73	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	_	1.30	_	1.47	_	1.64	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t _{SUOPT_DSP}	Opcode Register Setup Time	0.31	_	0.35	_	0.39	_	ns
t _{HOPT_DSP}	Opcode Register Hold Time	-0.20	_	-0.24		-0.27	_	ns
t _{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.69		1.94		2.14		ns
t _{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.58		-0.80		-0.97		ns

Over Recommended Commercial Operating Conditions

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.

LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Over Recommended Commercial	Operating	Conditions
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Buffer Type	Description	-8	-7	-6	Units
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	-0.12	-0.13	-0.14	ns

1. Timing adders are characterized but not tested on every device.

2. LVCMOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.

5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

6. This data does not apply to the LatticeECP3-17EA device.

7. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Тур.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	_	_	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	_	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	_	_	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	_		0.5	UI, p-p

Note: Values are measured with PRBS 2⁷–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF}	Differential rise/fall time	20%-80%	_	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{2, 3, 4}	Output data deterministic jitter		_	—	0.17	UI
J _{TX_TJ} ^{1, 2, 3, 4}	Total output data jitter		_	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.

2. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	_	_	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	_	_	dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{1, 2, 3}	Deterministic jitter tolerance (peak-to-peak)		—		0.37	UI
J _{RX_RJ} ^{1, 2, 3}	Random jitter tolerance (peak-to-peak)		—		0.18	UI
J _{RX_SJ} ^{1, 2, 3}	Sinusoidal jitter tolerance (peak-to-peak)		—	_	0.10	UI
J _{RX_TJ} ^{1, 2, 3}	Total jitter tolerance (peak-to-peak)		—	_	0.65	UI
T _{RX_EYE}	Receiver eye opening		0.35			UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.

LatticeECP3 sysCONFIG Port Timing Specifications

Parameter	r Description			Max.	Units
POR, Confi	guration Initialization, and Wakeup				1
	Time from the Application of V_{CC} , V_{CCAUX} or V_{CCIO8}^{*} (Whichever	Master mode		23	ms
t _{ICFG}	is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Slave mode	—	6	ms
t _{VMC}	Time from t _{ICFG} to the Valid Master MCLK		—	5	μs
t _{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low		_	37	ns
t _{DINIT} 1	PROGRAMN High to INITN High Delay		—	1	ms
t _{MWC}	Additional Wake Master Clock Signals After DONE Pin is High		100	500	cycles
t _{CZ}	MCLK From Active To Low To High-Z		—	300	ns
t _{IODISS}	User I/O Disable from PROGRAMN Low			100	ns
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequer	ice		100	ns
All Configu	ration Modes				
t _{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t _{HCDI}	Data Hold Time to CCLK/MCLK		1	—	ns
t _{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Seria	l				1
t _{SSCH}	CCLK Minimum High Pulse	5	—	ns	
t _{SSCL}	CCLK Minimum Low Pulse		5	_	ns
	Without encryption		_	33	MHz
ICCLK	CCLK Frequency	With encryption		20	MHz
Master and	Slave Parallel	1			
t _{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t _{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t _{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	_	ns
t _{HWD}	WRITEN Hold Time to CCLK/MCLK		1	_	ns
t _{DCB}	CCLK/MCLK to BUSY Delay Time		_	12	ns
t _{CORD}	CCLK to Out for Read Data		_	12	ns
t _{BSCH}	CCLK Minimum High Pulse		6	_	ns
t _{BSCL}	CCLK Minimum Low Pulse		6	_	ns
t _{BSCYC}	Byte Slave Cycle Time		30	—	ns
		Without encryption		33	MHz
[†] CCLK	CCLK/MCLK Frequency	With encryption		20	MHz
Master and	Slave SPI			1	1
t _{CFGX}	INITN High to MCLK Low			80	ns
t _{CSSPI}	INITN High to CSSPIN Low		0.2	2	μs
t _{SOCDO}	MCLK Low to Output Valid			15	ns
t _{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		μs
,		Without encryption		33	MHz
[†] CCLK	CCLK Frequency	With encryption		20	MHz
t _{SSCH}	CCLK Minimum High Pulse		5	_	ns

Over Recommended Operating Conditions

sysl/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V _{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V _{ID}	Input differential voltage	150	_	1200	mV
V _{ICM}	Input common mode voltage	3	_	3.265	V
V _{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R _T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.

Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
Z _O	Single-ended PCB trace impedance	30	50	75	Ohms
R _T	Differential termination resistance	50	100	150	Ohms
V _{OD}	Output voltage, differential, V _{OP} - V _{OM}	300	_	600	mV
V _{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V _{OD} , between H and L	—	_	50	mV
ΔV_{ID}	Change in V _{OS} , between H and L	—	_	50	mV
V _{THD}	Input voltage, differential, V _{INP} - V _{INM}	200	_	600	mV
V _{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	0.3+(V _{THD} /2)	_	2.1-(V _{THD} /2)	
T _R , T _F	Output rise and fall times, 20% to 80%	—	_	550	ps
T _{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.