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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-6fn1156i

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, [LatticeECP3 Memory Usage Guide](#).

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

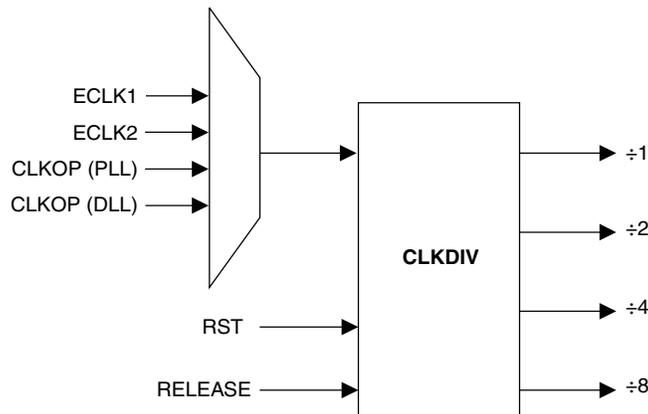
Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-8. Clock Divider Connections



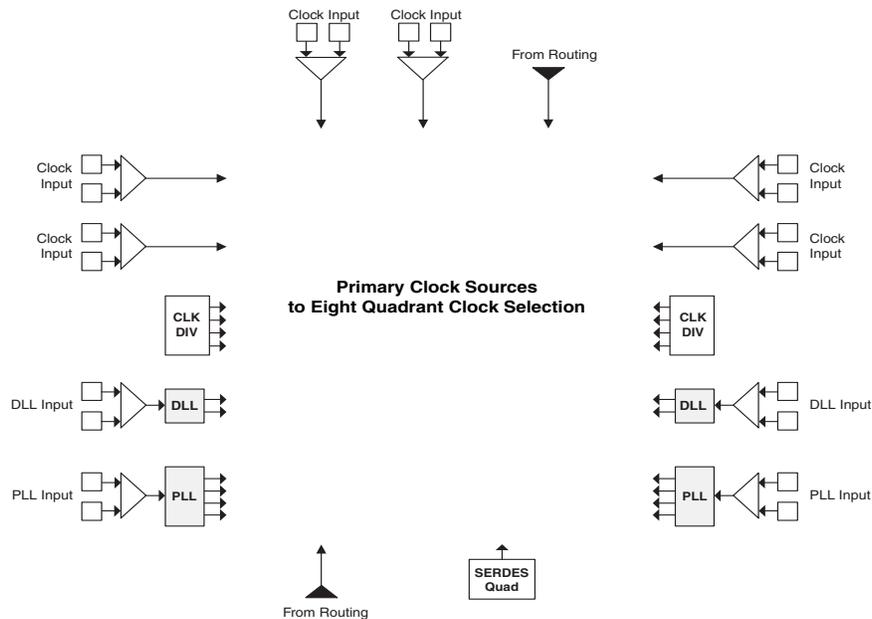
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-10. Primary Clock Sources for LatticeECP3-35

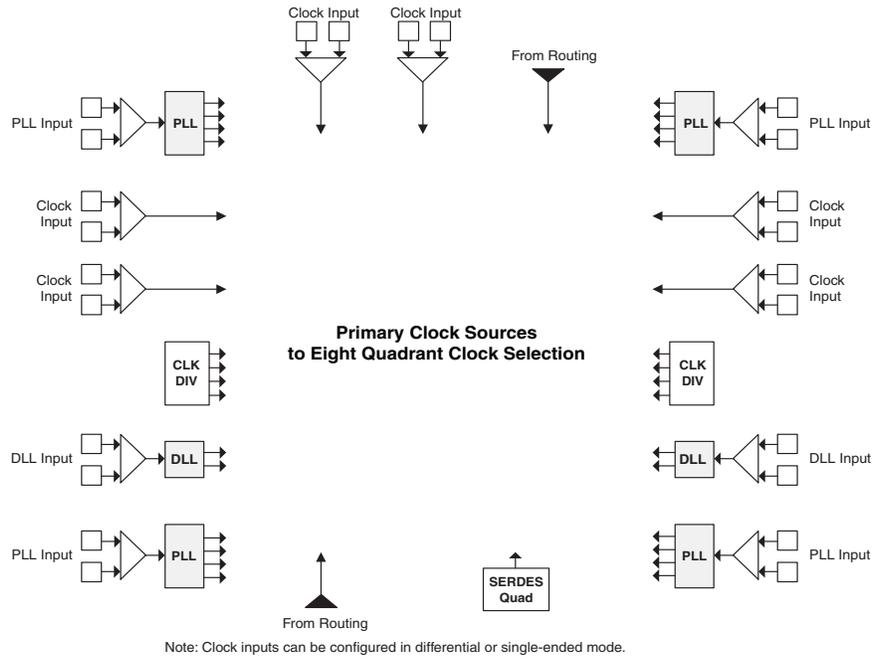
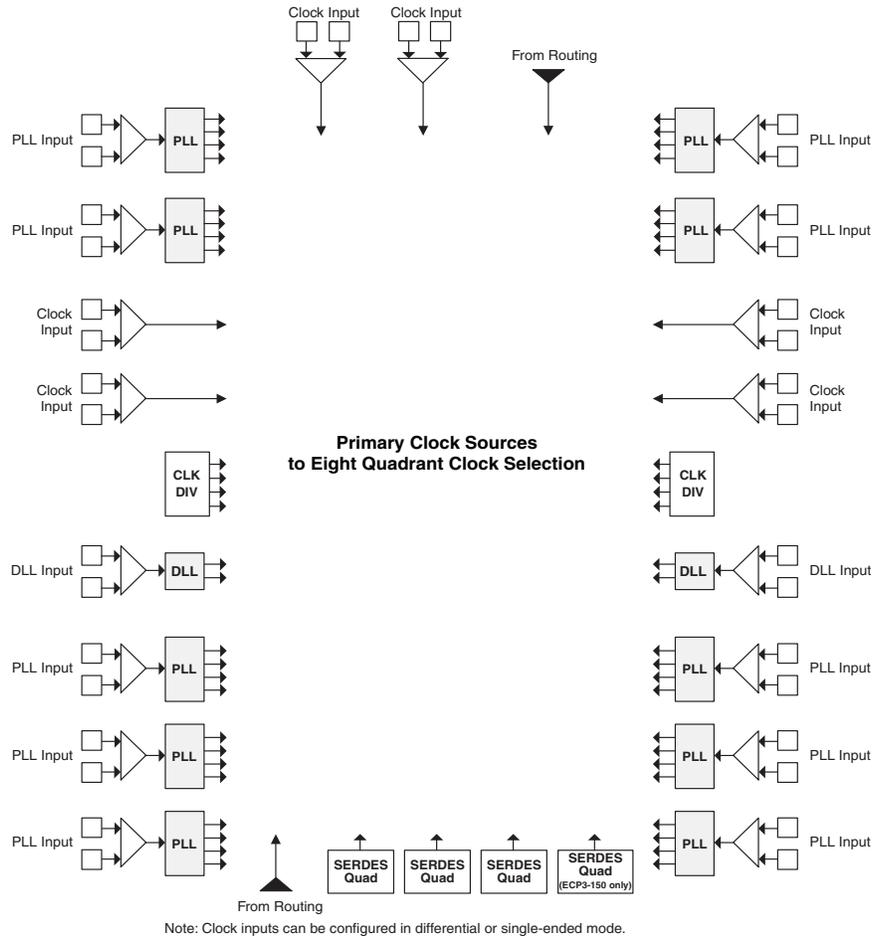


Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150

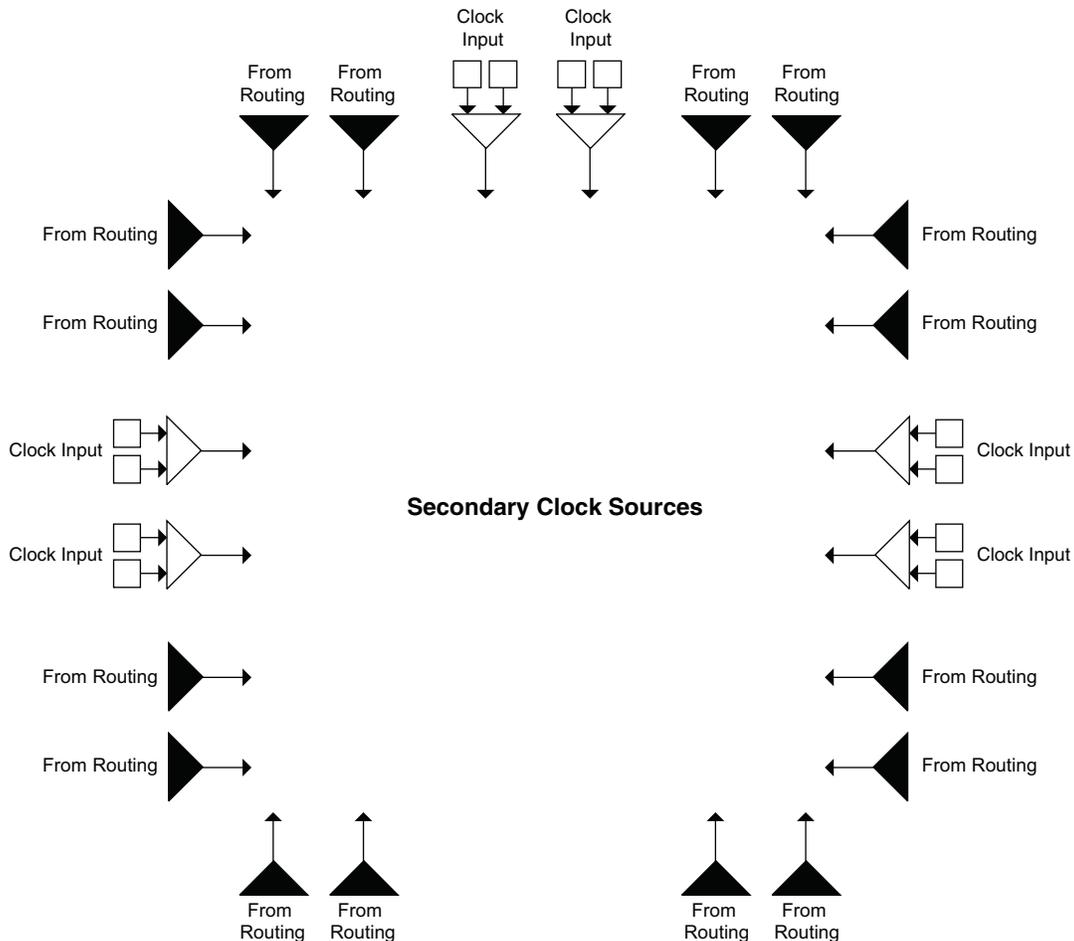


Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

Figure 2-14. Secondary Clock Sources

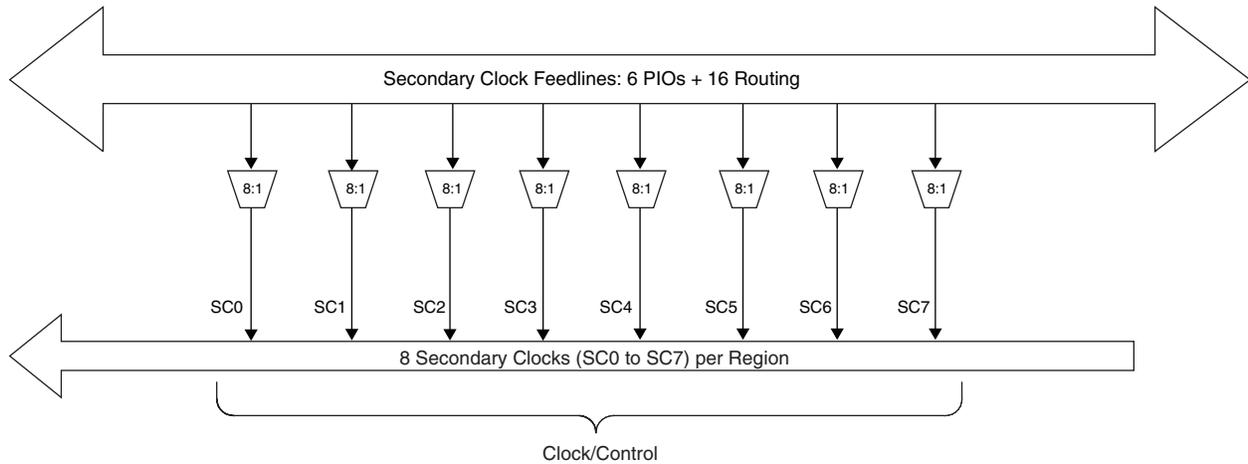


Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

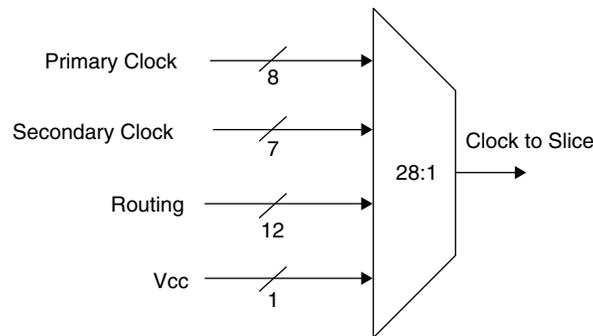
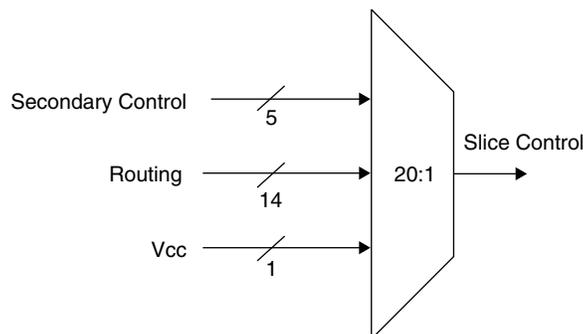


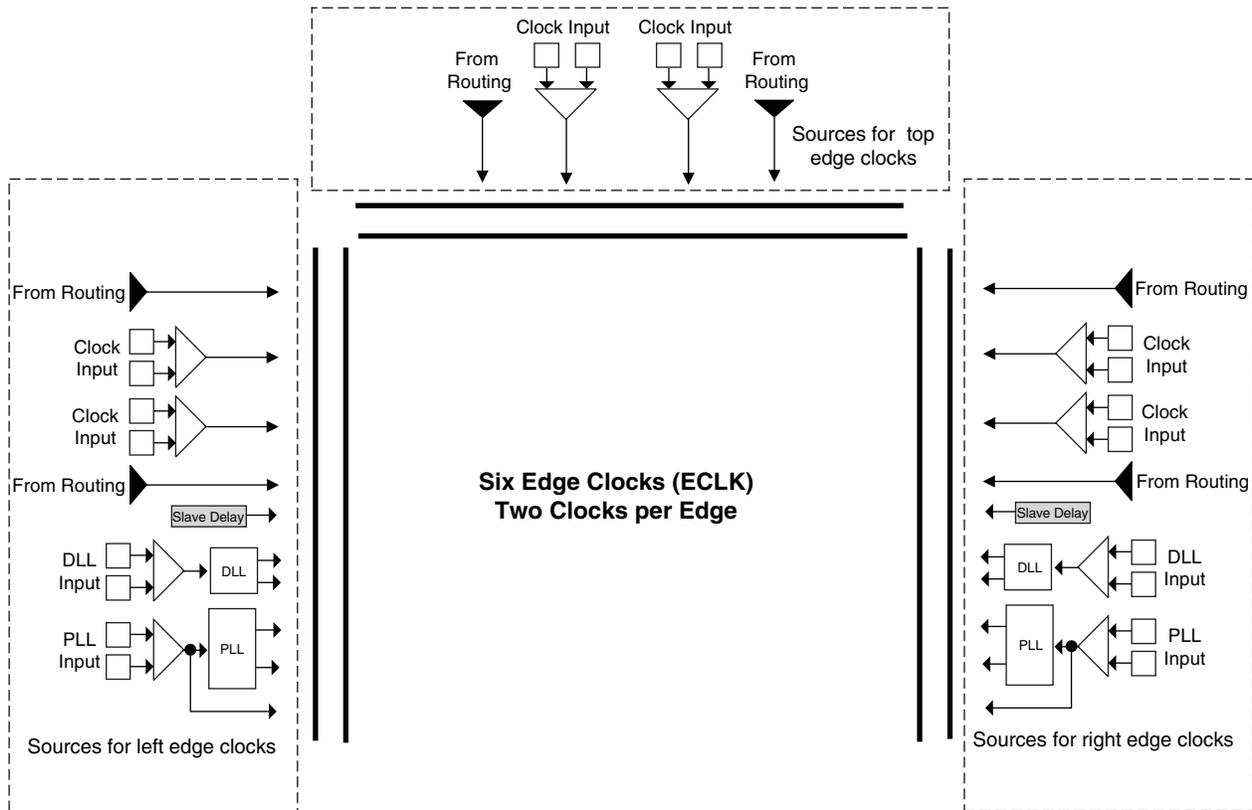
Figure 2-18. Slice0 through Slice2 Control Selection



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

Figure 2-19. Edge Clock Sources



Notes:

1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

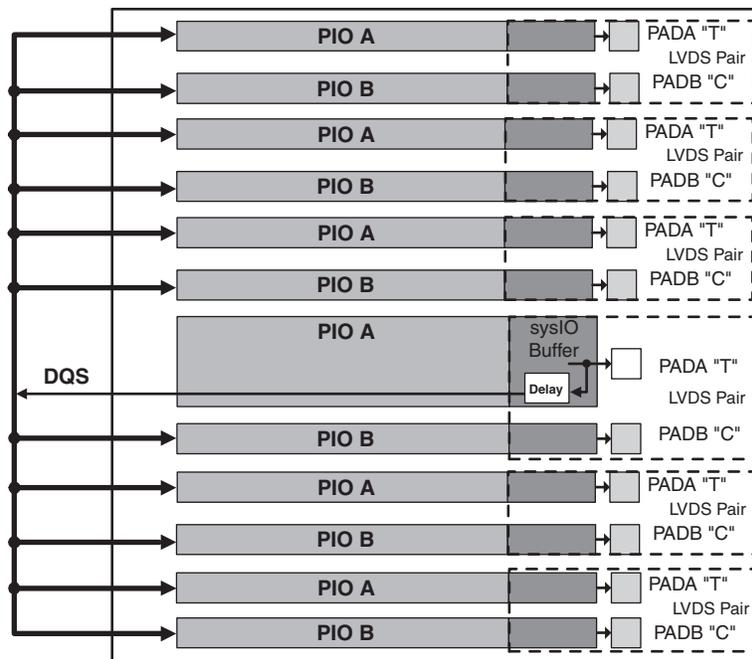
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



LatticeECP3 Supply Current (Standby)^{1, 2, 3, 4, 5, 6}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical		Units
			-6L, -7L, -8L	-6, -7, -8	
I _{CC}	Core Power Supply Current	ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
		ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
I _{CCAUX}	Auxiliary Power Supply Current	ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
		ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
I _{CCPLL}	PLL Power Supply Current (Per PLL)	ECP-17EA	0.0	0.0	mA
		ECP3-35EA	0.1	0.1	mA
		ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
		ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I _{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
I _{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
		ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a "blank" configuration data file.
5. T_J = 85 °C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS18	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS15	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS12	-0.3	$0.35 V_{CC}$	$0.65 V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI33	-0.3	$0.3 V_{CCIO}$	$0.5 V_{CCIO}$	3.6	$0.1 V_{CCIO}$	$0.9 V_{CCIO}$	1.5	-0.5
SSTL18_I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
SSTL18_II (DDR2 Memory)	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.28	$V_{CCIO} - 0.28$	8	-8
							11	-11
SSTL2_I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
							12	-12
SSTL2_II (DDR Memory)	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
							20	-20
SSTL3_I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL3_II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL15 (DDR3 Memory)	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.3	$V_{CCIO} - 0.3$	7.5	-7.5
						$V_{CCIO} * 0.8$	9	-9
HSTL15_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
HSTL18_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
							12	-12
HSTL18_II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16

1. For electromigration, the average DC current drawn by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed $n * 8$ mA, where n is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

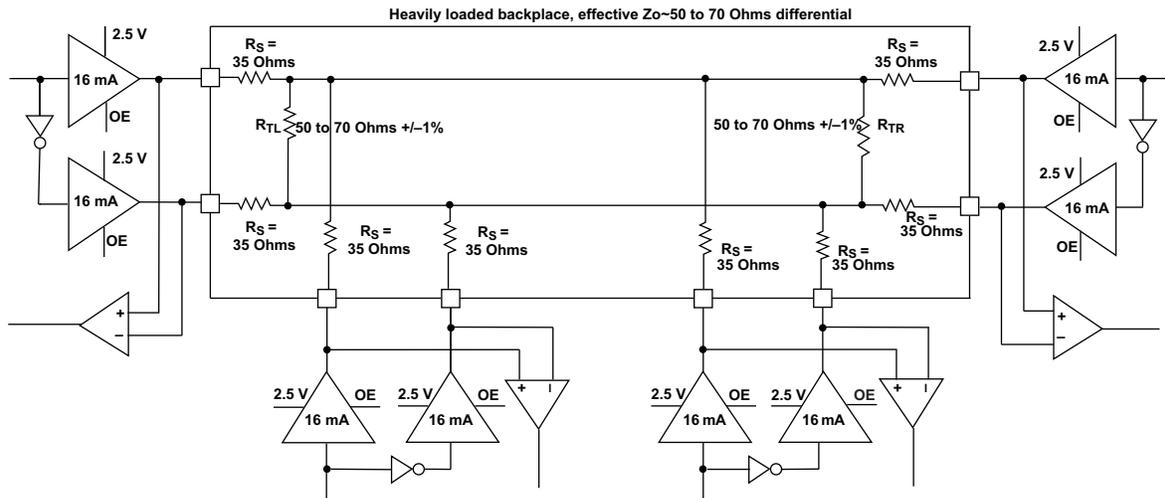


Table 3-5. MLVDS25 DC Conditions¹

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R _{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R _{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V _{OH}	Output High Voltage	1.52	1.60	V
V _{OL}	Output Low Voltage	0.98	0.90	V
V _{OD}	Output Differential Voltage	0.54	0.70	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

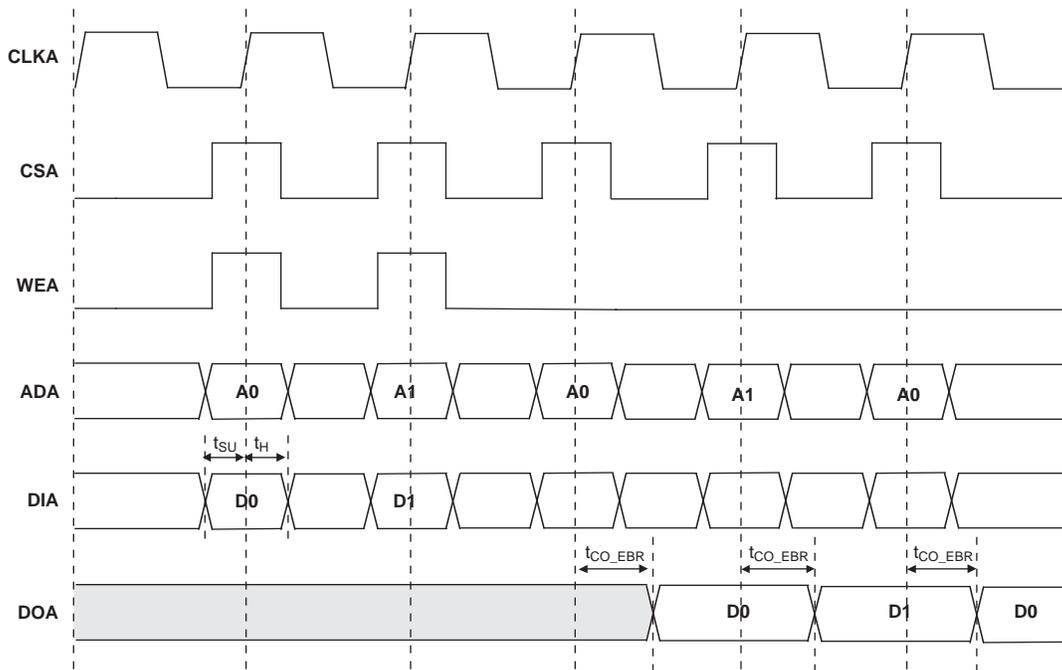
LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDR2_RX.ECLK.Aligned) (No CLKDIV)									
Left and Right Sides Using DLLCLKPIN for Clock Input									
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	460	—	385	—	345	MHz
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	460	—	385	—	311	MHz
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	460	—	385	—	311	MHz
t _{DVACKGDDR}	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	460	—	385	—	311	MHz
Top Side Using PCLK Pin for Clock Input									
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—	235	—	170	—	130	MHz
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	—	235	—	170	—	130	MHz
t _{DVACKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	—	235	—	170	—	130	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR2_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left and Right Sides									
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDR2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
t _{DVACKGDDR}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDR1_TX.SCLK.Centered)¹⁰									
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	666	—	665	—	664	—	ps

Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

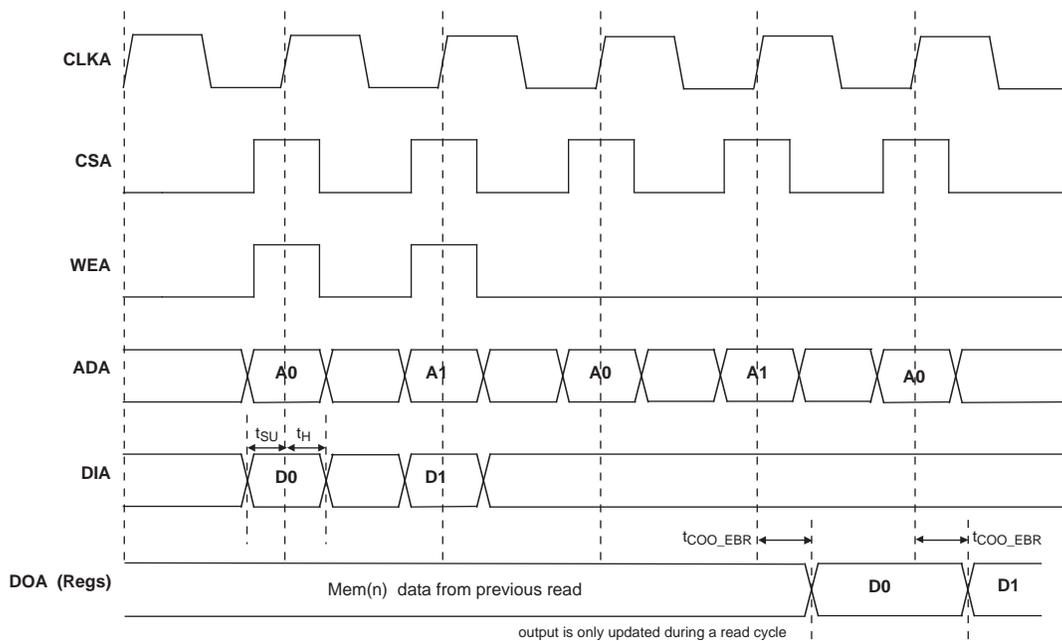
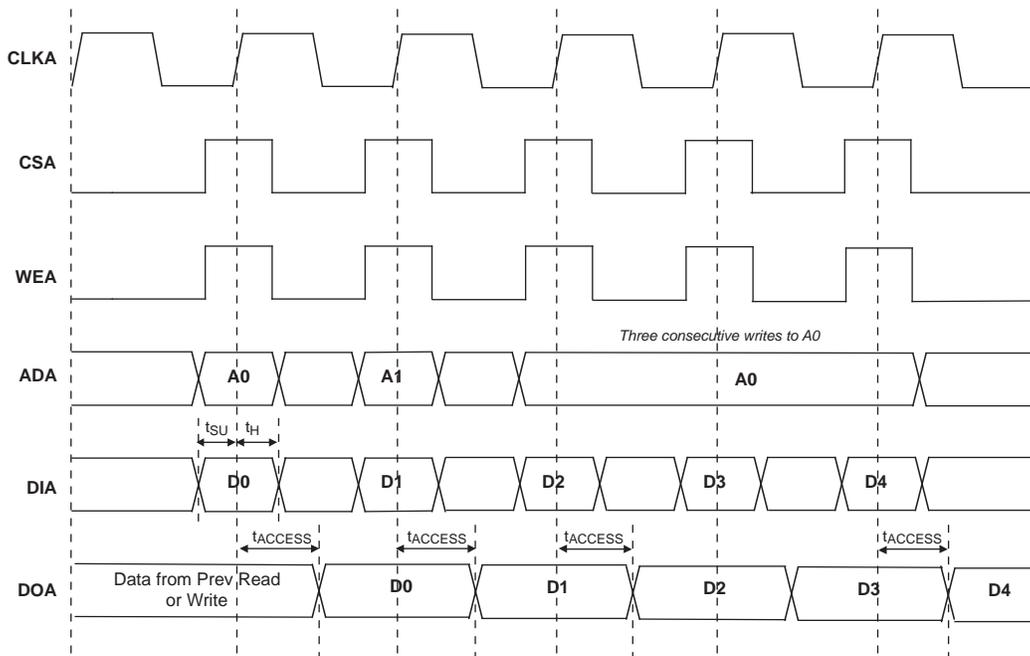


Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7}
Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
Input Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
RS25	RS25, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
PPLVDS	Point-to-Point LVDS	0.03	-0.01	-0.03	ns
TRLVDS	Transition-Reduced LVDS	0.03	0.00	-0.04	ns
Mini MLVDS	Mini LVDS	0.03	-0.01	-0.03	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns
LVTTTL33	LVTTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC33	LVC33, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVC25	LVC25, VCCIO = 2.5 V	0.00	0.00	0.00	ns
LVC18	LVC18, VCCIO = 1.8 V	-0.13	-0.13	-0.13	ns
LVC15	LVC15, VCCIO = 1.5 V	-0.07	-0.07	-0.07	ns
LVC12	LVC12, VCCIO = 1.2 V	-0.20	-0.19	-0.19	ns
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns
Output Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns
LVDS25	LVDS, VCCIO = 2.5 V	-0.11	-0.07	-0.03	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns

Figure 3-16. Jitter Transfer – 1.25 Gbps

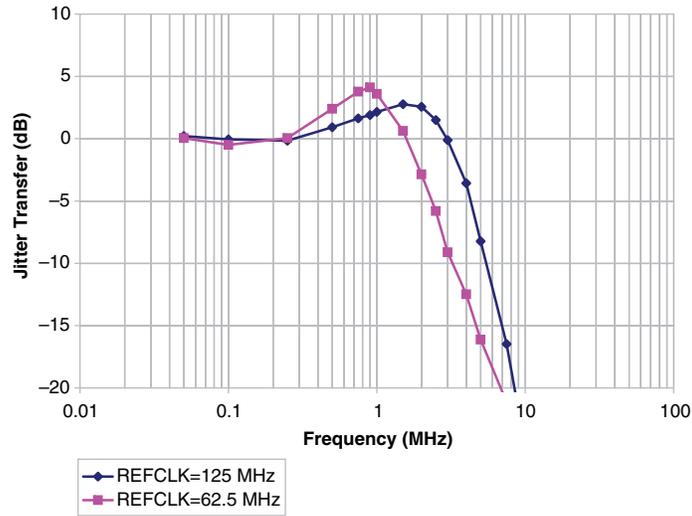
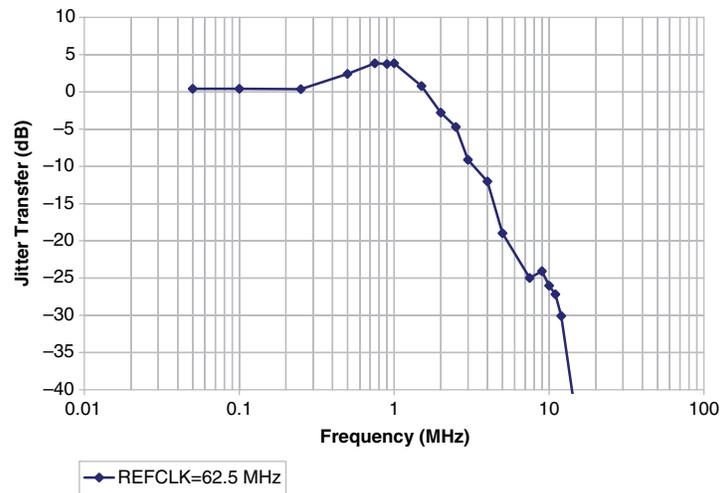


Figure 3-17. Jitter Transfer – 622 Mbps



SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ^{1,2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

- Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{CLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
- Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
- All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
- The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

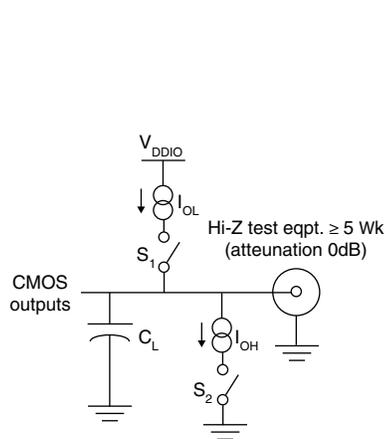
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR _{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

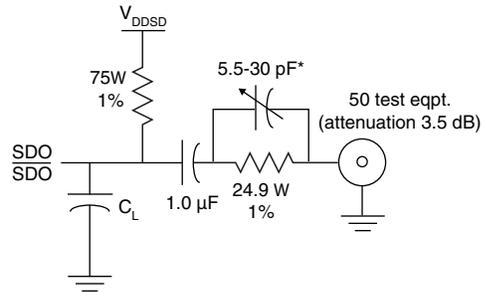
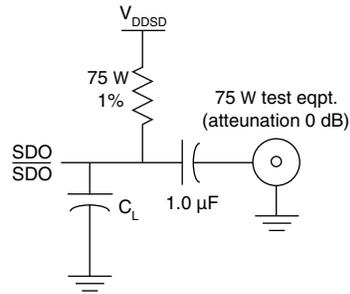
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F _{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC _V	Duty cycle, video clock		45	50	55	%

Figure 3-19. Test Loads

Test Loads

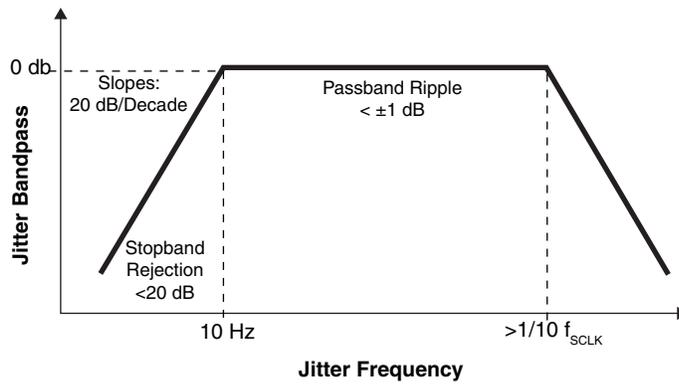


C_L including probe and jig capacitance, 3 pF max.
 S_1 - open, S_2 - closed for V_{OH} measurement.
 S_1 - closed, S_2 - open for V_{OL} measurement.



*Risetime compensation.

Timing Jitter Bandpass



Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSN/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank ²	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Commercial

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.