Lattice Semiconductor Corporation - LFE3-95EA-6LFN484C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-6lfn484c

LatticeECP3 Family Data Sheet Introduction

February 2012 Data Sheet DS1021

Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

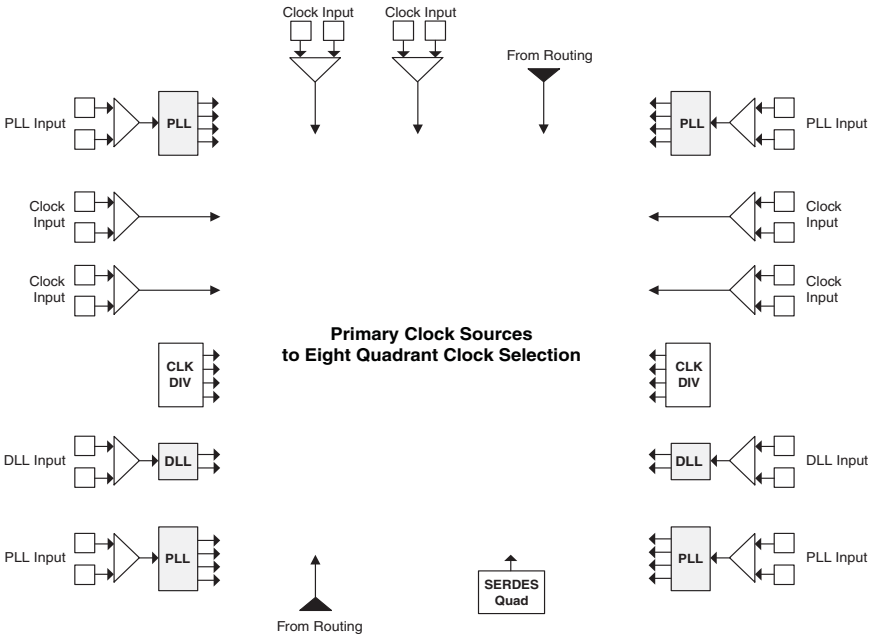
The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

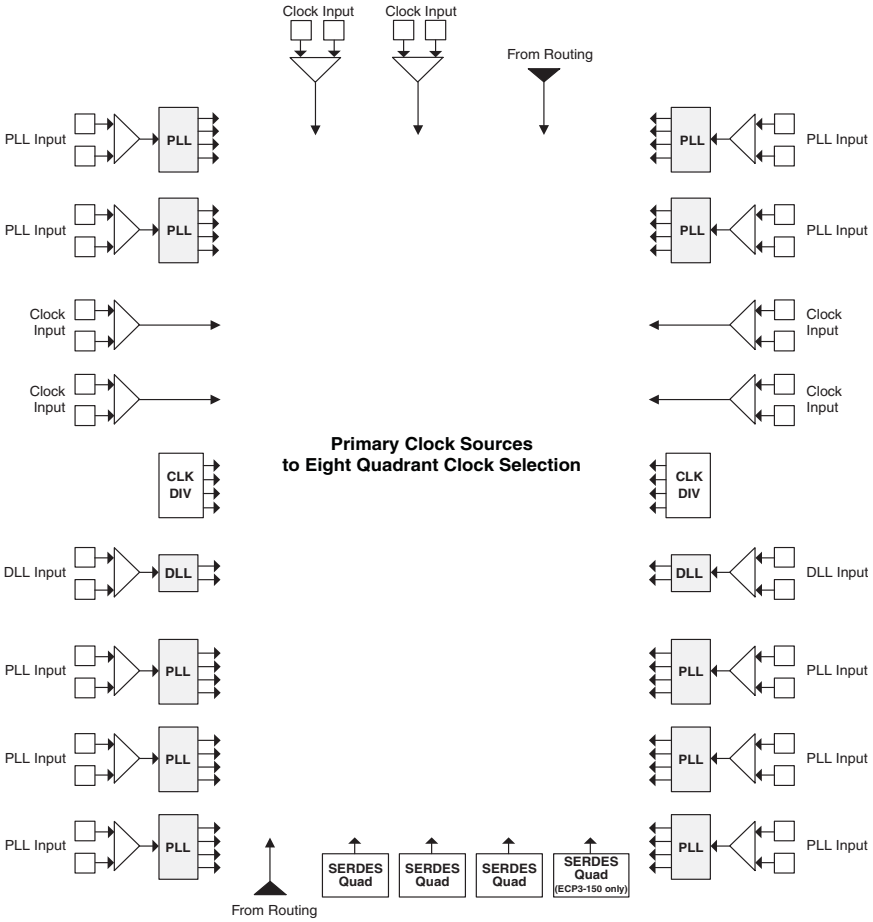
Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-10. Primary Clock Sources for LatticeECP3-35



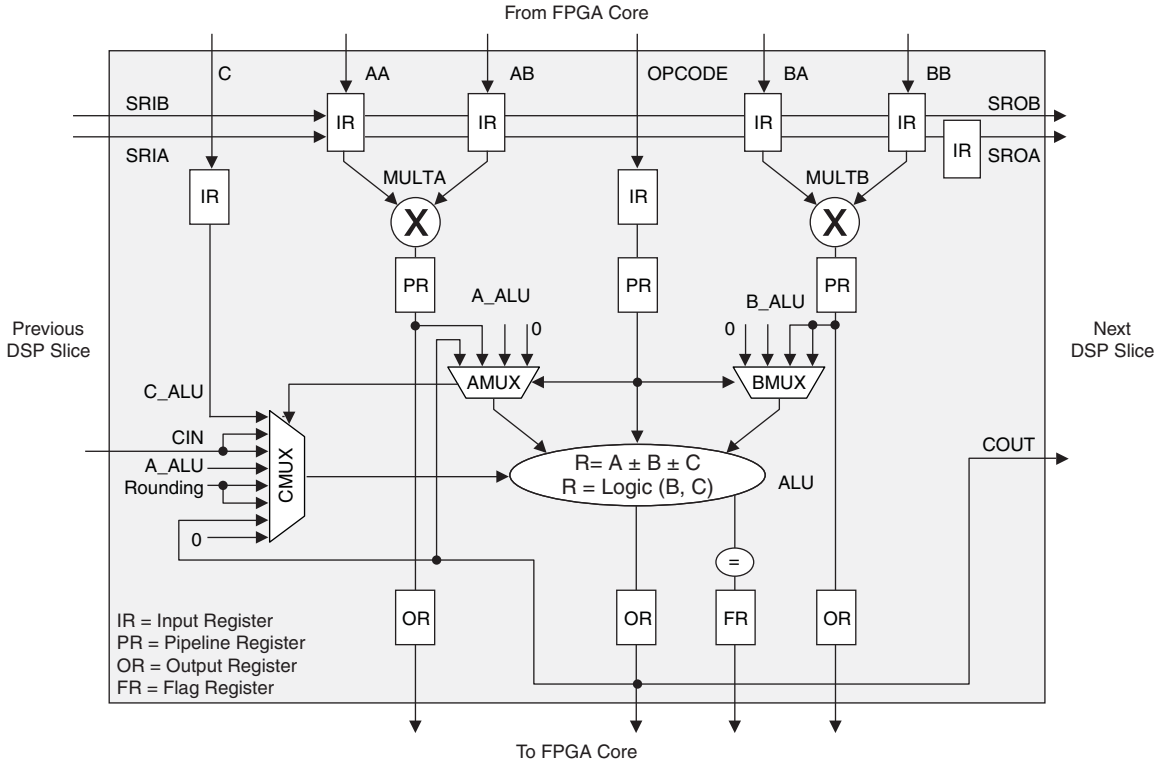
Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-25. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

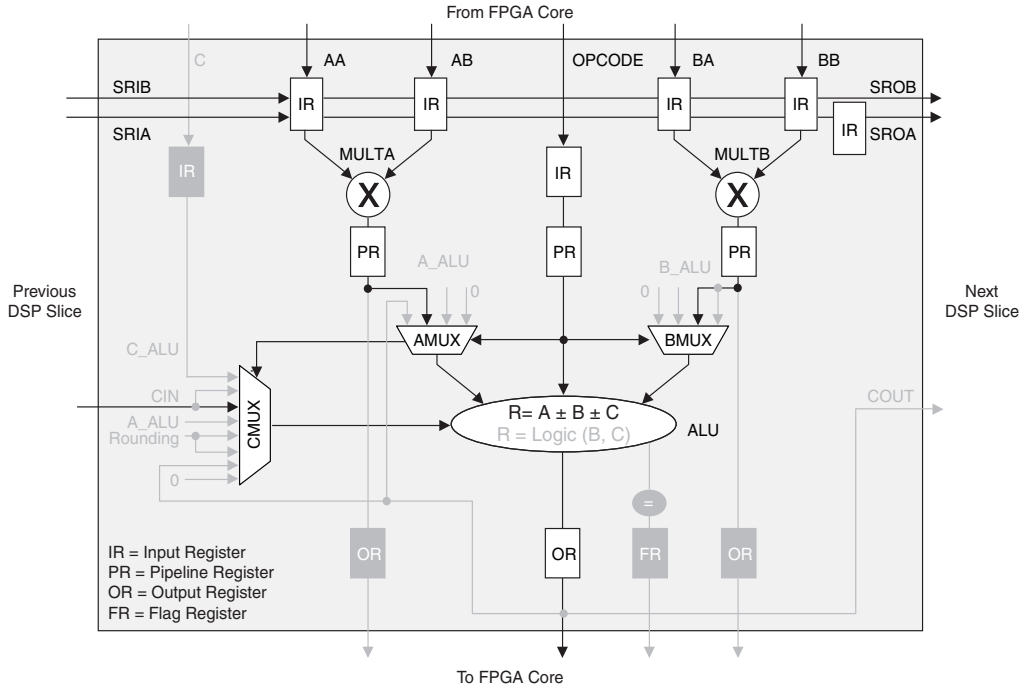
Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

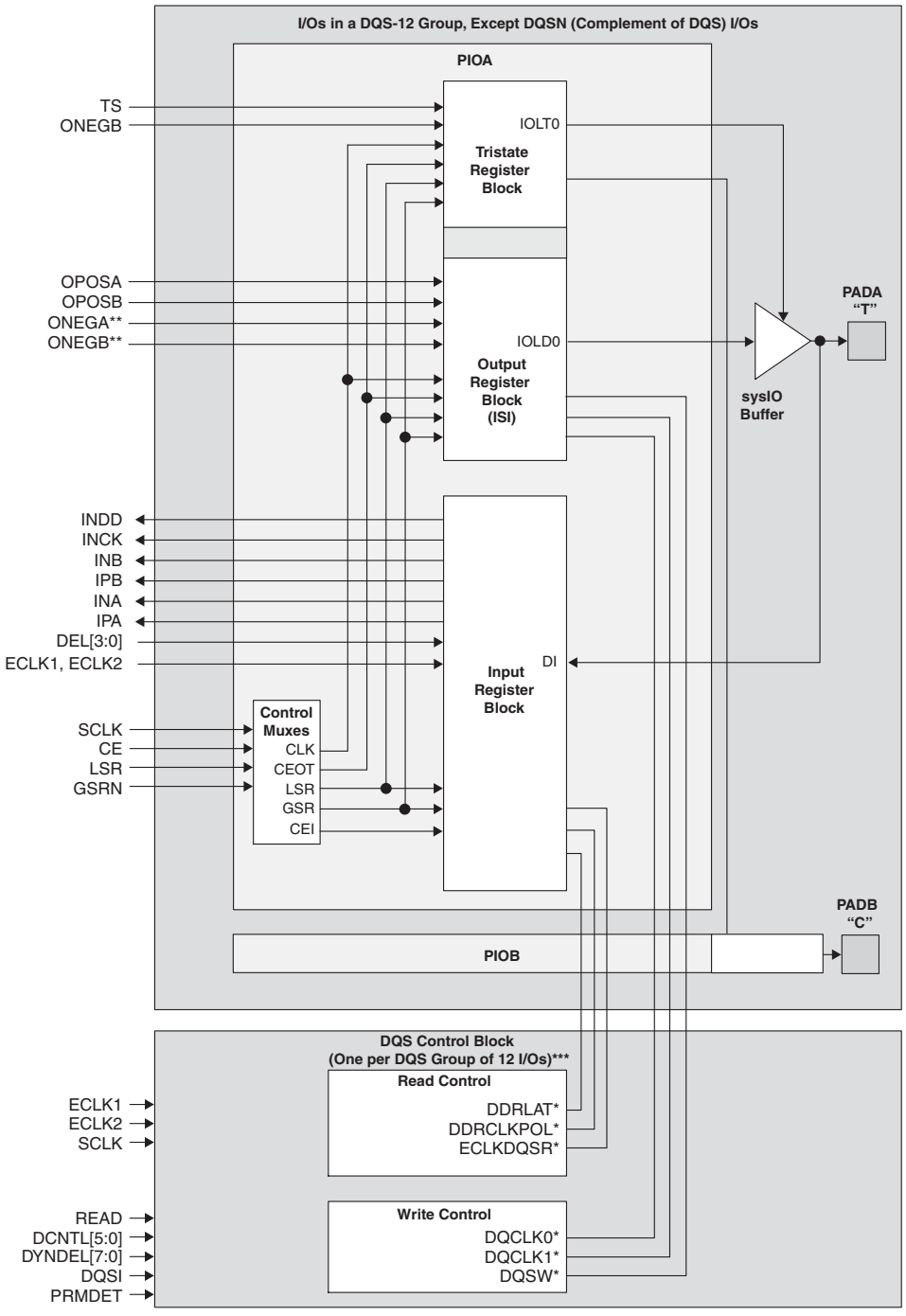
The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-35. DQS Grouping on the Left, Right and Top Edges

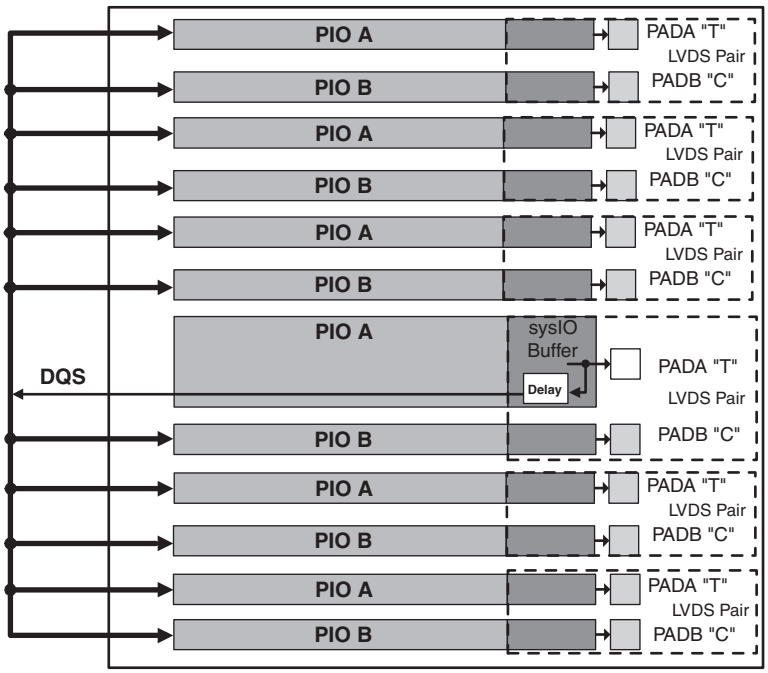
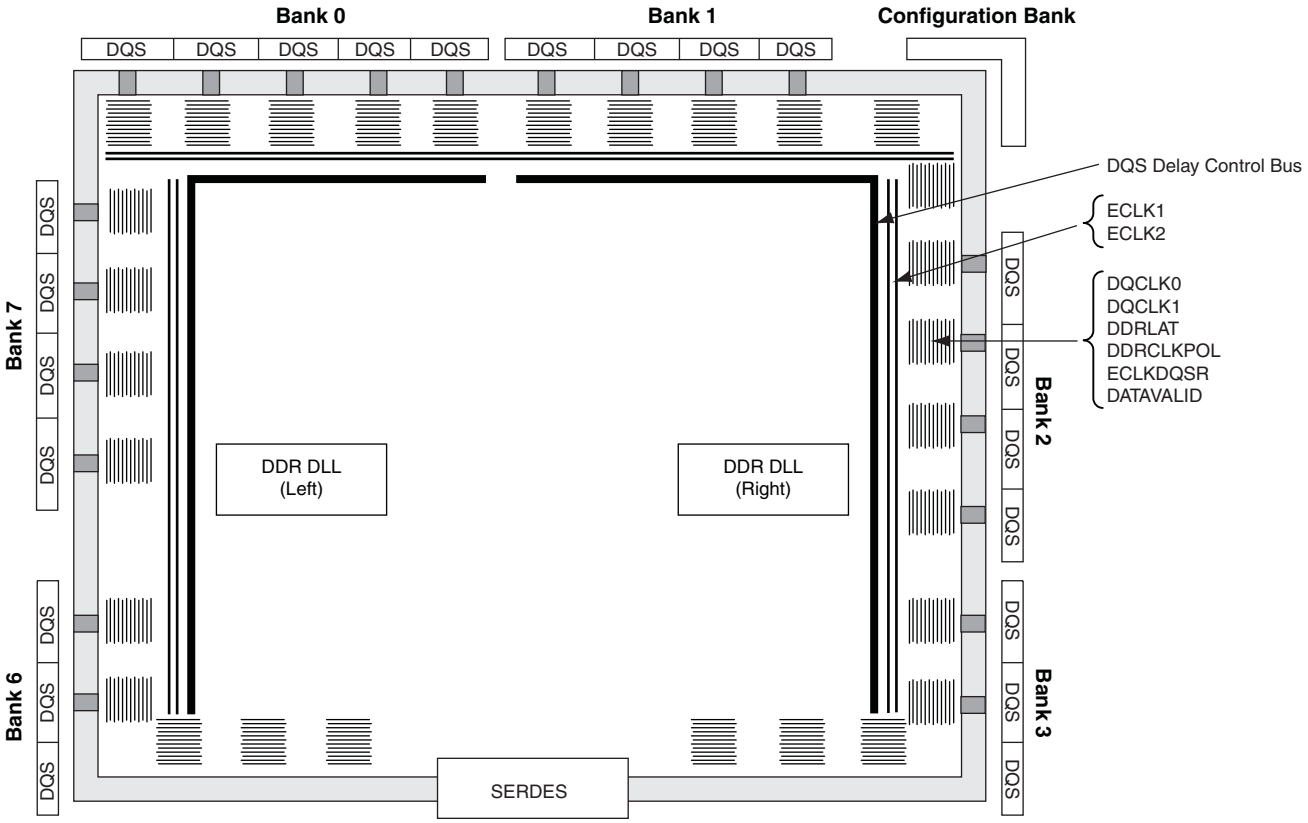


Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



*Includes shared configuration I/Os and dedicated configuration I/Os.

Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)

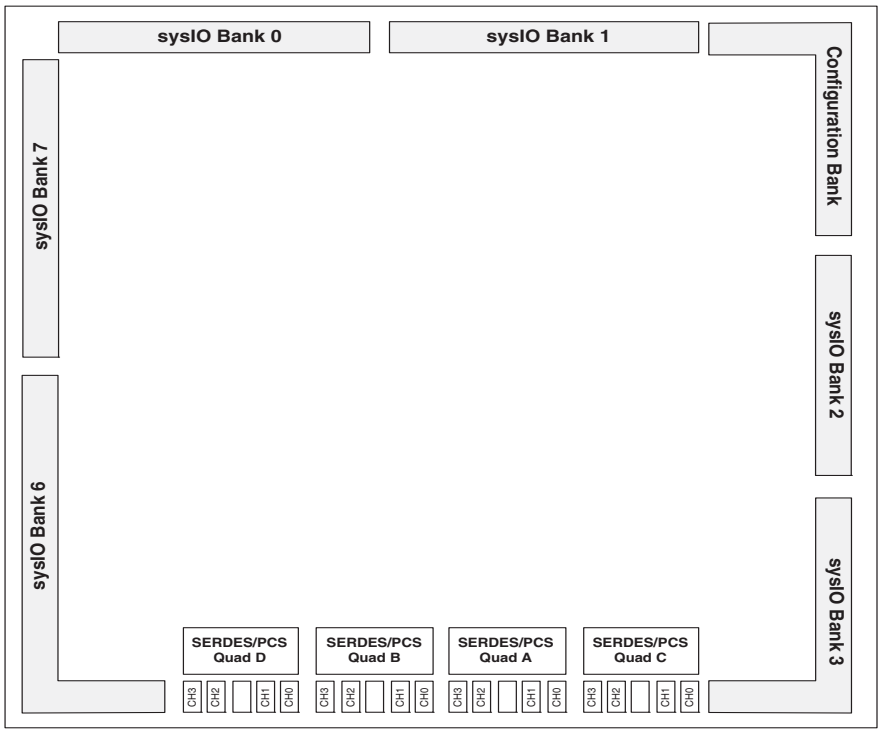


Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143[1], 177[1], 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3[2]	155.52	x1	N/A
SONET-STS-12[2]	622.08	x1	N/A
SONET-STS-48[2]	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.
2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.

Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

MCCLK (MHz)	MCCLK (MHz)
	10
2.5[1]	13
4.3	15[2]
5.4	20
6.9	26
8.1	33[3]
9.2	

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.
2. Maximum MCCLK with encryption enabled.
3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the LatticeECP3 Pin Migration Tables and Diamond software for specific restrictions and limitations.

LatticeECP3 Family Data Sheet DC and Switching Characteristics

April 2014 Data Sheet DS1021

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . –0.5 V to 1.32 V

Supply Voltage V_{CCAUX} . . . . . –0.5 V to 3.75 V

Supply Voltage V_{CCJ} . . . . . –0.5 V to 3.75 V

Output Supply Voltage V_{CCIO} . . . . . –0.5 V to 3.75 V

Input or I/O Tristate Voltage Applied[4]. . . –0.5 V to 3.75 V

Storage Temperature (Ambient) . . . . . .–65 V to 150 °C

Junction Temperature (T_J) . . . . . .+125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3.3 V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

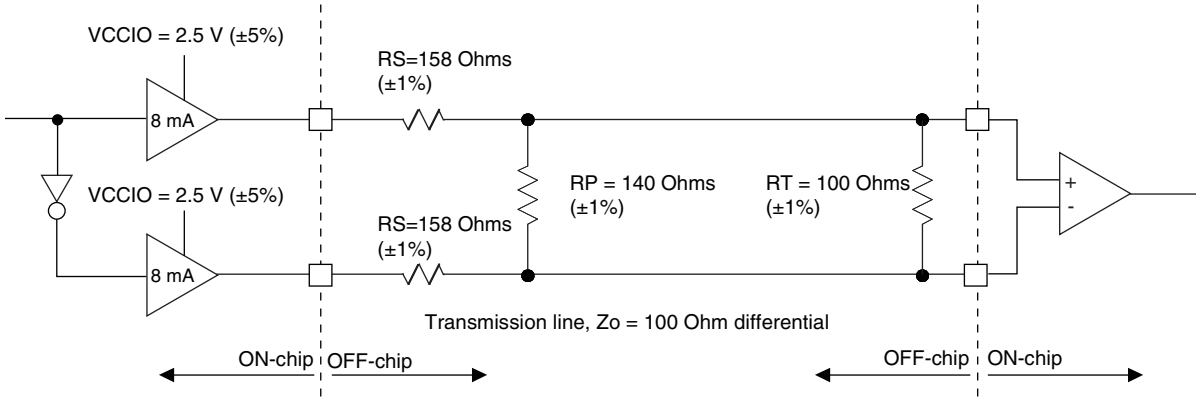


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	158	Ω
R_P	Driver Parallel Resistor (+/–1%)	140	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

MLVDS25

The LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

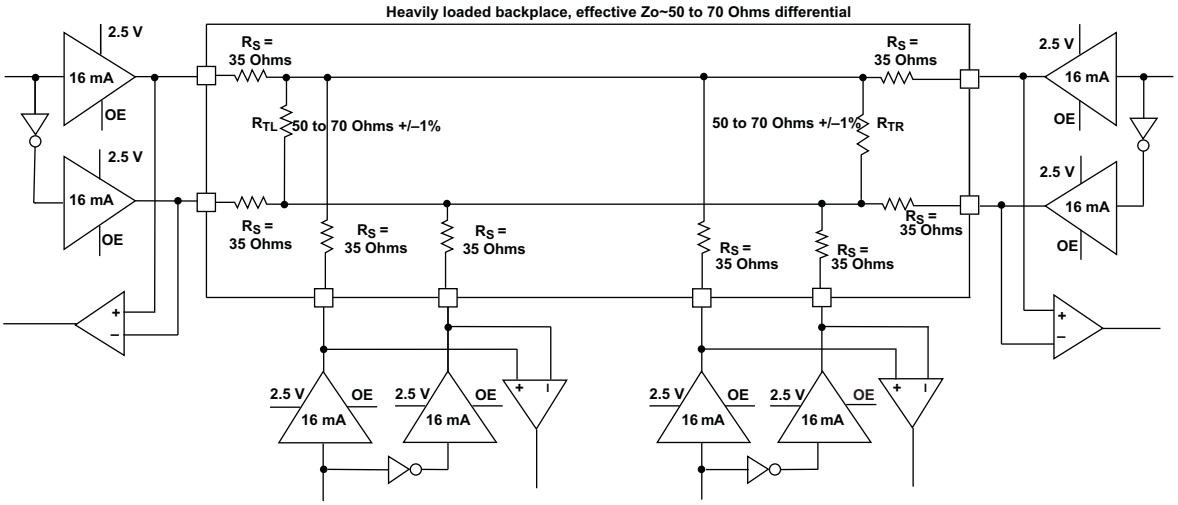


Table 3-5. MLVDS25 DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/–1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/–1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/–1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

Register-to-Register Performance[1, 2, 3]

Function	–8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
3. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond and ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond and ispLEVER design tools can provide logic timing numbers at a particular temperature and voltage.

SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z		–20%	50/75/HiZ	+20%	Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/– 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDO}	Serial data rate		270	—	2975	Mbps
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [1, 2]	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC_V	Duty cycle, video clock		45	50	55	%

Pin Information Summary

Pin Information Summary		ECP3-17EA			ECP3-35EA			ECP3-70EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	20	36	26	42	48	42	60	86
	Bank 1	14	10	24	14	36	36	36	48	78
	Bank 2	6	7	12	6	24	24	24	34	36
	Bank 3	18	12	44	16	54	59	54	59	86
	Bank 6	20	11	44	18	63	61	63	67	86
	Bank 7	19	26	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4	4	8	8
	Bank 3	0	0	0	2	4	4	4	12	12
	Bank 6	0	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310	295	380	490
VCC		6	16	16	6	16	32	16	32	32
VCCAUX		4	5	8	4	8	12	8	12	16
VTT		4	7	4	4	4	4	4	4	8
VCCA		4	6	4	4	4	8	4	8	16
VCCPLL		2	2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	3	2	2	2	4	2	4	4
	Bank 1	2	3	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	2	4	2	4	4
	Bank 3	2	3	2	2	2	4	2	4	4
	Bank 6	2	3	2	2	2	4	2	4	4
	Bank 7	2	3	2	2	2	4	2	4	4
	Bank 8	1	2	2	1	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139	98	139	233
NC		0	0	73	0	0	96	0	0	238
Reserved[1]		0	0	2	0	2	2	2	2	2
SERDES		26	18	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672	484	672	1156

Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software

Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	–6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	–7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	–8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	–6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	–7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	–8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW[1]	1.2 V	–6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW[1]	1.2 V	–7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW[1]	1.2 V	–8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW[1]	1.2 V	–6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW[1]	1.2 V	–7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW[1]	1.2 V	–8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250 V.

Date	Version	Section	Change Summary
March 2010	01.6	Architecture	Added Read-Before-Write information.
		DC and Switching Characteristics	Added footnote #6 to Maximum I/O Buffer Speed table.
			Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table.
		Pinout Information	Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices.
		Ordering Information	Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices.
			Removed dual mark information.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.
			Updated Table 2-13, SERDES Standard Support to include SONET/SDH and updated footnote 2.
		DC and Switching Characterisitcs	Added footnote to ESD Performance table.
			Updated SERDES Power Supply Requirements table and footnotes.
			Updated Maximum I/O Buffer Speed table.
			Updated Pin-to-Pin Peformance table.
			Updated sysCLOCK PLL Timing table.
			Updated DLL timing table.
			Updated High-Speed Data Transmitter tables.
			Updated High-Speed Data Receiver table.
			Updated footnote for Receiver Total Jitter Tolerance Specification table.
			Updated Periodic Receiver Jitter Tolerance Specification table.
			Updated SERDES External Reference Clock Specification table.
			Updated PCI Express Electrical and Timing AC and DC Characteristics.
			Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics.
			Updated SMPTE AC/DC Characteristics Transmit table.
			Updated Mini LVDS table.
			Updated RSDS table.
			Added Supply Current (Standby) table for EA devices.
			Updated Internal Switching Characteristics table.
			Updated Register-to-Register Performance table.
			Added HDMI Electrical and Timing Characteristics data.
			Updated Family Timing Adders table.
			Updated sysCONFIG Port Timing Specifications table.
			Updated Recommended Operating Conditions table.
			Updated Hot Socket Specifications table.
			Updated Single-Ended DC table.
			Updated TRLVDS table and figure.
			Updated Serial Data Input Specifications table.
			Updated HDMI Transmit and Receive table.
		Ordering Information	Added LFE3-150EA “TW” devices and footnotes to the Commercial and Industrial tables.