E: Lattice Semiconductor Corporation - LFE3-95EA-6LFN672C Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-6lfn672c

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Figure 2-8. Clock Divider Connections



Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- 1. **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- 3. **Read-Before-Write (EA devices only)** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP[™] Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.



This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.



Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches

LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice)
- Multiply (36 x 36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic (addition/subtraction of three inputs)
 - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such



as, overflow, underflow and convergent rounding, etc.

- Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-24, the LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2[™] sysDSP block, such that, legacy applications can be targeted to the LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LatticeECP3 sysDSP slices, as shown in Figure 2-25.



Figure 2-24. Simplified sysDSP Slice Block Diagram



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element



To FPGA Core



MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

Figure 2-27. MAC DSP Element









Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysl/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.



Figure 2-34. Output and Tristate Block for Left and Right Edges



Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysl/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

	PIO A	↓	PADA "T"
	PIO B		PADB "C"
	PIO A		PADA "T"
	PIO B	+	PADB "C"
	PIO A		PADA "T"
	PIO B	L+	PADB "C"
_ DQS	PIO A	SysIO Buffer Delay ◀	PADA "T" LVDS Pair
	PIO B		PADB "C"
	PIO A		PADA "T" LVDS Pair
	→ PIO A → PIO B		PADA "T" LVDS Pair PADB "C"
	→ PIO A → PIO B → PIO A		PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
			PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



2. Left and Right (Banks 2, 3, 6 and 7) sysl/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysl/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. Configuration Bank sysl/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysl/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysl/O Standards

The LatticeECP3 sysl/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysl/O buffer to support a variety of standards please see TN1177, LatticeECP3 syslO Usage Guide.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-8		-8 -		6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775		0.775	—	0.775		UI
f _{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices		250		250		250	MHz
Generic DDRX2 Ir Input	Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock								
Left and Right Sic	les								
t _{SUGDDR}	Data Setup Before CLK	ECP3-150EA	321		403		471		ps
t _{HOGDDR}	Data Hold After CLK	ECP3-150EA	321		403	_	471		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	405	—	325	_	280	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	321	_	403	_	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-70EA/95EA	321	_	403	_	535		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	405		325	_	250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-35EA	335	_	425	_	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-35EA	335	—	425	_	535	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	405	_	325	_	250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-17EA	335	_	425	—	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-17EA	335	_	425	_	535		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	405		325		250	MHz
Generic DDRX2 Ir	puts with Clock and Data (>10	Bits Wide) Aligned at Pin	(GDDR)	(2_RX.E	CLK.Alig	ned)			
Left and Right Sid	le Using DLLCLKIN Pin for Clo	ck Input							
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775		0.775		0.775		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA		460	—	385	—	345	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775		0.775	_	0.775		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA		460		385		311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	460		385		311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	_	0.790	—	0.790	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	460	_	385	_	311	MHz
Top Side Using P	CLK Pin for Clock Input								
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA	_	0.225	—	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775		0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	235	_	170	_	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	_	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170		130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	_	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	235		170	_	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790		0.790	_	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA		235		170		130	MHz

Over Recommended Commercial Operating Conditions







Figure 3-7. DDR/DDR2/DDR3 Parameters





LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7} (Continued)

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5 V	-0.07	-0.04	-0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	-0.22	-0.19	-0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.3V	-0.06	-0.06	-0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.3V	-0.01	-0.02	-0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.3V	-0.07	-0.07	-0.08	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.3V	-0.12	-0.13	-0.14	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	-0.06	-0.06	-0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	-0.01	-0.02	-0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	-0.07	-0.07	-0.08	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	-0.05	-0.06	-0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	-0.12	-0.13	-0.14	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	-0.04	-0.03	-0.03	ns

Over Recommended Commercial Operating Conditions



SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

ltem	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmi	t Data Latency ¹				•	•	
	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
T1	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	_	_	2	1	word clk
Т3	SERDES Bridge transmit	—		_	2	1	word clk
тл	Serializer: 8-bit mode		_		15 + Δ1	—	UI + ps
14	Serializer: 10-bit mode	—	_		18 + Δ1	—	UI + ps
TE	Pre-emphasis ON		_		1 + ∆2	—	UI + ps
15	Pre-emphasis OFF	—	—	—	0 + ∆3	—	UI + ps
Receive	Data Latency ²				•		
D1	Equalization ON			_	Δ1	_	UI + ps
	Equalization OFF		_		Δ2	—	UI + ps
D 2	Deserializer: 8-bit mode	—	_	_	10 + ∆3	—	UI + ps
Π <u>Ζ</u>	Deserializer: 10-bit mode	—	—	—	12 + ∆3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
R7	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. $\Delta 1 = -245 \text{ ps}, \Delta 2 = +88 \text{ ps}, \Delta 3 = +112 \text{ ps}.$

2. $\Delta 1 = +118$ ps, $\Delta 2 = +132$ ps, $\Delta 3 = +700$ ps.







Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Тур.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	_	_	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	_	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	_	_	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	_		0.5	UI, p-p

Note: Values are measured with PRBS 2⁷–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.



Figure 3-14. Jitter Transfer – 3.125 Gbps



Figure 3-15. Jitter Transfer – 2.5 Gbps





LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units			
t _{SSCL}	CCLK Minimum Low Pulse	5		ns			
t _{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	_	ns			
t _{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	_	ns			
Master and	Master and Slave SPI (Continued)						
t _{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	_	ns			
t _{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	_	ns			
t _{HLQZ}	HOLDN to Output High-Z	_	9	ns			
t _{HHQX}	HOLDN to Output Low-Z	_	9	ns			

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle





LatticeECP3 Family Data Sheet Pinout Information

March 2015

Data Sheet DS1021

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
	10	[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Column Number. When Edge is L (Left) or R (Right), only need to specify Row Number.
P[Eage] [Row/Column Number]_[A/B]	1/0	[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
P[Edge][Row Number]E_[A/B/C/D]	I	These general purpose signals are input-only pins and are located near the PLLs.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V _{CC}		Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	_	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCIOx}		Dedicated power supply pins for I/O bank x.
V _{CCA}	_	SERDES, transmit, receive, PLL and reference clock buffer power supply. All V_{CCA} supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect V_{CCA} to V_{CC} .
V _{CCPLL_[LOC]}	—	General purpose PLL supply pins where LOC=L (left) or R (right).
V _{REF1_x} , V _{REF2_x}	_	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
VTTx	—	Power supply for on-chip termination of I/Os.
XRES ¹		10 kOhm +/-1% resistor must be connected between this pad and ground.
PLL, DLL and Clock Functions		
[LOC][num]_GPLL[T, C]_IN_[index]	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, $T =$ true and C = complement, index A,B,Cat each side.
[LOC][num]_GPLL[T, C]_FB_[index]	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, $T =$ true and C = complement, index A,B,Cat each side.
[LOC]0_GDLLT_IN_[index] ²	I/O	General Purpose DLL (GDLL) input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
[LOC]0_GDLLT_FB_[index] ²	I/O	Optional feedback GDLL input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
PCLK[T, C][n:0]_[3:0] ²	I/O	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.

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LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Date	Version	Section	Change Summary
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modi- fied corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characteristics	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before- Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{\text{DIBGDDR}},t_{\text{W}_\text{PRI}},t_{\text{W}_\text{EDGE}}$ and $t_{\text{SKEW}_\text{EDGE}_\text{DQS}}.$
			LatticeECP3 Internal Switching Characteristics table - updated data for $t_{\mbox{COO_PIO}}$ and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f _{OUT} .
			External Reference Clock Specification (refclkp/refclkn) table - updated data for $V_{REF\text{-IN-SE}}$ and $V_{REF\text{-IN-DIFF}}$
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for $\ensuremath{t_{\text{MWC}}}$.
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
August 2009	01.3	DC and Switching Characteristics	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
July 2009	01.2	Multiple	Changed references of "multi-boot" to "dual-boot" throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characteristics	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bul- leted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.