# E. Lattice Semiconductor Corporation - <u>LFE3-95EA-7FN1156C Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-7fn1156c

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# LatticeECP3 Family Data Sheet Architecture

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Data Sheet DS1021

## **Architecture Overview**

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM<sup>™</sup> Embedded Block RAM (EBR) and rows of sys-DSP<sup>™</sup> Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG<sup>™</sup> port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

## **PFU Blocks**

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



### **Edge Clock Sources**

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.





Notes:

1. Clock inputs can be configured in differential or single ended mode.

2. The two DLLs can also drive the two top edge clocks.

3. The top left and top right PLL can also drive the two top edge clocks.

## Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.



#### Figure 2-20. Sources of Edge Clock (Left and Right Edges)



Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.



#### Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- 1. **Normal** Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- 3. **Read-Before-Write (EA devices only)** When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

#### Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

#### Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

## sysDSP<sup>™</sup> Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.



as, overflow, underflow and convergent rounding, etc.

- Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-24, the LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2<sup>™</sup> sysDSP block, such that, legacy applications can be targeted to the LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LatticeECP3 sysDSP slices, as shown in Figure 2-25.



Figure 2-24. Simplified sysDSP Slice Block Diagram



#### Figure 2-25. Detailed sysDSP Slice Diagram



Note: A\_ALU, B\_ALU and C\_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	<b>1</b> <sup>1</sup>	1/2	_

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.



#### Figure 2-37. DQS Local Bus



## **Polarity Control Logic**

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

### DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.



# LatticeECP3 Supply Current (Standby)<sup>1, 2, 3, 4, 5, 6</sup>

			Тур	Typical	
Symbol	Parameter	Device	-6L, -7L, -8L	-6, -7, -8	Units
		ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
I <sub>CC</sub>	Core Power Supply Current	ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
		ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply Current	ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
		ECP-17EA	0.0	0.0	mA
	PLL Power Supply Current (Per PLL)	ECP3-35EA	0.1	0.1	mA
I <sub>CCPLL</sub>		ECP3-70EA	0.1	0.1	mA
ICCPLL		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
		ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
I <sub>CCIO</sub>	Bank Power Supply Current (Per Bank)	ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I <sub>CCJ</sub>	JTAG Power Supply Current	All Devices	2.5	2.5	mA
		ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
I <sub>CCA</sub>	Iransmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

## **Over Recommended Operating Conditions**

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the  $V_{\mbox{CCIO}}$  or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5.  $T_J = 85$  °C, power supplies at nominal voltage.

6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.



## **Typical Building Block Function Performance**

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)<sup>1, 2, 3</sup>

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

## Register-to-Register Performance<sup>1, 2, 3</sup>

Function	–8 Timing	Units							
Basic Functions									
16-bit Decoder	500	MHz							
32-bit Decoder	500	MHz							
64-bit Decoder	500	MHz							
4:1 MUX	500	MHz							
8:1 MUX	500	MHz							
16:1 MUX	500	MHz							
32:1 MUX	445	MHz							
8-bit adder	500	MHz							
16-bit adder	500	MHz							
64-bit adder	305	MHz							
16-bit counter	500	MHz							
32-bit counter	460	MHz							
64-bit counter	320	MHz							
64-bit accumulator	315	MHz							
Embedded Memory Functions									
512x36 Single Port RAM, EBR Output Registers	340	MHz							
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz							
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	130	MHz							
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz							
Distributed Memory Functions									
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz							
32x4 Pseudo-Dual Port RAM	500	MHz							
64x8 Pseudo-Dual Port RAM	400	MHz							
DSP Function									
18x18 Multiplier (All Registers)	400	MHz							
9x9 Multiplier (All Registers)	400	MHz							
36x36 Multiply (All Registers)	260	MHz							



# LatticeECP3 External Switching Characteristics (Continued)<sup>1, 2, 3, 13</sup>

			-8 -7		_	-6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.7	—	0.8	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.6	—	1.8	_	2.0	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	ECP3-35EA	_	3.2	—	3.4	—	3.6	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.6	_	0.7	_	0.8	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-35EA	0.3	—	0.3	—	0.4	-	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.6	_	1.7	_	1.8	_	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	_	0.0	_	0.0	_	ns
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	ECP3-17EA	_	3.0	—	3.3	—	3.5	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.6	_	0.7	_	0.8	—	ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	ECP3-17EA	0.3	_	0.3	_	0.4	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.6	—	1.7	—	1.8	—	ns
t <sub>H_DELPLL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	_	0.0	_	0.0	—	ns
Generic DDR <sup>12</sup>									
Generic DDRX1 In Input	puts with Clock and Data (>10 Bits	Wide) Centered at Pi	n (GDDF	RX1_RX.S	SCLK.Ce	ntered) L	Ising PC	LK Pin fo	or Clock
t <sub>SUGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	480	—	480	_	480		ps
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	480	—	480	—	480		ps
f <sub>MAX_GDDR</sub>	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.SC	CLK.PLL	Aligned)	Using P	LLCLKIN	Pin for
Data Left, Right, a	nd Top Sides and Clock Left and F	Right Sides							
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	_	0.225		0.225		0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	_	UI
f <sub>MAX GDDR</sub>	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.S0	CLK.Alig	ned) Usiı	ng DLL -	CLKIN P	in for
Data Left, Right ar	d Top Sides and Clock Left and R	ight Sides							
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	_	0.225	—	0.225	—	0.225	UI
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775		UI
f <sub>MAX GDDR</sub>	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In Input	puts with Clock and Data (<10 Bits	Wide) Centered at Pi	n (GDDF	X1_RX.	DQS.Cen	tered) U	sing DQ	S Pin for	Clock
t <sub>SUGDDB</sub>	Data Setup After CLK	All ECP3EA Devices	535	_	535		535		ps
tHOGDDR	Data Hold After CLK	All ECP3EA Devices	535	—	535		535	_	ps
f <sub>MAX GDDB</sub>	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In	puts with Clock and Data (<10bits	wide) Aligned at Pin (	GDDRX	1_RX.DQ	S.Aligne	d) Using	DQS Pin	for Cloc	k Input
Data and Clock Le	ft and Right Sides	· - · ·			-				-
t <sub>DVACI KGDDB</sub>	Data Setup Before CLK	All ECP3EA Devices	—	0.225	_	0.225		0.225	UI
STROLIGED									

## **Over Recommended Commercial Operating Conditions**



# LatticeECP3 External Switching Characteristics (Continued)<sup>1, 2, 3, 13</sup>

			-	-8	-	-7	-	-6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units		
Generic DDRX2 In	puts with Clock and Data (>10bits	s wide) are Aligned at I	Pin (GDD	RX2_RX	.ECLK.A	ligned)	1				
Left and Right Side	es Using DLLCLKPIN for Clock Ir			0.005	1	0.005	1	0.005			
<sup>t</sup> DVACLKGDDR	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225			
	Data Hold After CLK	ECP3-150EA	0.775	-	0.775		0.775				
<sup>T</sup> MAX_GDDR	DDRX2 Clock Frequency	ECP3-150EA	_	460	_	385	_	345	MHZ		
<sup>t</sup> DVACLKGDDR	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI		
<sup>t</sup> DVECLKGDDR	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775		0.775	—	UI		
fMAX_GDDR	DDRX2 Clock Frequency	ECP3-70EA/95EA		460		385		311	MHZ		
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	ECP3-35EA	_	0.210	—	0.210	—	0.210	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790		0.790	—	0.790	_	UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-35EA	_	460	_	385	_	311	MHz		
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK (Left and Right Sides)	ECP3-17EA	_	0.210	_	0.210		0.210	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	—	UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-17EA		460		385		311	MHz		
Top Side Using PC	LK Pin for Clock Input										
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	ECP3-150EA		0.225		0.225		0.225	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-150EA	0.775	—	0.775	—	0.775	_	UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-150EA	_	235	—	170		130	MHz		
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	_	0.225	_	0.225	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-70EA/95EA	0.775	—	0.775	—	0.775	_	UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	235		170	—	130	MHz		
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	ECP3-35EA	_	0.210		0.210		0.210	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-35EA	0.790	—	0.790	—	0.790		UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-35EA		235		170		130	MHz		
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	ECP3-17EA		0.210		0.210		0.210	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	ECP3-17EA	0.790	—	0.790		0.790		UI		
f <sub>MAX_GDDR</sub>	DDRX2 Clock Frequency	ECP3-17EA	_	235		170		130	MHz		
Generic DDRX2 In Input	puts with Clock and Data (<10 Bit	ts Wide) Centered at P	in (GDDF	RX2_RX.I	DQS.Cen	tered) U	sing DQ	S Pin for	Clock		
Left and Right Side	es										
t <sub>SUGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	330	_	330		352		ps		
t <sub>HOGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	330	—	330	—	352	_	ps		
f <sub>MAX GDDR</sub>	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	_	375	MHz		
Generic DDRX2 In	puts with Clock and Data (<10 Bit	ts Wide) Aligned at Pin	(GDDR)	(2_RX.D0	QS.Align	ed) Using	g DQS Pi	n for Clo	ck Input		
Left and Right Side	es										
t <sub>DVACLKGDDR</sub>	Data Setup Before CLK	All ECP3EA Devices	_	0.225	_	0.225	—	0.225	UI		
t <sub>DVECLKGDDR</sub>	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	_	0.775	_	UI		
f <sub>MAX GDDR</sub>	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz		
Generic DDRX1 O	utput with Clock and Data (>10 B	its Wide) Centered at P	in (GDD	RX1_TX.	SCLK.Ce	ntered)10	)				
t <sub>DVBGDDR</sub>	Data Valid Before CLK	ECP3-150EA	670	—	670		670		ps		
t <sub>DVAGDDR</sub>	Data Valid After CLK	ECP3-150EA	670	<b>—</b>	670	<b>—</b>	670	<b>—</b>	ps		
f <sub>MAX</sub> GDDR	DDRX1 Clock Frequency	ECP3-150EA	—	250	—	250	—	250	MHz		
	Data Valid Before CLK	ECP3-70EA/95EA	666	—	665		664	—	ps		
	Data Valid After CLK	ECP3-70EA/95EA	666		665		664		ps		
BIAGDDIT	1	1		I		l			· ·		

## Over Recommended Commercial Operating Conditions



# LatticeECP3 Internal Switching Characteristics<sup>1, 2, 5</sup> (Continued)

		_	8	-7		-6		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory	0.141		0.145		0.149		ns
t <sub>SUCE_EBR</sub>	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t <sub>HCE_EBR</sub>	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t <sub>SUBE_EBR</sub>	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t <sub>HBE_EBR</sub>	Byte Enable Hold Time to EBR Output Register	0.118	_	0.098	_	0.077	_	ns
DSP Block Tin	ning <sup>3</sup>							
t <sub>SUI_DSP</sub>	Input Register Setup Time	0.32	_	0.36	_	0.39	_	ns
t <sub>HI_DSP</sub>	Input Register Hold Time	-0.17	_	-0.19	_	-0.21	_	ns
t <sub>SUP_DSP</sub>	Pipeline Register Setup Time	2.23	_	2.30	_	2.37	_	ns
t <sub>HP_DSP</sub>	Pipeline Register Hold Time	-1.02	_	-1.09	_	-1.15	_	ns
t <sub>SUO_DSP</sub>	Output Register Setup Time	3.09	_	3.22	_	3.34	_	ns
t <sub>HO_DSP</sub>	Output Register Hold Time	-1.67	_	-1.76	_	-1.84	_	ns
t <sub>COI_DSP</sub>	Input Register Clock to Output Time	_	3.05	_	3.35	_	3.73	ns
t <sub>COP_DSP</sub>	Pipeline Register Clock to Output Time	_	1.30	_	1.47	_	1.64	ns
t <sub>COO_DSP</sub>	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t <sub>SUOPT_DSP</sub>	Opcode Register Setup Time	0.31	_	0.35	_	0.39	_	ns
t <sub>HOPT_DSP</sub>	Opcode Register Hold Time	-0.20	_	-0.24		-0.27	_	ns
t <sub>SUDATA_DSP</sub>	Cascade_data through ALU to Output Register Setup Time	1.69		1.94		2.14		ns
t <sub>HPDATA_DSP</sub>	Cascade_data through ALU to Output Register Hold Time	-0.58		-0.80		-0.97		ns

### **Over Recommended Commercial Operating Conditions**

1. Internal parameters are characterized but not tested on every device.

2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. DSP slice is configured in Multiply Add/Sub 18 x 18 mode.

4. The output register is in Flip-flop mode.

5. For details on –9 speed grade devices, please contact your Lattice Sales Representative.



## sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2		500	MHz
'IN	CLKFB)		Primary clock <sup>4</sup>	2		420	MHz
f	Output clock frequency (CLKOP,		Edge clock	4	_	500	MHz
OUT	CLKOS)		Primary clock <sup>4</sup>	4	_	420	MHz
f <sub>OUT1</sub>	K-Divider output frequency	CLKOK		0.03125	_	250	MHz
f <sub>OUT2</sub>	K2-Divider output frequency	CLKOK2		0.667	_	166	MHz
f <sub>VCO</sub>	PLL VCO frequency			500	_	1000	MHz
f <sub>PFD</sub> <sup>3</sup>	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock <sup>4</sup>	2	_	420	MHz
AC Charac	teristics					-	
t <sub>PA</sub>	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t <sub>DT</sub>	CLKOS at 50% setting)	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f <sub>OUT</sub> > 250 MHz	Primary clock	30	50	70	%
t <sub>CPA</sub>	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t <sub>OPW</sub>	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
		$f_{OUT} \ge 420 \text{ MHz}$		—	_	200	ps
t <sub>OPJIT</sub> 1	Output clock period jitter	420 MHz > $f_{OUT} \ge 100$ MHz		_	_	250	ps
		f <sub>OUT</sub> < 100 MHz		—	_	0.025	UIPP
t <sub>SK</sub>	Input clock to output clock skew when N/M = integer			_		500	ps
+ 2	Look time	2 to 25 MHz		—	_	200	us
LOCK		25 to 500 MHz		—		50	us
t <sub>UNLOCK</sub>	Reset to PLL unlock time to ensure fast reset			_		50	ns
t <sub>HI</sub>	Input clock high time	90% to 90%		0.5	_	—	ns
t <sub>LO</sub>	Input clock low time	10% to 10%		0.5	_	—	ns
t <sub>IPJIT</sub>	Input clock period jitter			—	_	400	ps
+	Reset signal pulse width high, RSTK			10	_	_	ns
'RST	Reset signal pulse width high, RST			500	_	_	ns

#### **Over Recommended Operating Conditions**

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for  $f_{PFD} > 4$  MHz. For  $f_{PFD} < 4$  MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for  $f_{PFD} < 4$  MHz.

4. When using internal feedback, maximum can be up to 500 MHz.



#### Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2<sup>7</sup>-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



#### Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Тур.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	_	_	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	_	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	_	_	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	_		0.5	UI, p-p

Note: Values are measured with PRBS 2<sup>7</sup>–1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.



### SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F <sub>REF</sub>	Frequency range	15	_	320	MHz
F <sub>REF-PPM</sub>	Frequency tolerance <sup>1</sup>	-1000	_	1000	ppm
V <sub>REF-IN-SE</sub>	Input swing, single-ended clock <sup>2</sup>	200	_	V <sub>CCA</sub>	mV, p-p
V <sub>REF-IN-DIFF</sub>	Input swing, differential clock	200	_	2*V <sub>CCA</sub>	mV, p-p differential
V <sub>REF-IN</sub>	Input levels	0	_	V <sub>CCA</sub> + 0.3	V
D <sub>REF</sub>	Duty cycle <sup>3</sup>	40	_	60	%
T <sub>REF-R</sub>	Rise time (20% to 80%)	200	500	1000	ps
T <sub>REF-F</sub>	Fall time (80% to 20%)	200	500	1000	ps
Z <sub>REF-IN-TERM-DIFF</sub>	Differential input termination	-20%	100/2K	+20%	Ohms
C <sub>REF-IN-CAP</sub>	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL\_LOL\_SET and CDR\_LOL\_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

#### Figure 3-13. SERDES External Reference Clock Waveforms





#### Figure 3-14. Jitter Transfer – 3.125 Gbps



Figure 3-15. Jitter Transfer – 2.5 Gbps





## sysl/O Differential Electrical Characteristics

## Transition Reduced LVDS (TRLVDS DC Specification)

#### **Over Recommended Operating Conditions**

Symbol	Description	Min.	Nom.	Max.	Units
V <sub>CCO</sub>	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V <sub>ID</sub>	Input differential voltage	150	_	1200	mV
V <sub>ICM</sub>	Input common mode voltage	3	_	3.265	V
V <sub>CCO</sub>	Termination supply voltage	3.14	3.3	3.47	V
R <sub>T</sub>	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



### Mini LVDS

#### **Over Recommended Operating Conditions**

Parameter Symbol	Description	Min.	Тур.	Max.	Units
Z <sub>O</sub>	Single-ended PCB trace impedance	30	50	75	Ohms
R <sub>T</sub>	Differential termination resistance	50	100	150	Ohms
V <sub>OD</sub>	Output voltage, differential,  V <sub>OP</sub> - V <sub>OM</sub>	300	_	600	mV
V <sub>OS</sub>	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
$\Delta V_{OD}$	Change in V <sub>OD</sub> , between H and L	—	_	50	mV
$\Delta V_{ID}$	Change in $V_{OS}$ , between H and L	—	_	50	mV
V <sub>THD</sub>	Input voltage, differential,  V <sub>INP</sub> - V <sub>INM</sub>	200	_	600	mV
V <sub>CM</sub>	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	0.3+(V <sub>THD</sub> /2)	_	2.1-(V <sub>THD</sub> /2)	
T <sub>R</sub> , T <sub>F</sub>	Output rise and fall times, 20% to 80%	—	_	550	ps
T <sub>ODUTY</sub>	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.



## LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package <sup>1</sup>	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade <sup>1</sup>	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.