E.J. Lattice Semiconductor Corporation - <u>LFE3-95EA-7FN484C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-7fn484c

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Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM



ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.



The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.



Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sys-DSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding



Input signals are fed from the sysl/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-30 provides further information on the use of the gearbox function.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-37 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.



Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)



Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143 ¹ , 177 ¹ , 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3 ²	155.52	x1	N/A
SONET-STS-12 ²	622.08	x1	N/A
SONET-STS-48 ²	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.

2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.



MCCLK (MHz)	MCCLK (MHz)
	10
2.5 ¹	13
4.3	15 ²
5.4	20
6.9	26
8.1	33 ³
9.2	

 Table 2-16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.

2. Maximum MCCLK with encryption enabled.

3. Maximum MCCLK without encryption.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the LatticeECP3 Pin Migration Tables and Diamond software for specific restrictions and limitations.



DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
$I_{\rm IL}, I_{\rm IH}^{1, 4}$	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2 \text{ V})$	—	_	10	μΑ
I _{IH} ^{1, 3}	Input or I/O High Leakage	$(V_{CCIO} - 0.2 \text{ V}) < V_{IN} \leq 3.6 \text{ V}$	—	_	150	μΑ
I _{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7 V_{CCIO}$	-30	—	-210	μΑ
I _{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{CCIO}$	30	—	210	μΑ
I _{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	_	—	μΑ
I _{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μΑ
I _{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	_	—	210	μΑ
I _{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	-210	μΑ
V _{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance ²		_	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	_	5	7	pf

Over Recommended Operating Conditions

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25 °C, f = 1.0 MHz.

3. Applicable to general purpose I/Os in top and bottom banks. 4. When used as V_{REF} maximum leakage= 25 μ A.



sysI/O Differential Electrical Characteristics LVDS25

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} ¹ , V _{INM} ¹	Input Voltage		0	_	2.4	V
V _{CM} ¹	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	_	mV
I _{IN}	Input Current	Power On or Power Off		_	+/-10	μΑ
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm		1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9 V	1.03	_	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L		_	_	50	mV
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

1, On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.



Register-to-Register Performance^{1, 2, 3}

Function	–8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

3. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond and ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond and ispLEVER design tools can provide logic timing numbers at a particular temperature and voltage.



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7}

Buffer Type	Description	-8	-7	-6	Units		
Input Adjusters							
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns		
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	-0.04	ns		
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns		
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns		
RSDS25	RSDS, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns		
PPLVDS	Point-to-Point LVDS	0.03	-0.01	-0.03	ns		
TRLVDS	Transition-Reduced LVDS	0.03	0.00	-0.04	ns		
Mini MLVDS	Mini LVDS	0.03	-0.01	-0.03	ns		
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns		
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns		
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns		
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns		
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns		
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns		
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns		
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns		
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns		
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns		
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns		
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns		
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns		
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns		
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns		
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns		
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns		
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns		
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns		
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns		
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns		
LVTTL33	LVTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns		
LVCMOS33	LVCMOS, VCCIO = 3.3 V	0.07	0.07	0.07	ns		
LVCMOS25	LVCMOS, VCCIO = 2.5 V	0.00	0.00	0.00	ns		
LVCMOS18	LVCMOS, VCCIO = 1.8 V	-0.13	-0.13	-0.13	ns		
LVCMOS15	LVCMOS, VCCIO = 1.5 V	-0.07	-0.07	-0.07	ns		
LVCMOS12	LVCMOS, VCCIO = 1.2 V	-0.20	-0.19	-0.19	ns		
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns		
Output Adjusters							
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns		
LVDS25	LVDS, VCCIO = 2.5 V	-0.11	-0.07	-0.03	ns		
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns		
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns		

Over Recommended Commercial Operating Conditions



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F _{REF}	Frequency range	15	_	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	_	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ²	200	_	V _{CCA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	_	2*V _{CCA}	mV, p-p differential
V _{REF-IN}	Input levels	0	_	V _{CCA} + 0.3	V
D _{REF}	Duty cycle ³	40	_	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-20%	100/2K	+20%	Ohms
C _{REF-IN-CAP}	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms





SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDO}	Serial data rate		270	—	2975	Mbps
T _{JALIGNMENT} ²	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ²	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
T _{JALIGNMENT} ^{1, 2}	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
T _{JTIMING}	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
T _{JTIMING}	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
T _{JTIMING}	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

 Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used. The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.

2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.

3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 Ohm impedance differential signal from the Lattice SERDES device.

4. The cable driver drives: RL=75 Ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kOhm 1%.

Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
BR _{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER		_	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
F _{VCLK}	Video output clock frequency		27	-	74.25	MHz
DCV	Duty cycle, video clock		45	50	55	%



LatticeECP3 sysCONFIG Port Timing Specifications

Parameter	Description		Min.	Max.	Units
POR, Confi	guration Initialization, and Wakeup				1
	Time from the Application of V_{CC} , V_{CCAUX} or V_{CCIO8}^{*} (Whichever	Master mode		23	ms
t _{ICFG}	is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Slave mode	—	6	ms
t _{VMC}	Time from t _{ICFG} to the Valid Master MCLK		—	5	μs
t _{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low		_	37	ns
t _{DINIT} 1	PROGRAMN High to INITN High Delay	—	1	ms	
t _{MWC}	Additional Wake Master Clock Signals After DONE Pin is High	100	500	cycles	
t _{CZ}	MCLK From Active To Low To High-Z	—	300	ns	
t _{IODISS}	User I/O Disable from PROGRAMN Low		100	ns	
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequer	nce		100	ns
All Configu	ration Modes				
t _{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t _{HCDI}	Data Hold Time to CCLK/MCLK	1	—	ns	
t _{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Seria	l				1
t _{SSCH}	CCLK Minimum High Pulse	5	—	ns	
t _{SSCL}	CCLK Minimum Low Pulse	5	_	ns	
	Without encryption			33	MHz
ICCLK	CCLK Frequency	With encryption		20	MHz
Master and	Slave Parallel	1			
t _{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t _{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t _{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	_	ns
t _{HWD}	WRITEN Hold Time to CCLK/MCLK		1	_	ns
t _{DCB}	CCLK/MCLK to BUSY Delay Time		_	12	ns
t _{CORD}	CCLK to Out for Read Data		_	12	ns
t _{BSCH}	CCLK Minimum High Pulse		6	_	ns
t _{BSCL}	CCLK Minimum Low Pulse		6	_	ns
t _{BSCYC}	Byte Slave Cycle Time		30	—	ns
		Without encryption		33	MHz
[†] CCLK	CCLK/MCLK Frequency	With encryption		20	MHz
Master and	Slave SPI			1	1
t _{CFGX}	INITN High to MCLK Low			80	ns
t _{CSSPI}	INITN High to CSSPIN Low	0.2	2	μs	
t _{SOCDO}	MCLK Low to Output Valid		15	ns	
t _{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		μs
,		Without encryption		33	MHz
[†] CCLK	CCLK Frequency	With encryption		20	MHz
t _{SSCH}	CCLK Minimum High Pulse				ns

Over Recommended Operating Conditions



Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Тур.	Max.	Units
Output driver supply $(1/-5\%)$	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
V _{OD}	Output voltage, differential, R _T = 100 Ohms	100	200	600	mV
V _{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I _{RSDS}	Differential driver output current	1	2	6	mA
V _{THD}	Input voltage differential	100	—	-	mV
V _{CM}	Input common mode voltage	0.3	—	1.5	V
T _R , T _F	Output rise and fall times, 20% to 80%	—	500		ps
T _{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW1	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW1	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250 V.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.



Date	Version	Section	Change Summary
March 2010	01.6	Architecture	Added Read-Before-Write information.
		DC and Switching Characteristics	Added footnote #6 to Maximum I/O Buffer Speed table.
			Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table.
		Pinout Information	Added pin information for the LatticeECP3-70EA and LatticeECP3- 95EA devices.
		Ordering Information	Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices.
			Removed dual mark information.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.
			Updated Table 2-13, SERDES Standard Support to include SONET/ SDH and updated footnote 2.
		DC and Switching Characterisitcs	Added footnote to ESD Performance table.
			Updated SERDES Power Supply Requirements table and footnotes.
			Updated Maximum I/O Buffer Speed table.
			Updated Pin-to-Pin Peformance table.
			Updated sysCLOCK PLL Timing table.
			Updated DLL timing table.
			Updated High-Speed Data Transmitter tables.
			Updated High-Speed Data Receiver table.
			Updated footnote for Receiver Total Jitter Tolerance Specification table.
			Updated Periodic Receiver Jitter Tolerance Specification table.
			Updated SERDES External Reference Clock Specification table.
			Updated PCI Express Electrical and Timing AC and DC Characteristics.
			Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics.
			Updated SMPTE AC/DC Characteristics Transmit table.
			Updated Mini LVDS table.
			Updated RSDS table.
			Added Supply Current (Standby) table for EA devices.
			Updated Internal Switching Characteristics table.
			Updated Register-to-Register Performance table.
			Added HDMI Electrical and Timing Characteristics data.
			Updated Family Timing Adders table.
			Updated sysCONFIG Port Timing Specifications table.
			Updated Recommended Operating Conditions table.
			Updated Hot Socket Specifications table.
			Updated Single-Ended DC table.
			Updated TRLVDS table and figure.
			Updated Serial Data Input Specifications table.
			Updated HDMI Transmit and Receive table.
		Ordering Information	Added LFE3-150EA "TW" devices and footnotes to the Commercial and Industrial tables.