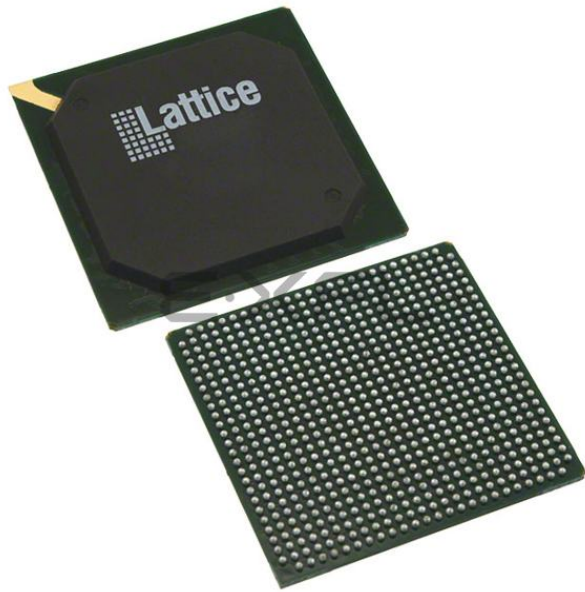




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

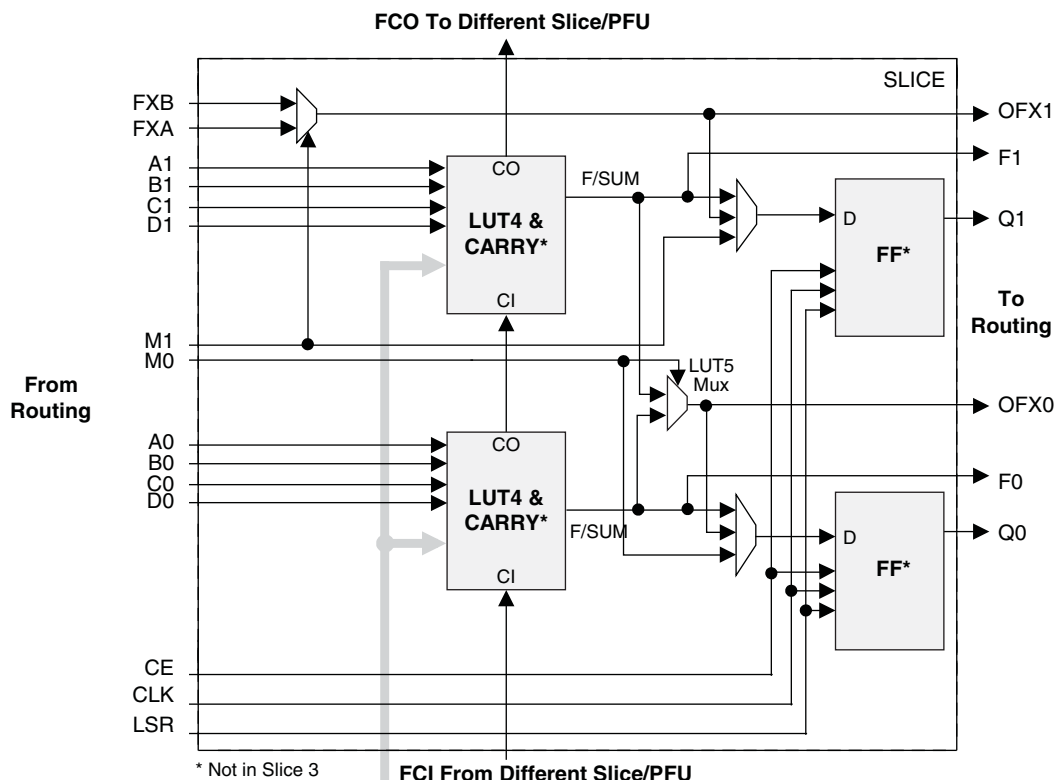
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-7fn672i

Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

WCK is CLK

WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2

WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, [LatticeECP3 Memory Usage Guide](#).

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond and ispLEVER design software tool suites take the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LatticeECP3 family support two to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

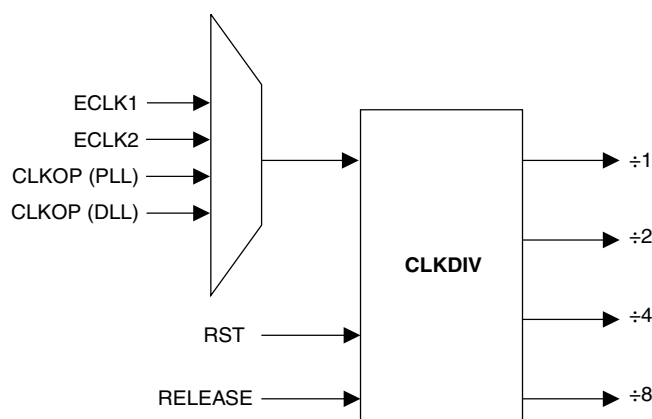
Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-8. Clock Divider Connections



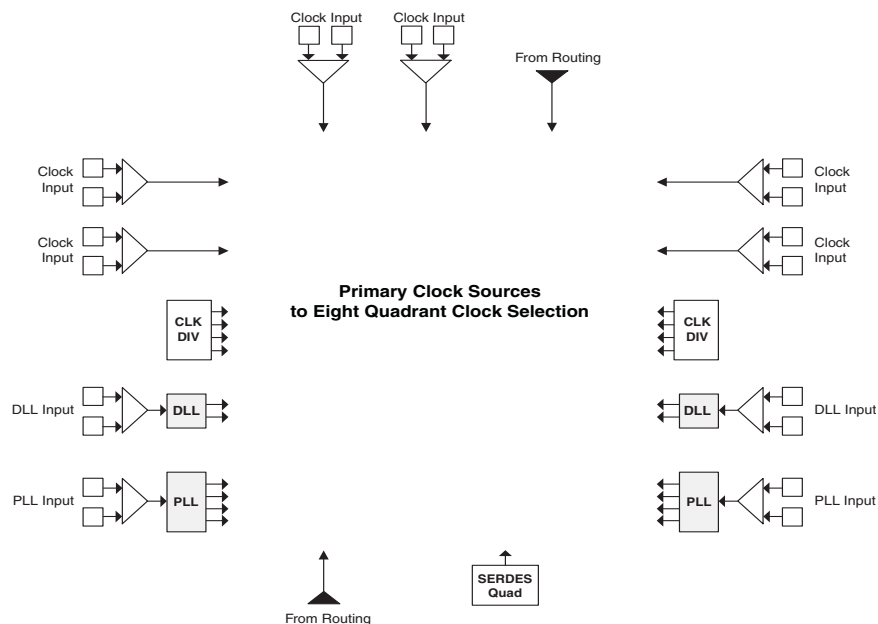
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

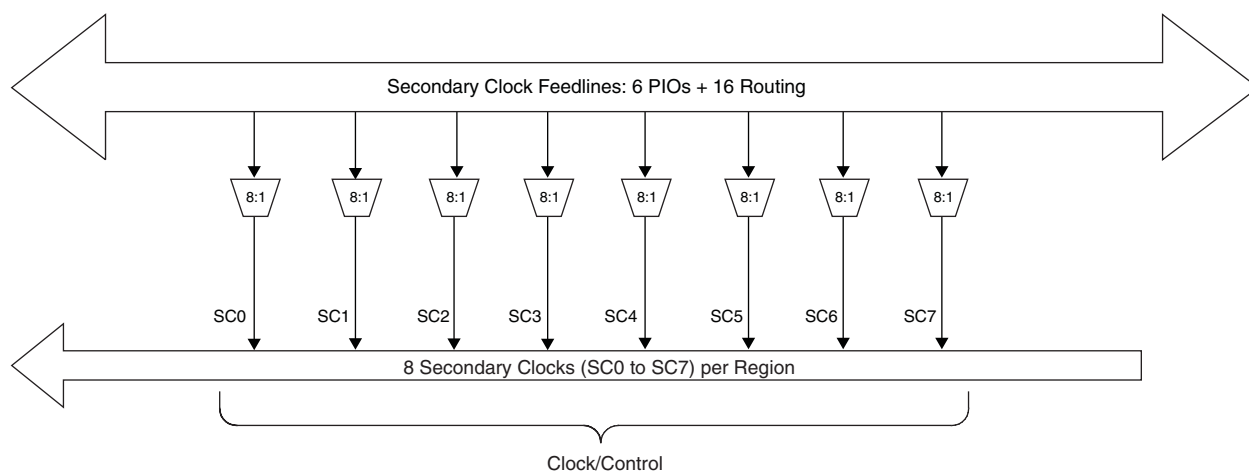
LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

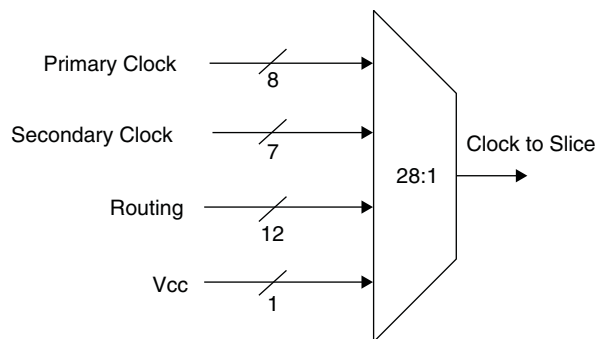


Figure 2-18. Slice0 through Slice2 Control Selection

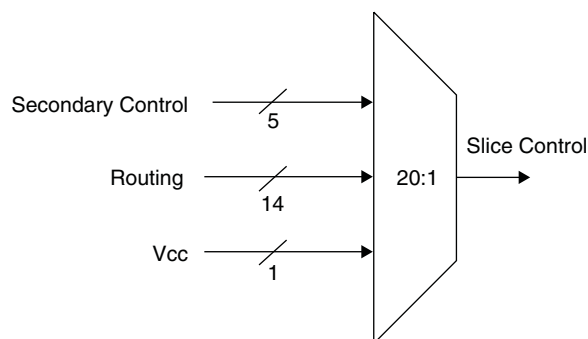


Figure 2-20. Sources of Edge Clock (Left and Right Edges)

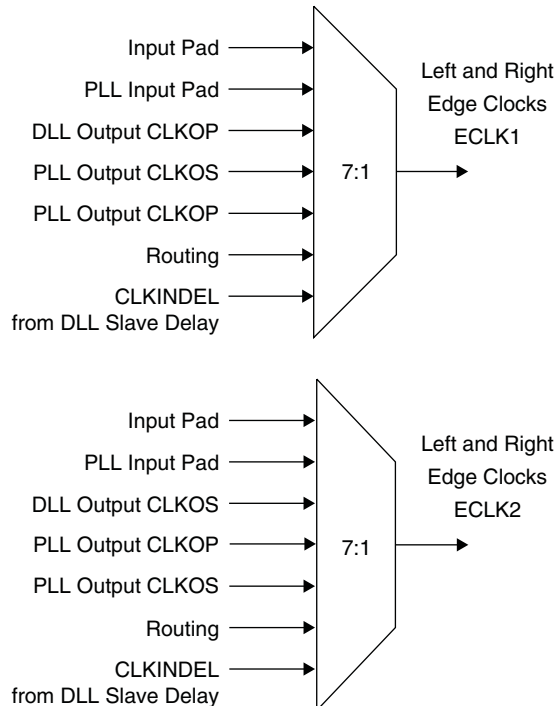
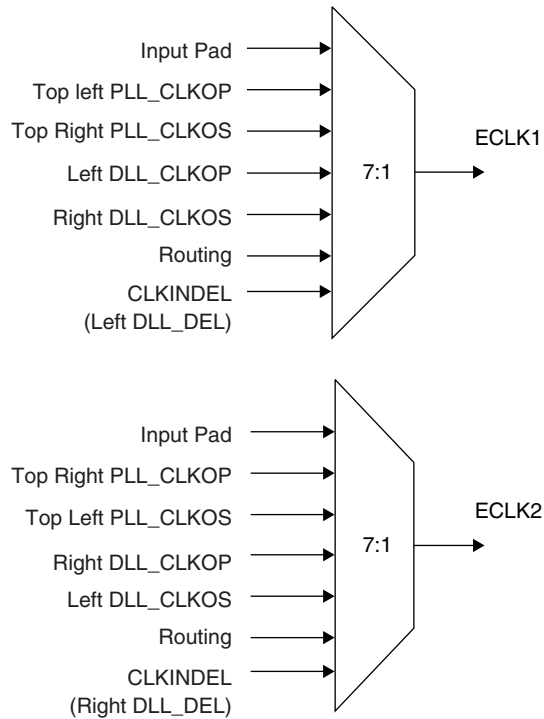


Figure 2-21. Sources of Edge Clock (Top Edge)



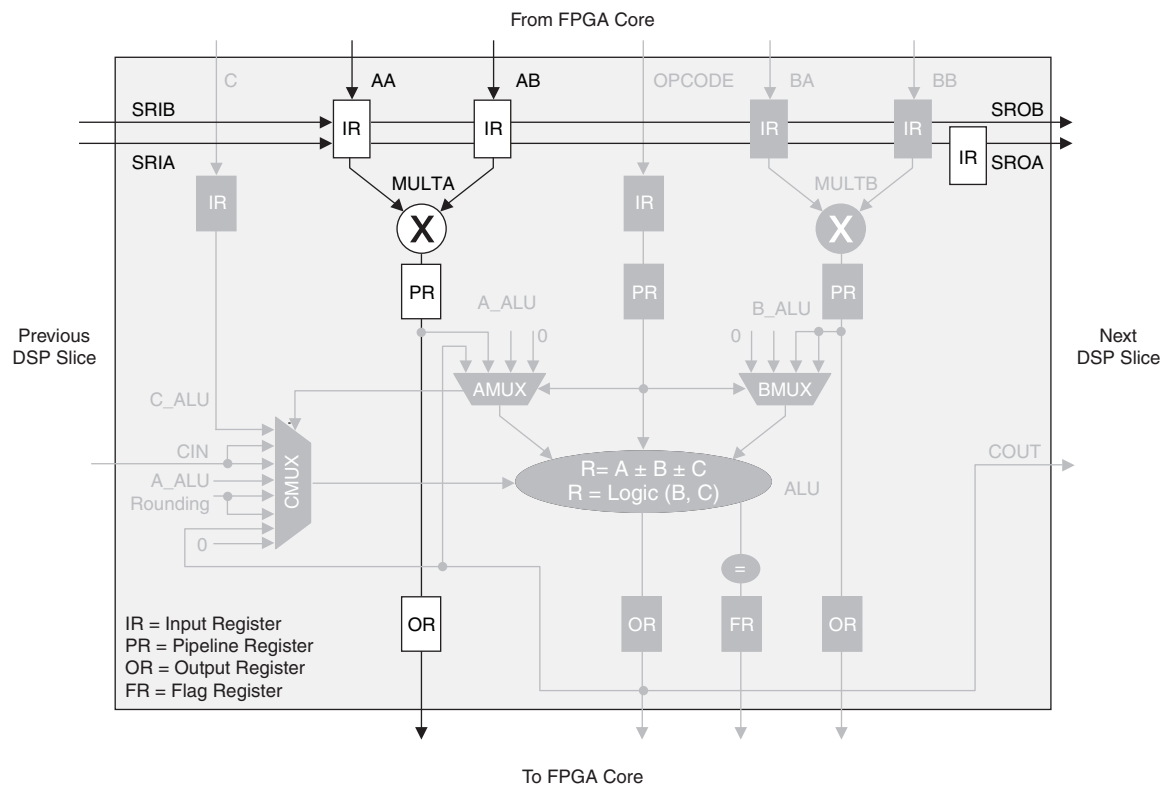
The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

For further information, please refer to TN1182, [LatticeECP3 sysDSP Usage Guide](#).

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

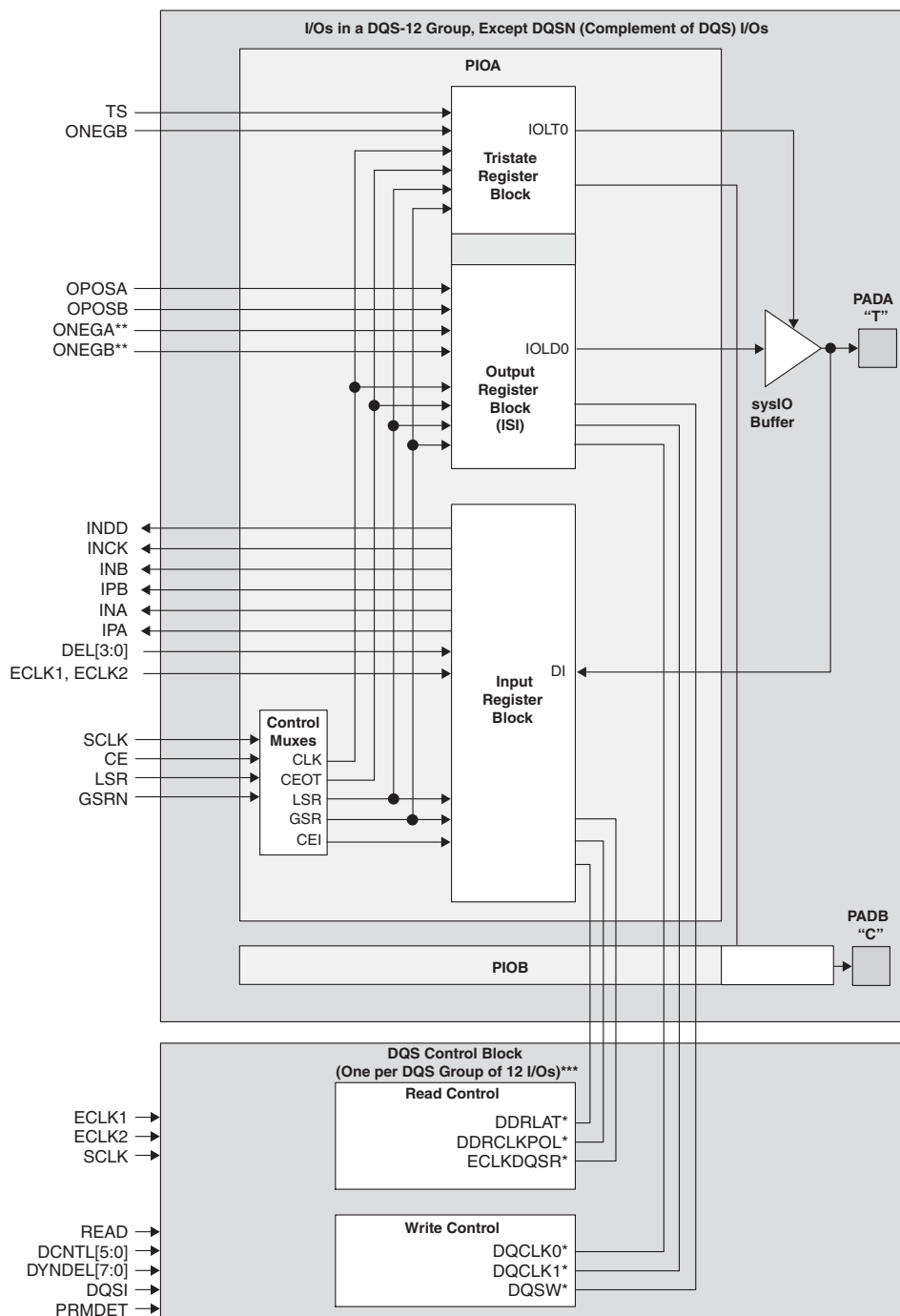
Figure 2-26. MULT sysDSP Element



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.

** Signals are available on the left and right sides only

*** Selected PIO.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-32. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

Table 2-11. PIO Signal List

Name	Type	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA ¹ , OPOSB, ONEGB ¹	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR ¹	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL ¹	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT ¹	Read Control	Used to guarantee INDDR2 gearing by selectively enabling a D-Flip-Flop in datapath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 ¹ , DQCLK1 ¹	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW ²	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approximately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID ¹	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

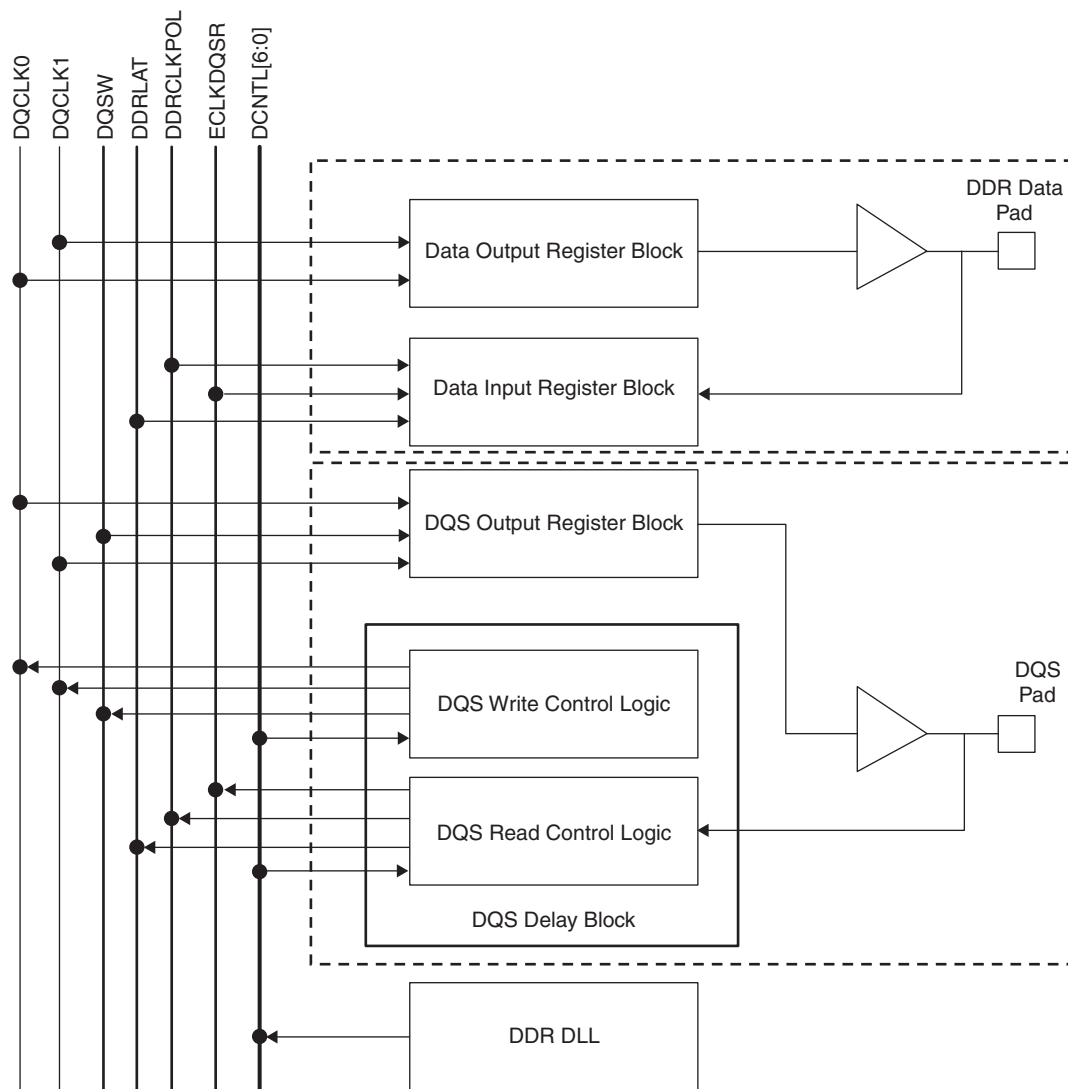
PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.

Figure 2-37. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

Register-to-Register Performance^{1, 2, 3}

Function	–8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	500	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	400	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	260	MHz

LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial Operating Conditions

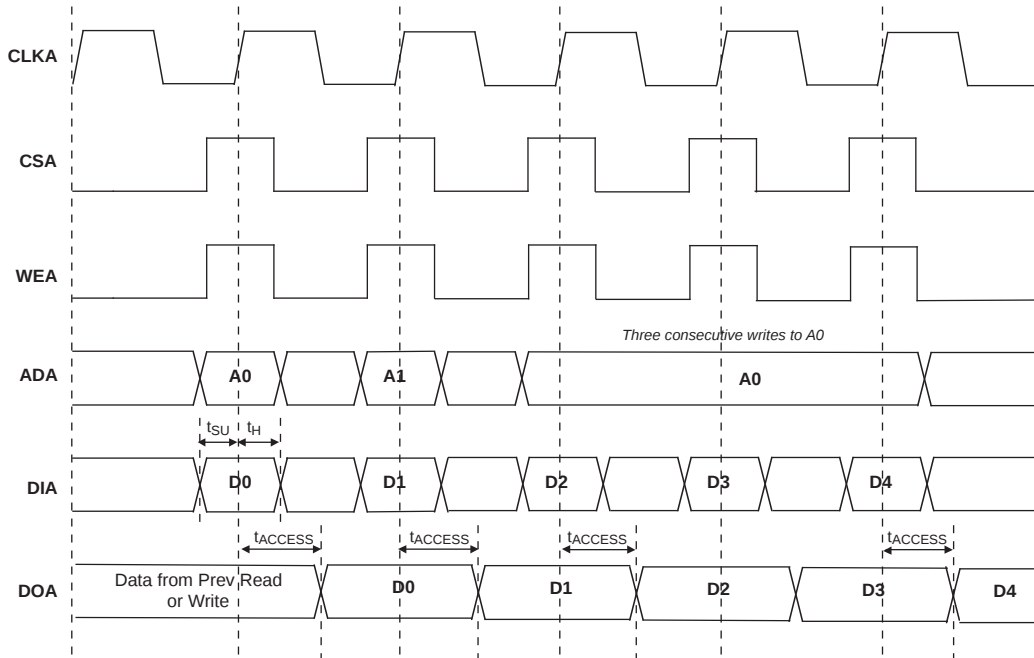
Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	—	4.1	—	4.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	—	1.4	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	—	1.5	—	1.6	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	—	500	—	420	—	375	MHz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting²									
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.3	—	3.6	—	3.9	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SU_DELP}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
t _{H_DELP}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.3	—	3.5	—	3.8	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.8	—	0.9	—	ns

LatticeECP3 Internal Switching Characteristics^{1, 2, 5}

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t _{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	−0.097	—	−0.103	—	−0.109	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t _{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t _{SUDATA_PFU}	Data Setup Time	−0.137	—	−0.155	—	−0.174	—	ns
t _{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t _{SUADDR_PFU}	Address Setup Time	−0.227	—	−0.257	—	−0.286	—	ns
t _{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	−0.055	—	−0.055	—	−0.063	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay ⁴	-	1.09	-	1.16	-	1.23	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	−0.085	—	−0.072	—	−0.058	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	−0.107	—	−0.094	—	−0.081	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	−0.218	—	−0.227	—	−0.237	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	−0.071	—	−0.070	—	−0.068	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	−0.107	—	−0.106	—	−0.106	—	ns

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f _{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock ⁴	2	—	420	MHz
f _{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock ⁴	4	—	420	MHz
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f _{VCO}	PLL VCO frequency			500	—	1000	MHz
f _{PFD} ³	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock ⁴	2	—	420	MHz
AC Characteristics							
t _{PA}	Programmable delay unit			65	130	260	ps
t _{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		f _{OUT} ≤ 250 MHz	Primary clock	45	50	55	%
		f _{OUT} > 250 MHz	Primary clock	30	50	70	%
t _{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t _{OPJIT} ¹	Output clock period jitter	f _{OUT} ≥ 420 MHz		—	—	200	ps
		420 MHz > f _{OUT} ≥ 100 MHz		—	—	250	ps
		f _{OUT} < 100 MHz		—	—	0.025	UIPP
t _{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps
t _{LOCK} ²	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t _{HI}	Input clock high time	90% to 90%		0.5	—	—	ns
t _{LO}	Input clock low time	10% to 10%		0.5	—	—	ns
t _{IPJIT}	Input clock period jitter			—	—	400	ps
t _{RST}	Reset signal pulse width high, RSTK			10	—	—	ns
	Reset signal pulse width high, RST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

Figure 3-16. Jitter Transfer – 1.25 Gbps

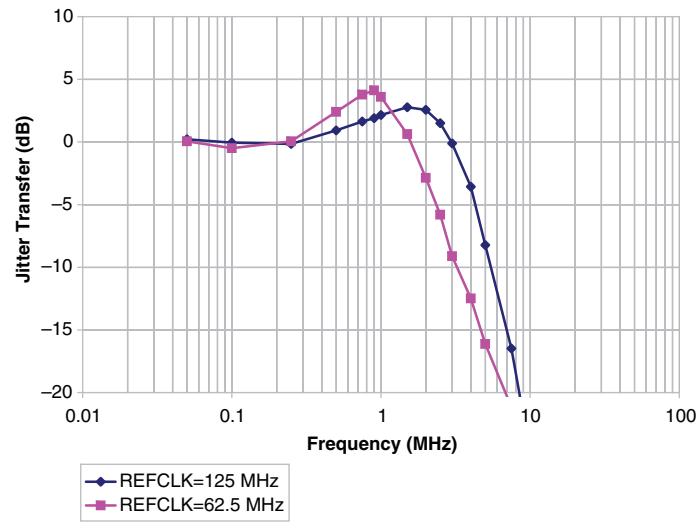


Figure 3-17. Jitter Transfer – 622 Mbps

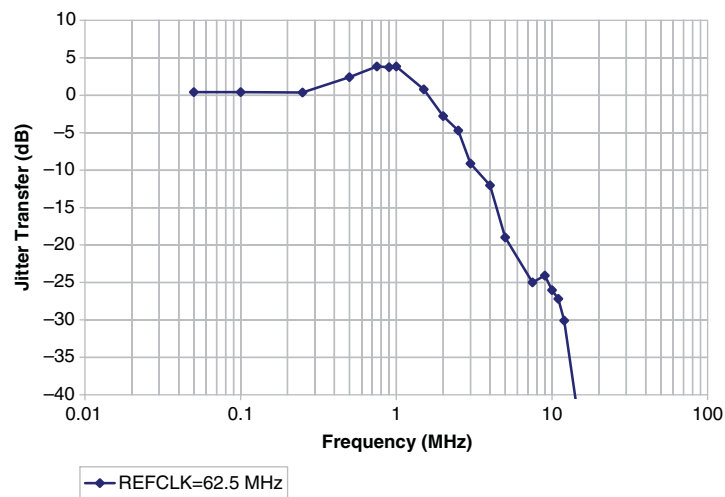
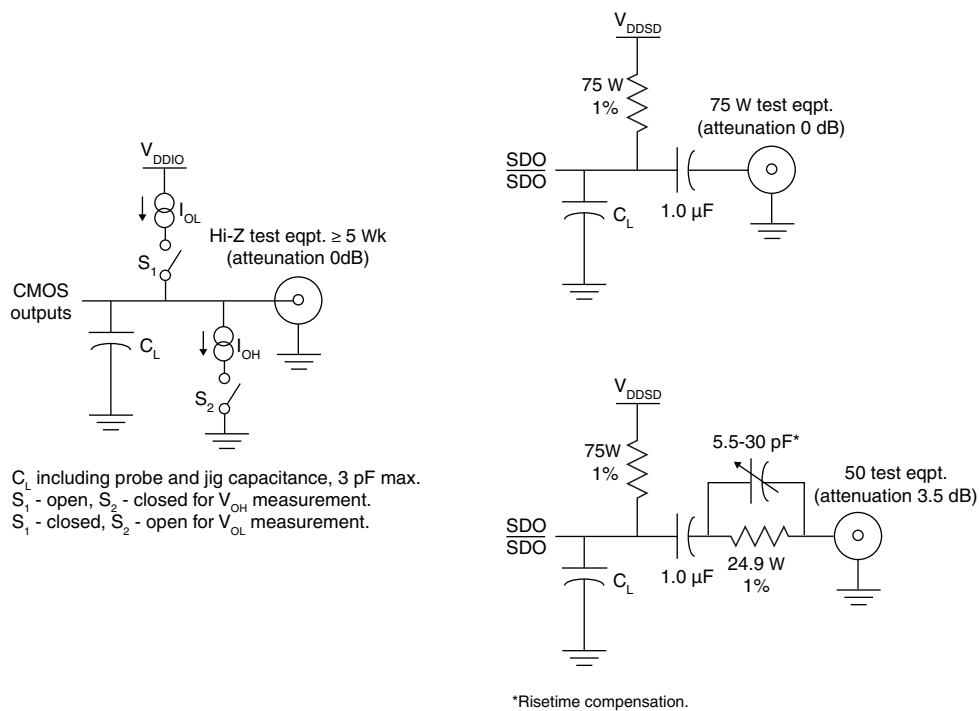


Figure 3-19. Test Loads

Test Loads



Timing Jitter Bandpass

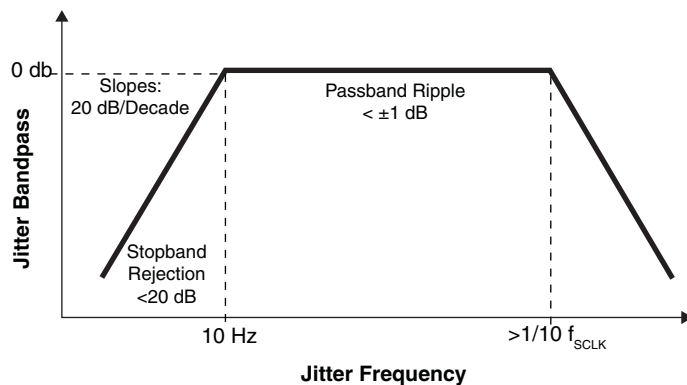
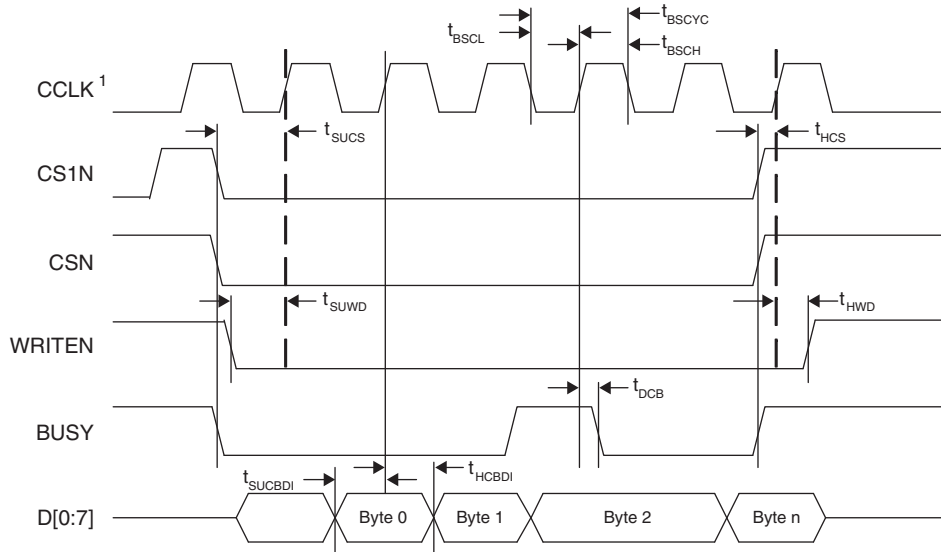


Figure 3-21. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3-22. sysCONFIG Master Serial Port Timing

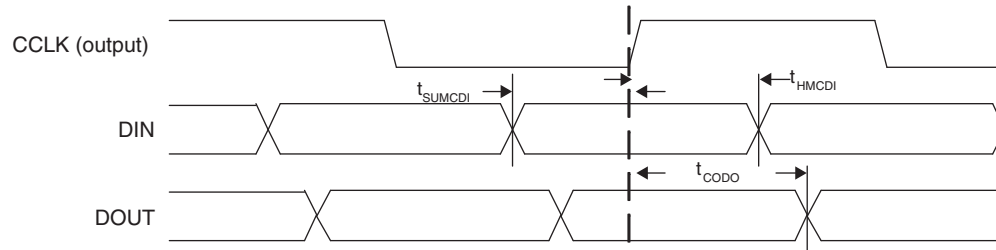
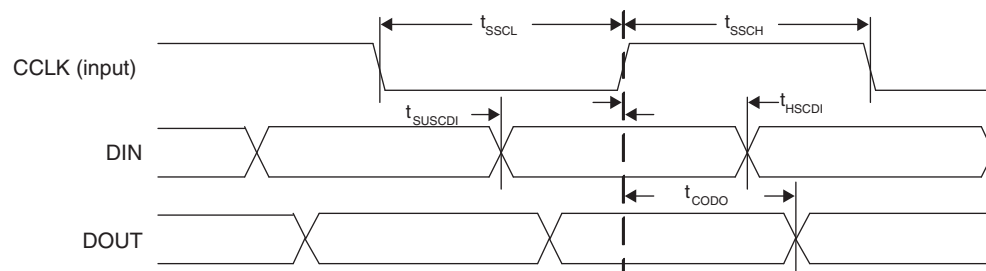


Figure 3-23. sysCONFIG Slave Serial Port Timing

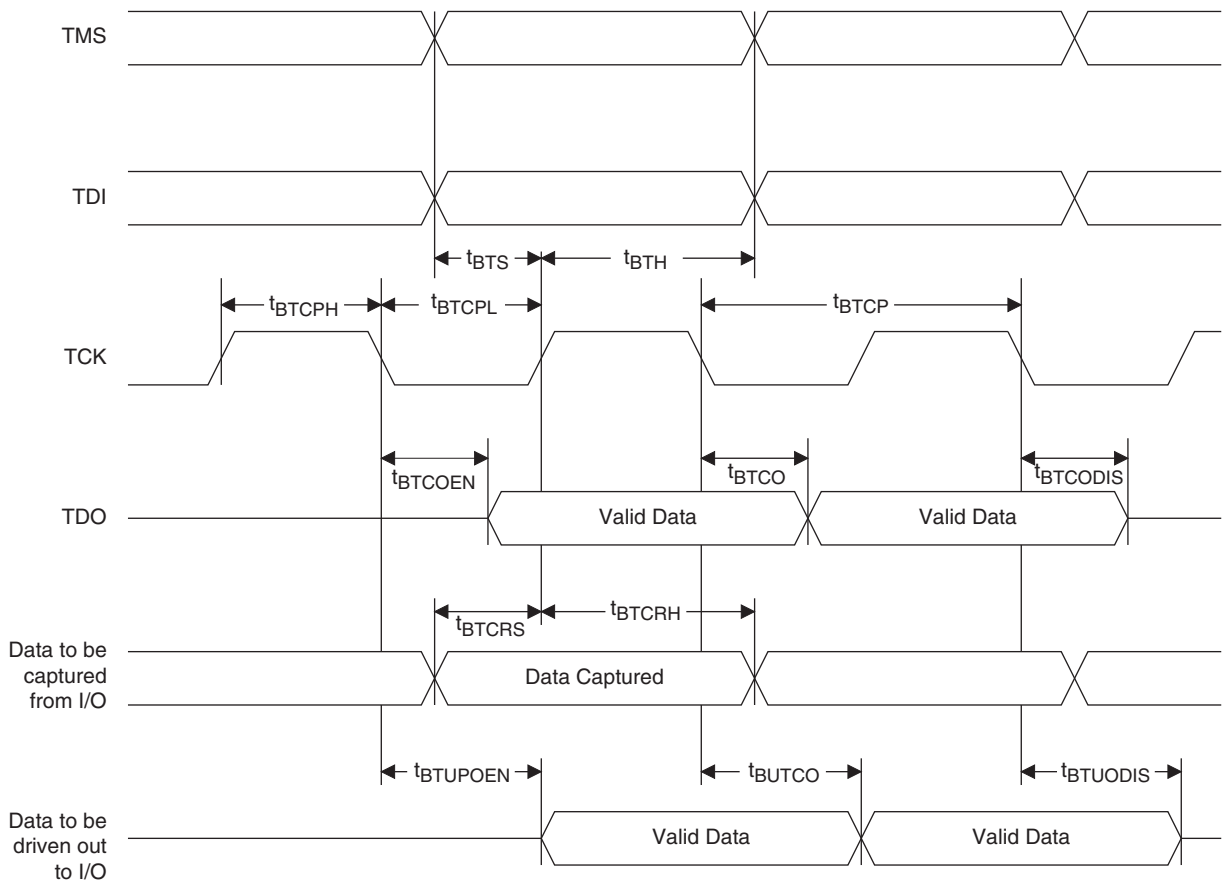


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t_{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t_{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-32. JTAG Port Timing Waveforms



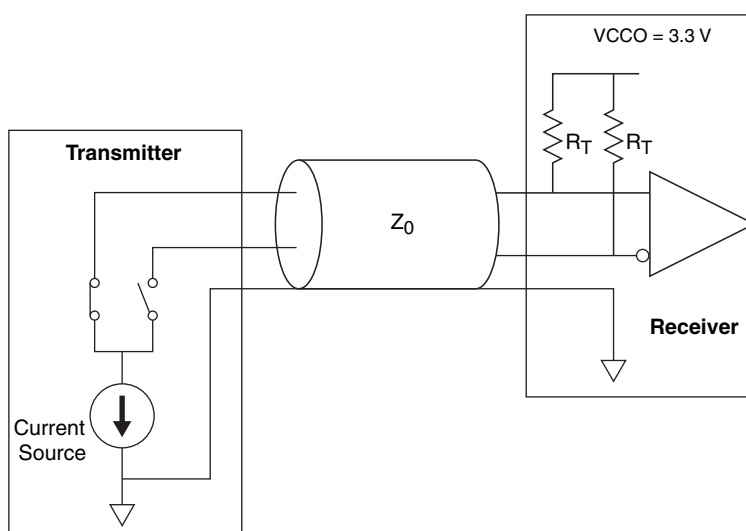
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $ V_{OP} - V_{OM} $	300	—	600	mV
V_{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD} , between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS} , between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $ V_{INP} - V_{INM} $	200	—	600	mV
V_{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	$0.3 + (V_{THD}/2)$	—	$2.1 - (V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per bank	Bank 0	42	60	86	60	94
	Bank 1	36	48	78	48	86
	Bank 2	24	34	36	34	58
	Bank 3	54	59	86	59	104
	Bank 6	63	67	86	67	104
	Bank 7	36	48	54	48	76
	Bank 8	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	4	8	8	8	8
	Bank 3	4	12	12	12	12
	Bank 6	4	12	12	12	12
	Bank 7	4	8	8	8	8
	Bank 8	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	0	0	0	0	0
	Bank 3	0	0	0	0	0
	Bank 6	0	0	0	0	0
	Bank 7	0	0	0	0	0
	Bank 8	0	0	0	0	0
Total Single-Ended User I/O		295	380	490	380	586
VCC		16	32	32	32	32
VCCAUX		8	12	16	12	16
VTT		4	4	8	4	8
VCCA		4	8	16	8	16
VCCPLL		4	4	4	4	4
VCCIO	Bank 0	2	4	4	4	4
	Bank 1	2	4	4	4	4
	Bank 2	2	4	4	4	4
	Bank 3	2	4	4	4	4
	Bank 6	2	4	4	4	4
	Bank 7	2	4	4	4	4
	Bank 8	2	2	2	2	2
VCCJ		1	1	1	1	1
TAP		4	4	4	4	4
GND, GNDIO		98	139	233	139	233
NC		0	0	238	0	116
Reserved ¹		2	2	2	2	2
SERDES		26	52	78	52	104
Miscellaneous Pins		8	8	8	8	8
Total Bonded Pins		484	672	1156	672	1156