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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 11500 |
| Number of Logic Elements/Cells | 92000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 490 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1156-BBGA |
| Supplier Device Package | 1156-FPBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-7lfn1156c |

# LatticeECP3 Family Data Sheet
# Introduction

February 2012

Data Sheet DS1021

## Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    — Half 36x36, two 18x18 or four 9x9 multipliers
    — Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells

- Dedicated read/write levelling functionality
- Dedicated gearing logic
- Source synchronous standards support
  — ADC/DAC, 7:1 LVDS, XGMII
  — High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

*Table 1-1. LatticeECP3™ Family Selection Guide*

| Device | ECP3-17 | ECP3-35 | ECP3-70 | ECP3-95 | ECP3-150 |
|---|---|---|---|---|---|
| LUTs (K) | 17 | 33 | 67 | 92 | 149 |
| sysMEM Blocks (18 Kbits) | 38 | 72 | 240 | 240 | 372 |
| Embedded Memory (Kbits) | 700 | 1327 | 4420 | 4420 | 6850 |
| Distributed RAM Bits (Kbits) | 36 | 68 | 145 | 188 | 303 |
| 18 x 18 Multipliers | 24 | 64 | 128 | 128 | 320 |
| SERDES (Quad) | 1 | 1 | 3 | 3 | 4 |
| PLLs/DLLs | 2 / 2 | 4 / 2 | 10 / 2 | 10 / 2 | 10 / 2 |
| **Packages and SERDES Channels/ I/O Combinations** | | | | | |
| 328 csBGA (10 x 10 mm) | 2 / 116 | | | | |
| 256 ftBGA (17 x 17 mm) | 4 / 133 | 4 / 133 | | | |
| 484 fpBGA (23 x 23 mm) | 4 / 222 | 4 / 295 | 4 / 295 | 4 / 295 | |
| 672 fpBGA (27 x 27 mm) | | 4 / 310 | 8 / 380 | 8 / 380 | 8 / 380 |
| 1156 fpBGA (35 x 35 mm) | | | 12 / 490 | 12 / 490 | 16 / 586 |

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1-1

DS1021 Introduction_01.6

# Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 586 user I/Os. The LatticeECP3 device family also offers up to 320 18 x 18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Diamond™ and ispLEVER® design software allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. Diamond and ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

*Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)*
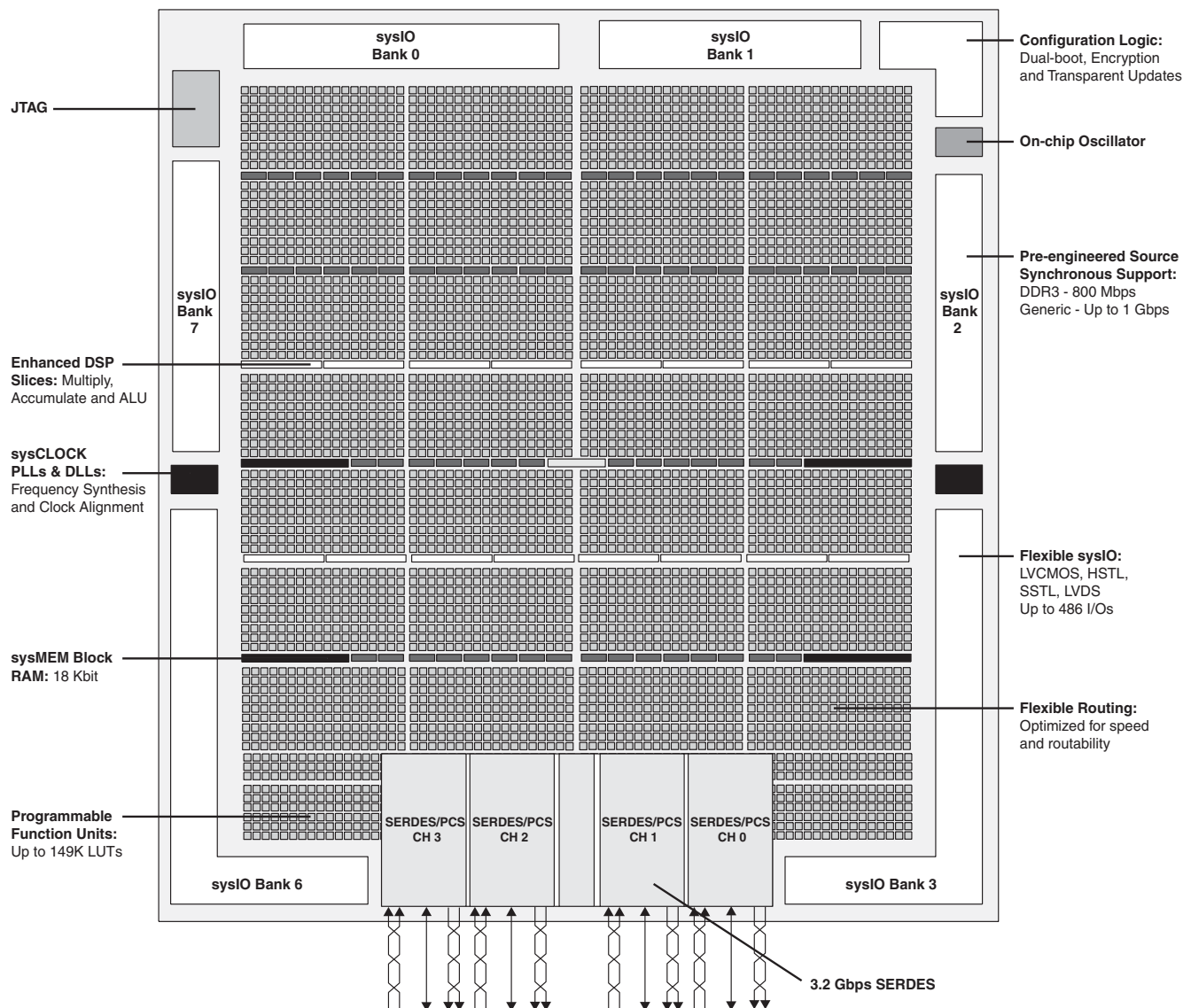


Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

## PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

*Figure 2-5. Delay Locked Loop Diagram (DLL)*
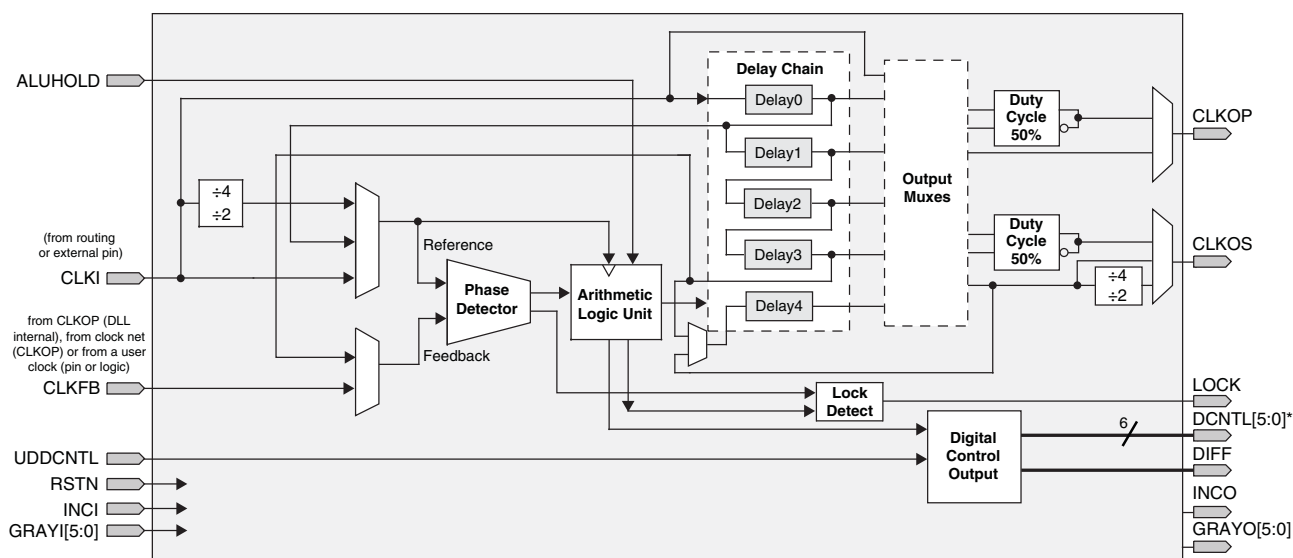


* This signal is not user accessible. This can only be used to feed the slave delay line.

## Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

*Figure 2-12. Per Quadrant Primary Clock Selection*
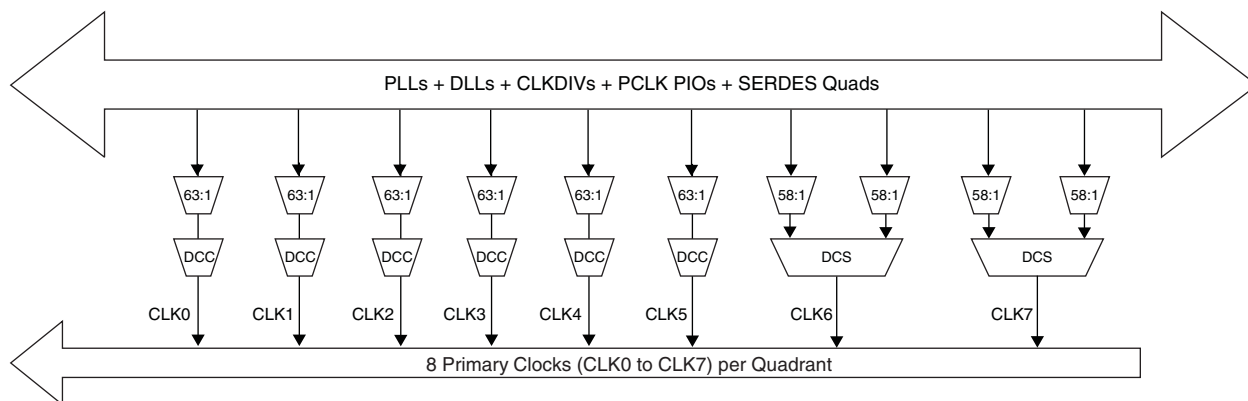


## Dynamic Clock Control (DCC)

The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

*Figure 2-13. DCS Waveforms*
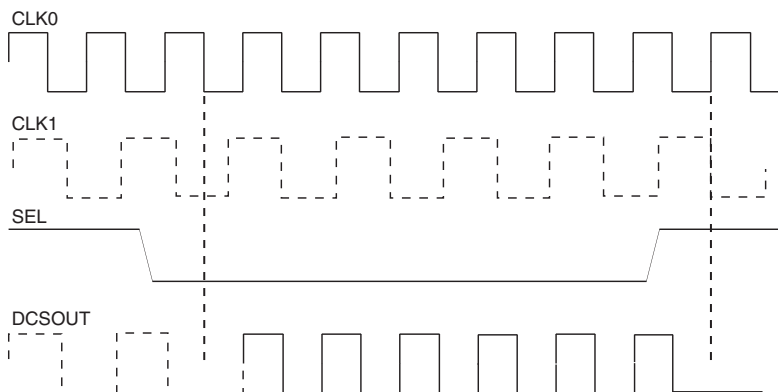
For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

## MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

*Figure 2-26. MULT sysDSP Element*
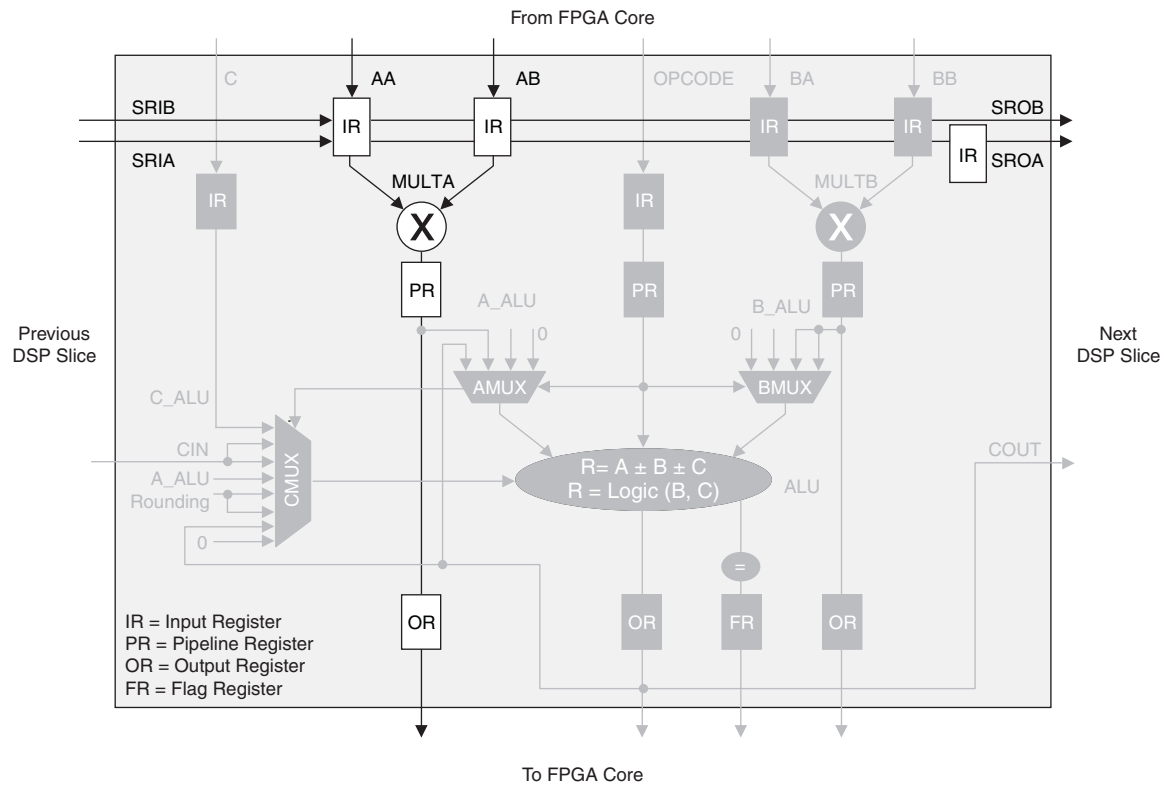
## MMAC DSP Element

The LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-28 shows the MMAC sysDSP element.
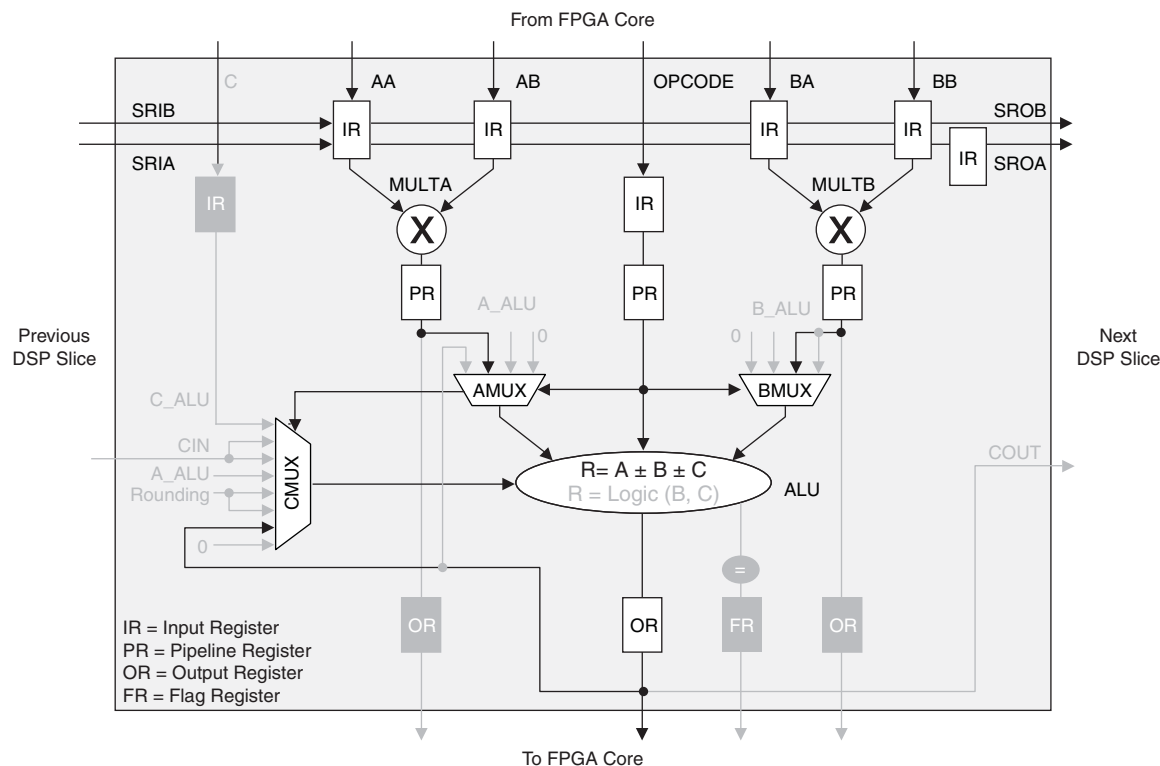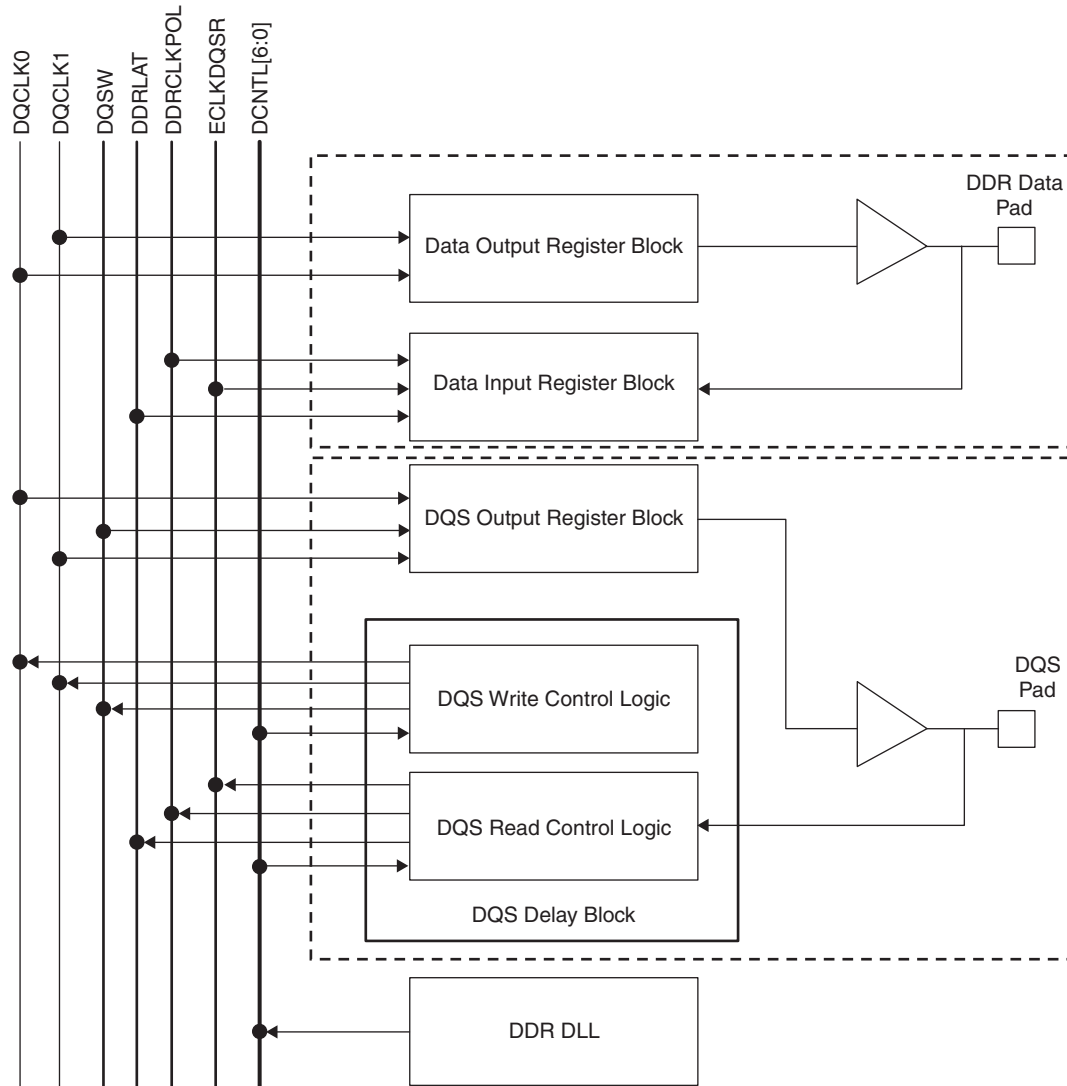
*Figure 2-28. MMAC sysDSP Element*

*Figure 2-37. DQS Local Bus*



## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

## DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

## Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

## External Resistor

LatticeECP3 devices require a single external, 10 kOhm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

## On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.

2. During configuration, users select a different master clock frequency.

3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/– 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

# SERDES Power Supply Requirements[1, 2, 3]

## Over Recommended Operating Conditions

| Symbol | Description | Typ. | Max. | Units |
|---|---|---|---|---|
| **Standby (Power Down)** | | | | |
| $I_{CCA-SB}$ | $V_{CCA}$ current (per channel) | 3 | 5 | mA |
| $I_{CCIB-SB}$ | Input buffer current (per channel) | — | — | mA |
| $I_{CCOB-SB}$ | Output buffer current (per channel) | — | — | mA |
| **Operating (Data Rate = 3.2 Gbps)** | | | | |
| $I_{CCA-OP}$ | $V_{CCA}$ current (per channel) | 68 | 77 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 5 | 7 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 19 | 25 | mA |
| **Operating (Data Rate = 2.5 Gbps)** | | | | |
| $I_{CCA-OP}$ | $V_{CCA}$ current (per channel) | 66 | 76 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | 5 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 15 | 18 | mA |
| **Operating (Data Rate = 1.25 Gbps)** | | | | |
| $I_{CCA-OP}$ | $V_{CCA}$ current (per channel) | 62 | 72 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | 5 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 15 | 18 | mA |
| **Operating (Data Rate = 250 Mbps)** | | | | |
| $I_{CCA-OP}$ | $V_{CCA}$ current (per channel) | 55 | 65 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | 5 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 14 | 17 | mA |
| **Operating (Data Rate = 150 Mbps)** | | | | |
| $I_{CCA-OP}$ | $V_{CCA}$ current (per channel) | 55 | 65 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | 5 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 14 | 17 | mA |

1. Equalization enabled, pre-emphasis disabled.
2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
3. Pre-emphasis adds 20 mA to ICCA-OP data.

# LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

## Over Recommended Commercial Operating Conditions

| Parameter | Description | Device | −8 Min. | −8 Max. | −7 Min. | −7 Max. | −6 Min. | −6 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| **Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)[10]** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | All ECP3EA Devices | 285 | — | 370 | — | 431 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | All ECP3EA Devices | 285 | — | 370 | — | 432 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | All ECP3EA Devices | — | 500 | — | 420 | — | 375 | MHz |
| **Memory Interface** | | | | | | | | | |
| **DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | All ECP3 Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | All ECP3 Devices | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | All ECP3 Devices | 95 | 200 | 95 | 200 | 95 | 166 | MHz |
| $f_{MAX\_DDR2}$ | DDR2 clock frequency | All ECP3 Devices | 125 | 266 | 125 | 200 | 125 | 166 | MHz |
| **DDR3 (Using PLL for SCLK) I/O Pin Parameters** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | All ECP3 Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | All ECP3 Devices | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | All ECP3 Devices | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR3}$ | DDR3 clock frequency | All ECP3 Devices | 300 | 400 | 266 | 333 | 266 | 300 | MHz |
| **DDR3 Clock Timing** | | | | | | | | | |
| $t_{CH}$ (avg)[9] | Average High Pulse Width | All ECP3 Devices | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | UI |
| $t_{CL}$ (avg)[9] | Average Low Pulse Width | All ECP3 Devices | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | UI |
| $t_{JIT}$ (per, lck)[9] | Output Clock Period Jitter During DLL Locking Period | All ECP3 Devices | −90 | 90 | −90 | 90 | −90 | 90 | ps |
| $t_{JIT}$ (cc, lck)[9] | Output Cycle-to-Cycle Period Jitter During DLL Locking Period | All ECP3 Devices | — | 180 | — | 180 | — | 180 | ps |

1.  Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
2.  General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
3.  Generic DDR timing numbers based on LVDS I/O.
4.  DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5.  DDR3 timing numbers based on SSTL15.
6.  Uses LVDS I/O standard.
7.  The current version of software does not support per bank skew numbers; this will be supported in a future release.
8.  Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
9.  Using settings generated by IPexpress.
10. These numbers are generated using best case PLL located in the center of the device.
11. Uses SSTL25 Class II Differential I/O Standard.
12. All numbers are generated with ispLEVER 8.1 software.
13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

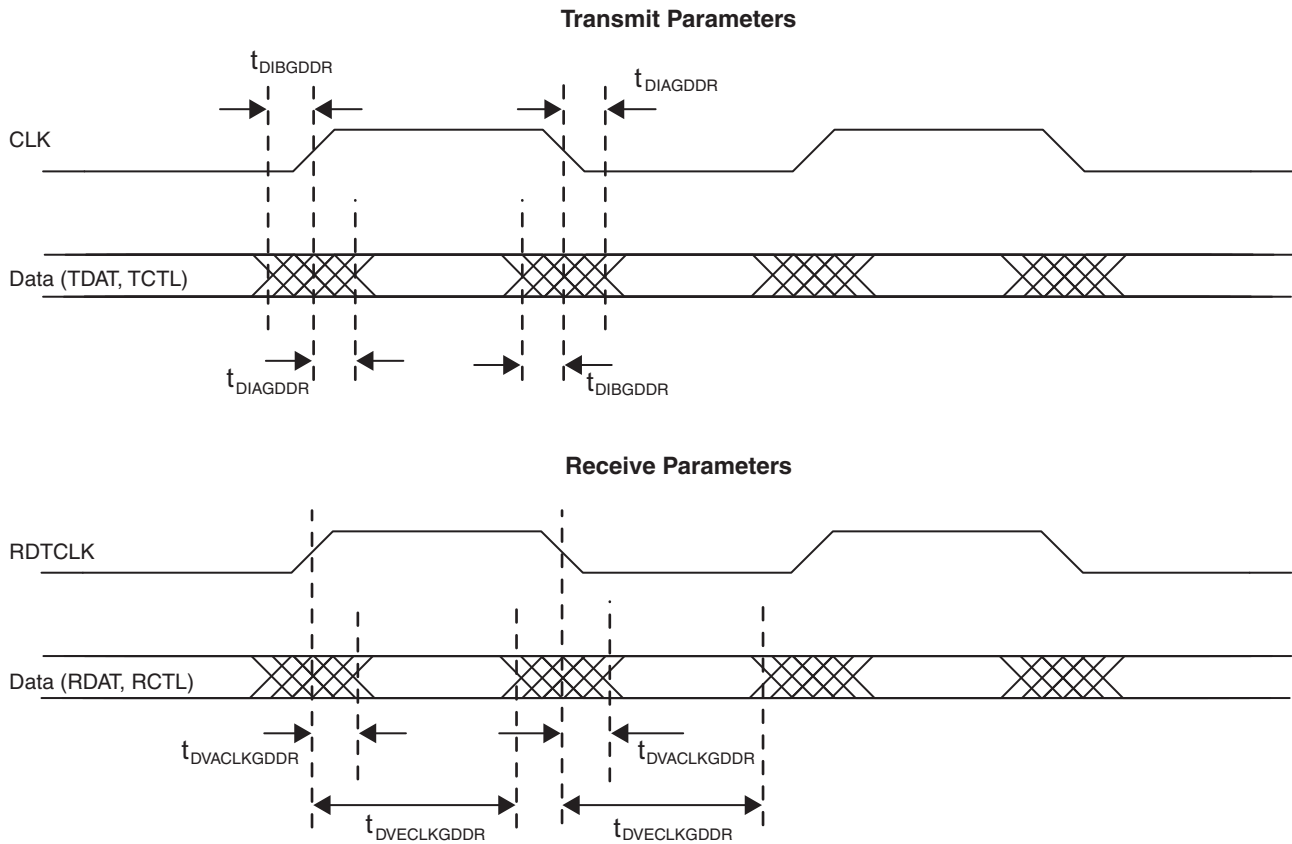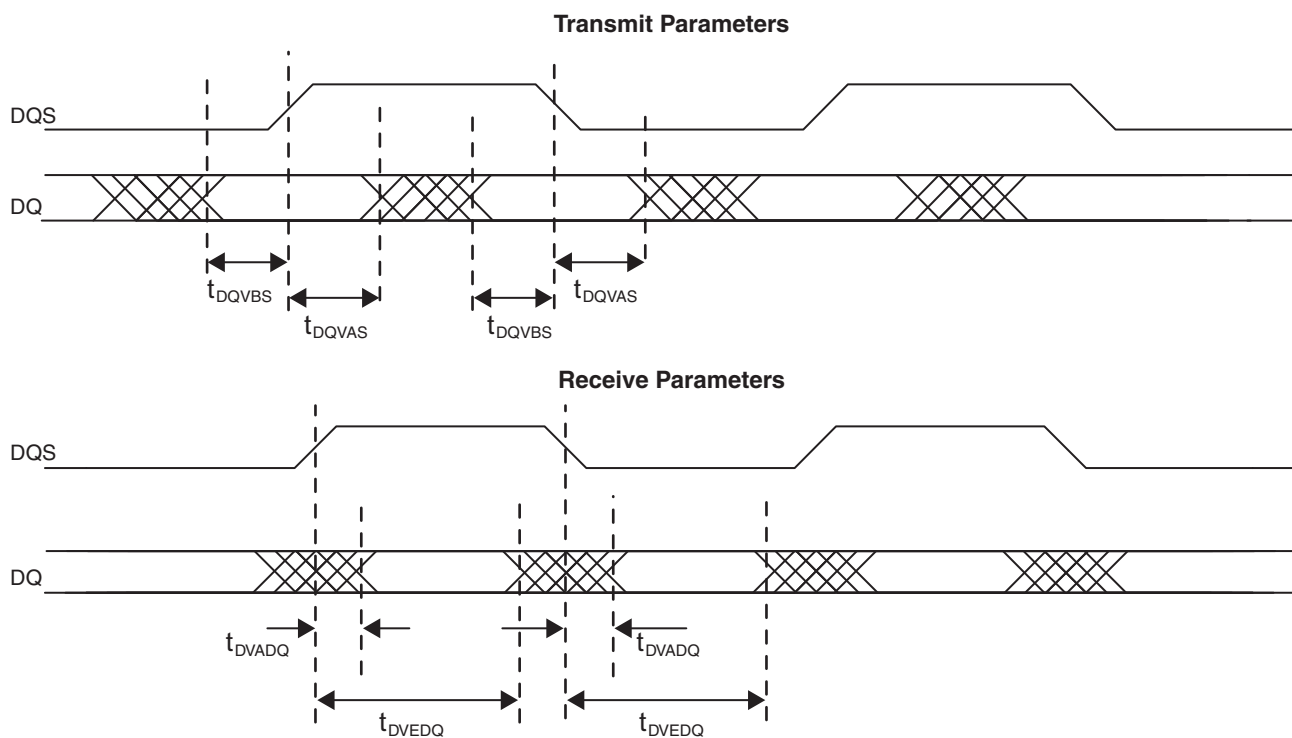*Figure 3-6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)*

**Transmit Parameters**



**Receive Parameters**



*Figure 3-7. DDR/DDR2/DDR3 Parameters*

**Transmit Parameters**



**Receive Parameters**

*Table 3-7. Channel Output Jitter*

| Description | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | — | — | 0.17 | UI, p-p |
| Random | 3.125 Gbps | — | — | 0.25 | UI, p-p |
| Total | 3.125 Gbps | — | — | 0.35 | UI, p-p |
| Deterministic | 2.5 Gbps | — | — | 0.17 | UI, p-p |
| Random | 2.5 Gbps | — | — | 0.20 | UI, p-p |
| Total | 2.5 Gbps | — | — | 0.35 | UI, p-p |
| Deterministic | 1.25 Gbps | — | — | 0.10 | UI, p-p |
| Random | 1.25 Gbps | — | — | 0.22 | UI, p-p |
| Total | 1.25 Gbps | — | — | 0.24 | UI, p-p |
| Deterministic | 622 Mbps | — | — | 0.10 | UI, p-p |
| Random | 622 Mbps | — | — | 0.20 | UI, p-p |
| Total | 622 Mbps | — | — | 0.24 | UI, p-p |
| Deterministic | 250 Mbps | — | — | 0.10 | UI, p-p |
| Random | 250 Mbps | — | — | 0.18 | UI, p-p |
| Total | 250 Mbps | — | — | 0.24 | UI, p-p |
| Deterministic | 150 Mbps | — | — | 0.10 | UI, p-p |
| Random | 150 Mbps | — | — | 0.18 | UI, p-p |
| Total | 150 Mbps | — | — | 0.24 | UI, p-p |

Note: Values are measured with PRBS $2^7$-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.
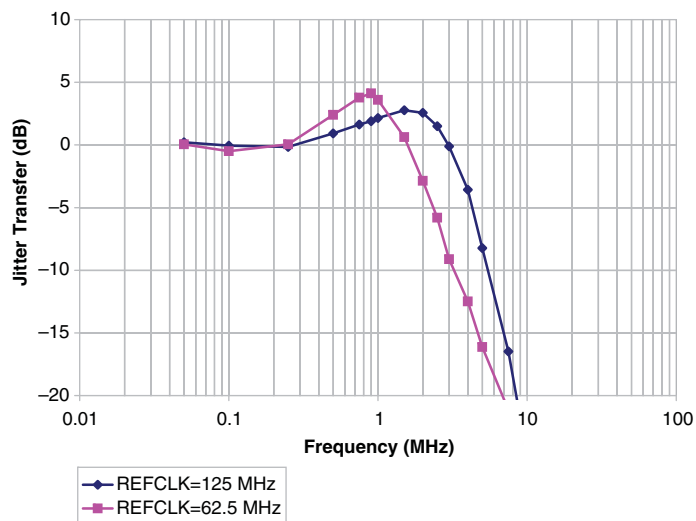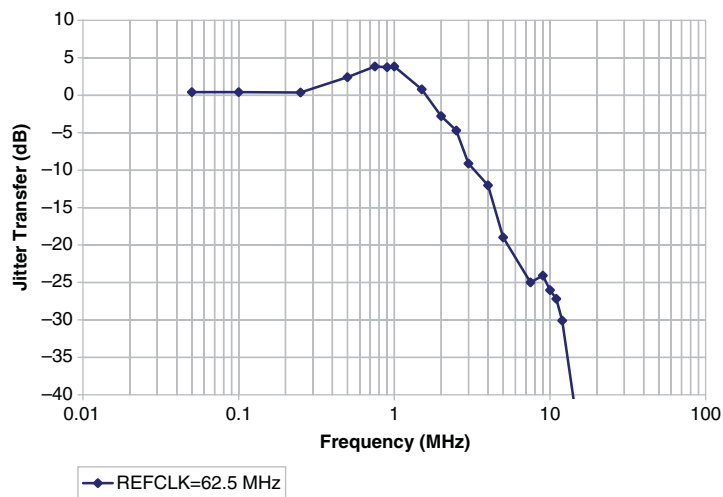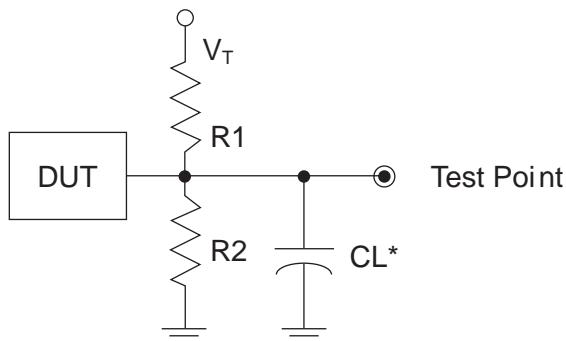
*Figure 3-16. Jitter Transfer – 1.25 Gbps*



*Figure 3-17. Jitter Transfer – 622 Mbps*

# Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

*Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards*



*CL Includes Test Fixture and Probe Capacitance

*Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces*

| Test Condition | $R_1$ | $R_2$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | ∞ | 0 pF | LVCMOS 3.3 = 1.5V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}$/2 | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}$/2 | — |
| LVCMOS 2.5 I/O (Z -> H) | ∞ | 1MΩ | 0 pF | $V_{CCIO}$/2 | — |
| LVCMOS 2.5 I/O (Z -> L) | 1 MΩ | ∞ | 0 pF | $V_{CCIO}$/2 | $V_{CCIO}$ |
| LVCMOS 2.5 I/O (H -> Z) | ∞ | 100 | 0 pF | $V_{OH}$ - 0.10 | — |
| LVCMOS 2.5 I/O (L -> Z) | 100 | ∞ | 0 pF | $V_{OL}$ + 0.10 | $V_{CCIO}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

  
# sysI/O Differential Electrical Characteristics

## Transition Reduced LVDS (TRLVDS DC Specification)

### Over Recommended Operating Conditions

| Symbol | Description | Min. | Nom. | Max. | Units |
|--------|-------------|------|------|------|-------|
| $V_{CCO}$ | Driver supply voltage (+/– 5%) | 3.14 | 3.3 | 3.47 | V |
| $V_{ID}$ | Input differential voltage | 150 | — | 1200 | mV |
| $V_{ICM}$ | Input common mode voltage | 3 | — | 3.265 | V |
| $V_{CCO}$ | Termination supply voltage | 3.14 | 3.3 | 3.47 | V |
| $R_T$ | Termination resistance (off-chip) | 45 | 50 | 55 | Ohms |

Note: LatticeECP3 only supports the TRLVDS receiver.
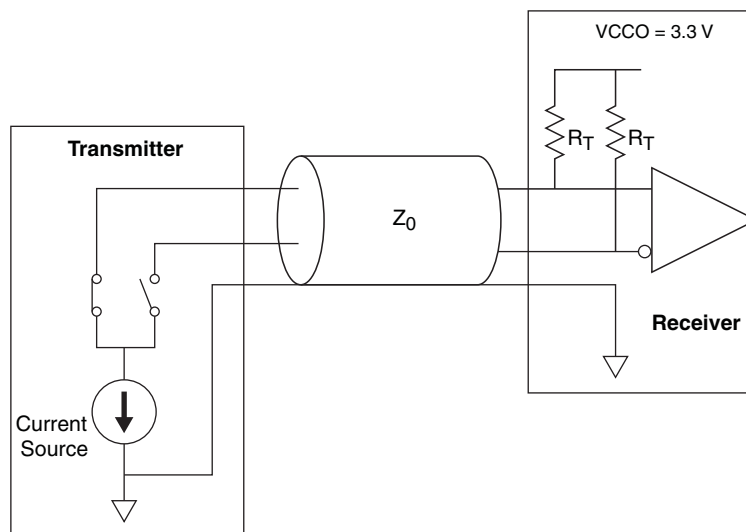


## Mini LVDS

### Over Recommended Operating Conditions

| Parameter Symbol | Description | Min. | Typ. | Max. | Units |
|------------------|-------------|------|------|------|-------|
| $Z_O$ | Single-ended PCB trace impedance | 30 | 50 | 75 | Ohms |
| $R_T$ | Differential termination resistance | 50 | 100 | 150 | Ohms |
| $V_{OD}$ | Output voltage, differential, $|V_{OP} - V_{OM}|$ | 300 | — | 600 | mV |
| $V_{OS}$ | Output voltage, common mode, $|V_{OP} + V_{OM}|/2$ | 1 | 1.2 | 1.4 | V |
| $\Delta V_{OD}$ | Change in $V_{OD}$, between H and L | — | — | 50 | mV |
| $\Delta V_{ID}$ | Change in $V_{OS}$, between H and L | — | — | 50 | mV |
| $V_{THD}$ | Input voltage, differential, $|V_{INP} - V_{INM}|$ | 200 | — | 600 | mV |
| $V_{CM}$ | Input voltage, common mode, $|V_{INP} + V_{INM}|/2$ | $0.3+(V_{THD}/2)$ | — | $2.1-(V_{THD}/2)$ | |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | — | 550 | ps |
| $T_{ODUTY}$ | Output clock duty cycle | 40 | — | 60 | % |

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

# Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Column Number. When Edge is L (Left) or R (Right), only need to specify Row Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| P[Edge][Row Number]E_[A/B/C/D] | I | These general purpose signals are input-only pins and are located near the PLLs. |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| RESERVED | — | This pin is reserved and should not be connected to anything on the board. |
| GND | — | Ground. Dedicated pins. |
| $V_{CC}$ | — | Power supply pins for core logic. Dedicated pins. |
| $V_{CCAUX}$ | — | Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. |
| $V_{CCIOx}$ | — | Dedicated power supply pins for I/O bank x. |
| $V_{CCA}$ | — | SERDES, transmit, receive, PLL and reference clock buffer power supply. All $V_{CCA}$ supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect $V_{CCA}$ to $V_{CC}$. |
| $V_{CCPLL\_[LOC]}$ | — | General purpose PLL supply pins where LOC=L (left) or R (right). |
| $V_{REF1\_x}$, $V_{REF2\_x}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| VTTx | — | Power supply for on-chip termination of I/Os. |
| XRES[1] | — | 10 kOhm +/-1% resistor must be connected between this pad and ground. |
| **PLL, DLL and Clock Functions** | | |
| [LOC][num]_GPLL[T, C]_IN_[index] | I | General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_GPLL[T, C]_FB_[index] | I | Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC]0_GDLLT_IN_[index][2] | I/O | General Purpose DLL (GDLL) input pads where LOC=RUM or LUM, T is True Complement, index is A or B. |
| [LOC]0_GDLLT_FB_[index][2] | I/O | Optional feedback GDLL input pads where LOC=RUM or LUM, T is True Complement, index is A or B. |
| PCLK[T, C][n:0]_[3:0][2] | I/O | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank. |

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-70EA-6FN484I | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-7FN484I | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-8FN484I | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-6LFN484I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-7LFN484I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-8LFN484I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70EA-6FN672I | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-7FN672I | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-8FN672I | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-6LFN672I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-7LFN672I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-8LFN672I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70EA-6FN1156I | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-7FN1156I | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-8FN1156I | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-6LFN1156I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-7LFN1156I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70EA-8LFN1156I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | IND | 67 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Part Number | Voltage | Grade[1] | Power | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE3-95EA-6FN484I | 1.2 V | –6 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-7FN484I | 1.2 V | –7 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-8FN484I | 1.2 V | –8 | STD | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-6LFN484I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-7LFN484I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-8LFN484I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-6FN672I | 1.2 V | –6 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-7FN672I | 1.2 V | –7 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-8FN672I | 1.2 V | –8 | STD | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-6LFN672I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-7LFN672I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-8LFN672I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-6FN1156I | 1.2 V | –6 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-7FN1156I | 1.2 V | –7 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-8FN1156I | 1.2 V | –8 | STD | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-6LFN1156I | 1.2 V | –6 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-7LFN1156I | 1.2 V | –7 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-8LFN1156I | 1.2 V | –8 | LOW | Lead-Free fpBGA | 1156 | IND | 92 |

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| | | | LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V. |
| | | | Updated SERDES External Reference Clock Waveforms. |
| | | | Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break-down table. |
| | | Pinout Information | "Logic Signal Connections" section heading renamed "Package Pinout Information". Software menu selections within this section have been updated. |
| | | | Signal Descriptions table – Updated description for $V_{CCA}$ signal. |
| April 2012 | 02.2EA | Architecture | Updated first paragraph of Output Register Block section. |
| | | | Updated the information about sysIO buffer pairs below Figure 2-38. |
| | | | Updated the information relating to migration between devices in the Density Shifting section. |
| | | DC and Switching Characteristics | Corrected the Definitions in the sysCLOCK PLL Timing table for $t_{RST}$. |
| | | Ordering Information | Updated topside marks with new logos in the Ordering Information section. |
| February 2012 | 02.1EA | All | Updated document with new corporate logo. |
| November 2011 | 02.0EA | Introduction | Added information for LatticeECP3-17EA, 328-ball csBGA package. |
| | | Architecture | Added information for LatticeECP3-17EA, 328-ball csBGA package. |
| | | DC and Switching Characteristics | Updated LatticeECP3 Supply Current table power numbers. |
| | | | Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers. |
| | | Pinout Information | Added information for LatticeECP3-17EA, 328-ball csBGA package. |
| | | Ordering Information | Added information for LatticeECP3-17EA, 328-ball csBGA package. |
| | | | Added ordering information for low power devices and -9 speed grade devices. |
| July 2011 | 01.9EA | DC and Switching Characteristics | Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document. |
| | | | sysCLOCK PLL TIming table, added footnote 4. |
| | | | External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC. |
| | | Pinout Information | Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package. |
| April 2011 | 01.8EA | Architecture | Updated Secondary Clock/Control Sources text section. |
| | | DC and Switching Characteristics | Added data for 150 Mbps to SERDES Power Supply Requirements table. |
| | | | Updated Frequencies in Table 3-6 Serial Output Timing and Levels |
| | | | Added Data for 150 Mbps to Table 3-7 Channel Output Jitter |
| | | | Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, $t_{JIT}$. |
| | | | Corrected Internal Switching Characteristics table, Description for EBR Timing, $t_{SUWREN\_EBR}$ and $t_{HWREN\_EBR}$. |
| | | | Added footnote 1 to sysConfig Port Timing Specifications table. |
| | | | Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| | | | Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram. |
| | | | Updated Device Configuration text section. |
| | | | Corrected software default value of MCCLK to be 2.5 MHz. |
| | | DC and Switching Characteristics | Updated VCCOB Min/Max data in Recommended Operating Conditions table. |
| | | | Corrected footnote 2 in sysIO Recommended Operating Conditions table. |
| | | | Added added footnote 7 for $t_{SKEW\_PRIB}$ to External Switching Characteristics table. |
| | | | Added 2-to-1 Gearing text section and table. |
| | | | Updated External Reference Clock Specification (refclkp/refclkn) table. |
| | | | LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{DINIT}$ information. |
| | | | Added sysCONFIG Port Timing waveform. |
| | | | Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$. |
| | | | Added footnote 4 to sysCLOCK PLL Timing table for $t_{PFD}$. |
| | | | Added SERDES/PCS Block Latency Breakdown table. |
| | | | External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF. |
| | | | Added SERDES External Reference Clock Waveforms. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Pin-to-pin performance table, changed "typically 3% slower" to "typically slower". |
| | | | Updated timing information |
| | | | Updated SERDES minimum frequency. |
| | | | Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements. |
| | | | Updated Serial Input Data Specifications table. |
| | | | Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section. |
| | | Pinout Information | Updated Signal Description tables. |
| | | | Updated Pin Information Summary tables and added footnote 1. |
| February 2009 | 01.0 | — | Initial release. |