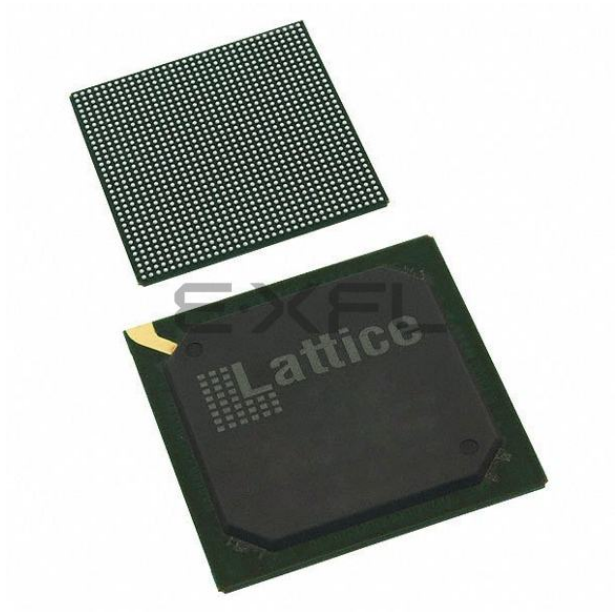
Lattice Semiconductor Corporation - LFE3-95EA-7LFN1156I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

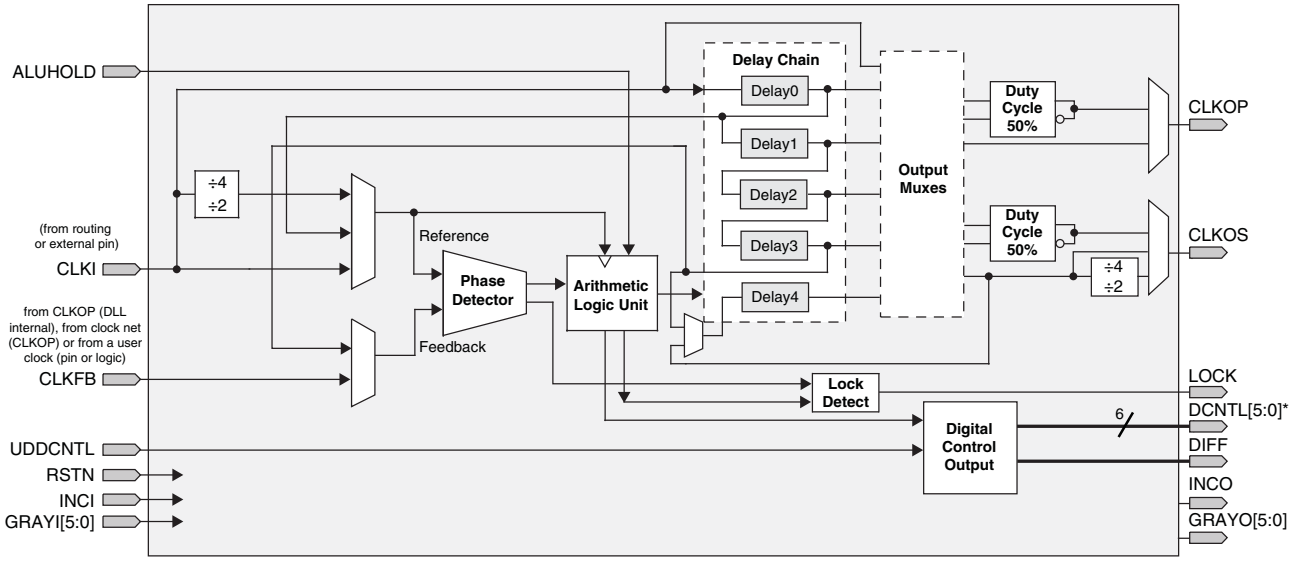
Details	
Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-7lfn1156i

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)



* This signal is not user accessible. This can only be used to feed the slave delay line.

Table 2-5. DLL Signals

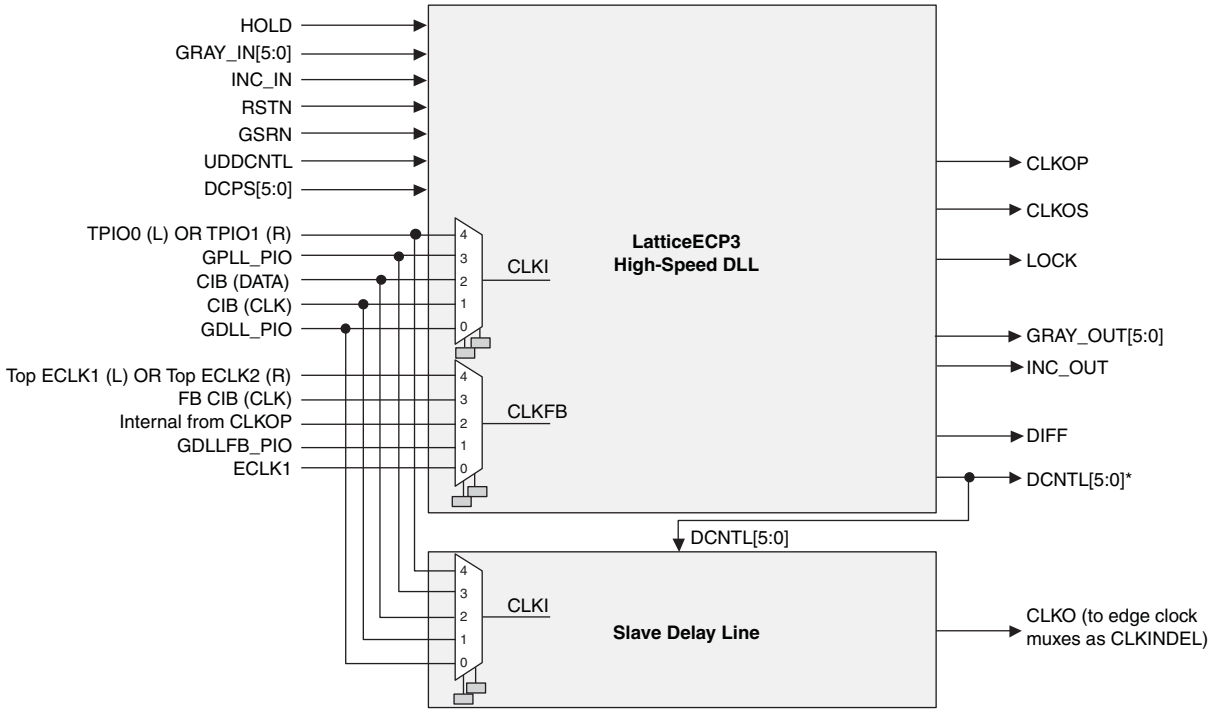
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



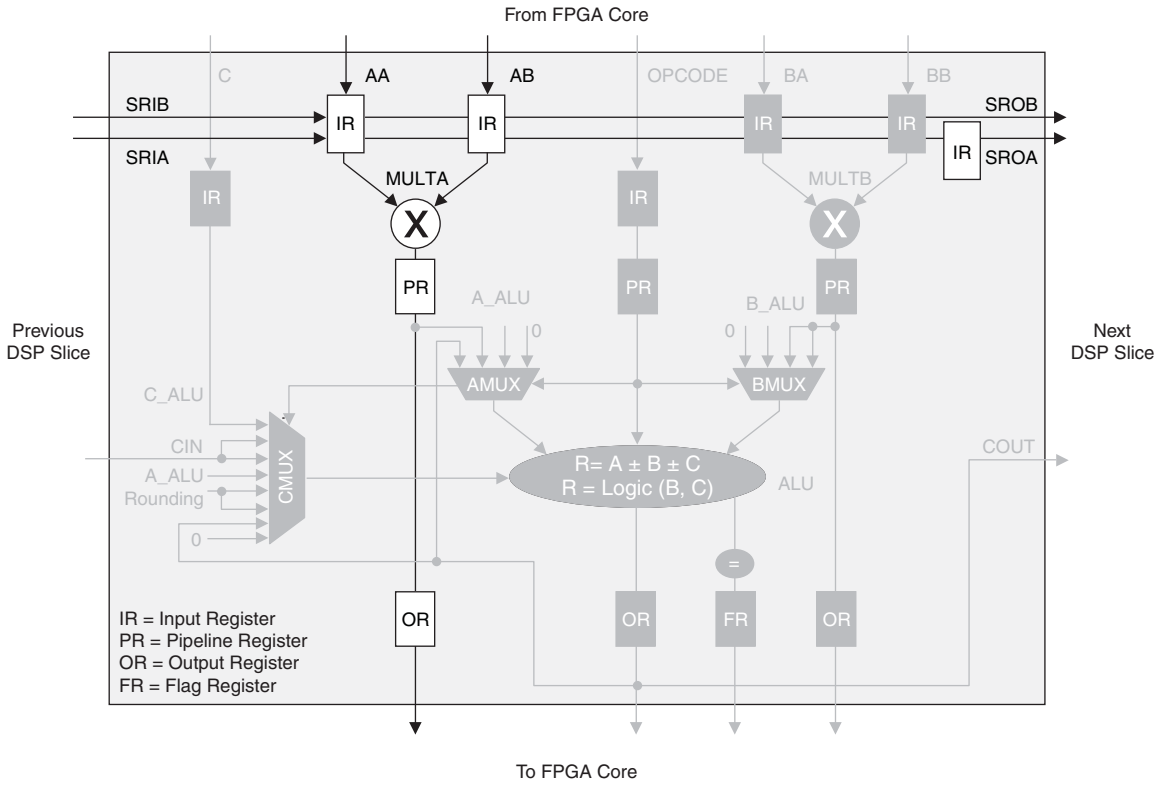
* This signal is not user accessible. It can only be used to feed the slave delay line.

For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

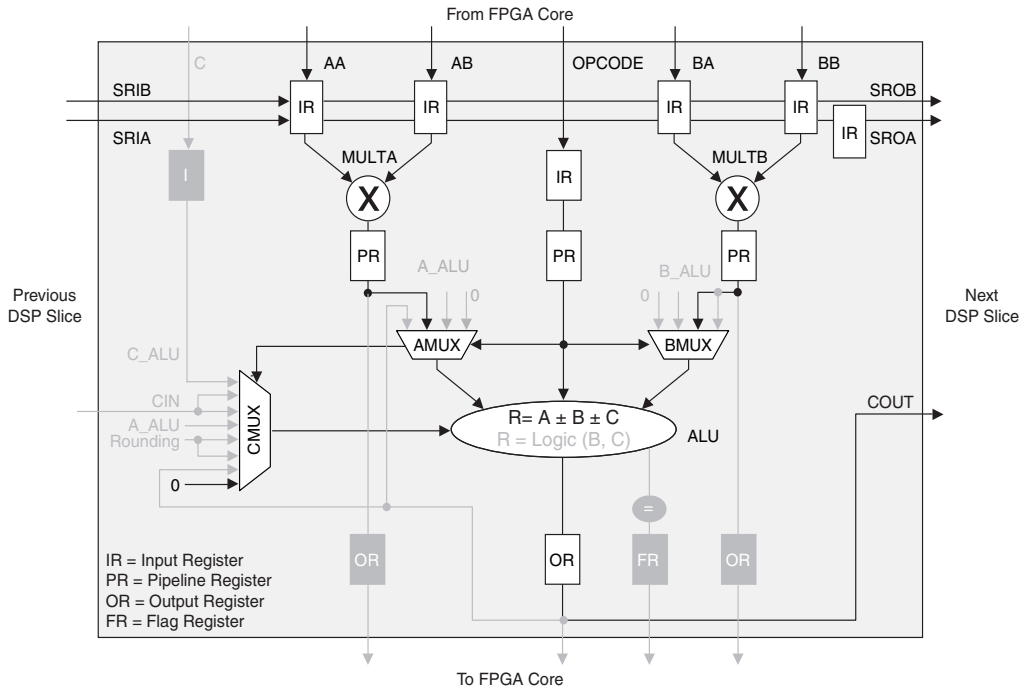
Figure 2-26. MULT sysDSP Element



MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0



LatticeECP3 External Switching Characteristics [1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clock[6]									
f_{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-150EA	—	500	—	420	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-150EA	—	300	—	330	—	360	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	ECP3-150EA	—	250	—	280	—	300	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	ECP3-70EA/95EA	0.8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-70EA/95EA	—	360	—	370	—	380	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	ECP3-70EA/95EA	—	310	—	320	—	330	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-35EA	—	500	—	420	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	ECP3-35EA	0. 8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-35EA	—	300	—	330	—	360	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	ECP3-35EA	—	250	—	280	—	300	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-17EA	—	500	—	420	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	ECP3-17EA	0. 8	—	0.9	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-17EA	—	310	—	340	—	370	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	ECP3-17EA	—	220	—	230	—	240	ps
Edge Clock[6]									
f_{MAX_EDGE}	Frequency for Edge Clock	ECP3-150EA	—	500	—	420	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-150EA	0.9	—	1.0	—	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	ECP3-150EA	—	200	—	210	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-70EA/95EA	0. 9	—	1.0	—	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	ECP3-70EA/95EA	—	200	—	210	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	ECP3-35EA	—	500	—	420	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-35EA	0. 9	—	1.0	—	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	ECP3-35EA	—	200	—	210	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	ECP3-17EA	—	500	—	420	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-17EA	0. 9	—	1.0	—	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	ECP3-17EA	—	200	—	210	—	220	ps
Generic SDR									
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock Without PLL[2]									
t_{CO}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.9	—	4.3	—	4.7	ns
t_{SU}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	ECP3-150EA	1.5	—	1.7	—	2.0	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.3	—	1.5	—	1.7	—	ns

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t_{CO}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.8	—	4.2	—	4.6	ns
t_{SU}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	1.4	—	1.6	—	1.8	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.3	—	1.5	—	1.7	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70EA/95EA	—	500	—	420	—	375	MHz
t_{CO}	Clock to Output - PIO Output Register	ECP3-35EA	—	3.7	—	4.1	—	4.5	ns
t_{SU}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	ECP3-35EA	1.2	—	1.4	—	1.6	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.3	—	1.4	—	1.5	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	—	0.0	—	0.0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-35EA	—	500	—	420	—	375	MHz
t_{CO}	Clock to Output - PIO Output Register	ECP3-17EA	—	3.5	—	3.9	—	4.3	ns
t_{SU}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	ECP3-17EA	1.3	—	1.5	—	1.6	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.3	—	1.4	—	1.5	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	—	0.0	—	0.0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-17EA	—	500	—	420	—	375	MHz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting[2]									
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	3.3	—	3.6	—	39	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.7	—	0.8	—	0.9	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.6	—	1.8	—	2.0	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.0	—	0.0	—	0.0	ns
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-70EA/95EA	—	3.3	—	3.5	—	3.8	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.8	—	0.9	—	ns

LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

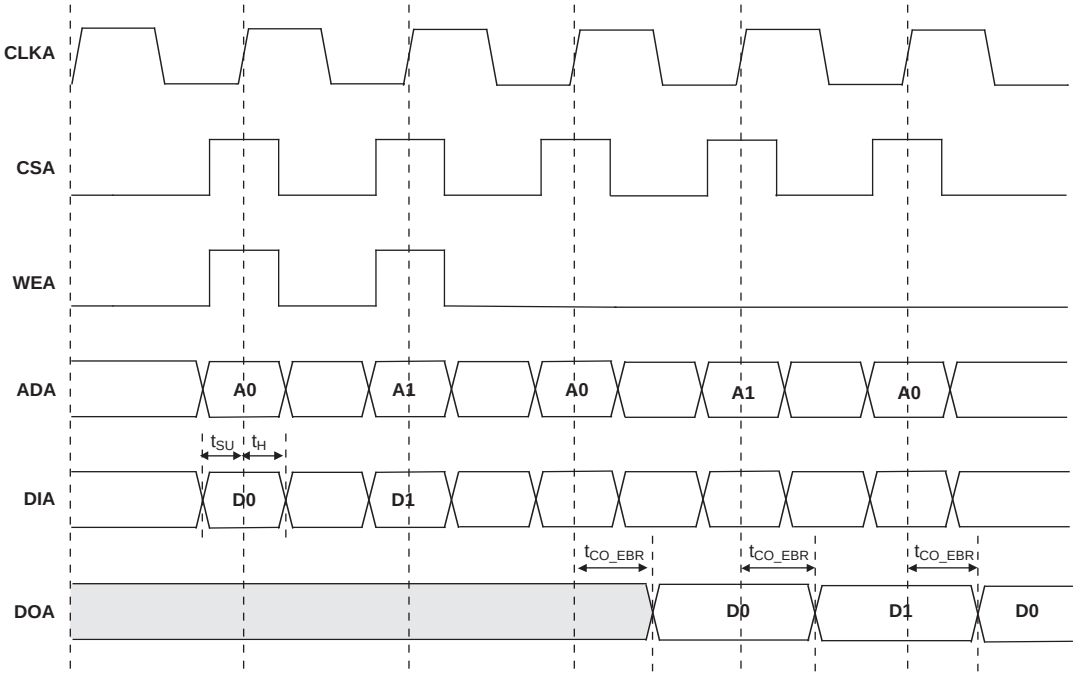
Over Recommended Commercial Operating Conditions

Parameter	Description	Device	–8		–7		–6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)[10]									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	All ECP3EA Devices	285	—	370	—	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All ECP3EA Devices	285	—	370	—	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	500	—	420	—	375	MHz
Memory Interface									
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing									
t_{CH} (avg)[9]	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{CL} (avg)[9]	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t_{JIT} (per, lck)[9]	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	–90	90	–90	90	–90	90	ps
t_{JIT} (cc, lck)[9]	Output Cycle-to-Cycle Period Jitter During DLL Locking Period	All ECP3 Devices	—	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
9. Using settings generated by IPexpress.
10. These numbers are generated using best case PLL located in the center of the device.
11. Uses SSTL25 Class II Differential I/O Standard.
12. All numbers are generated with ispLEVER 8.1 software.
13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.

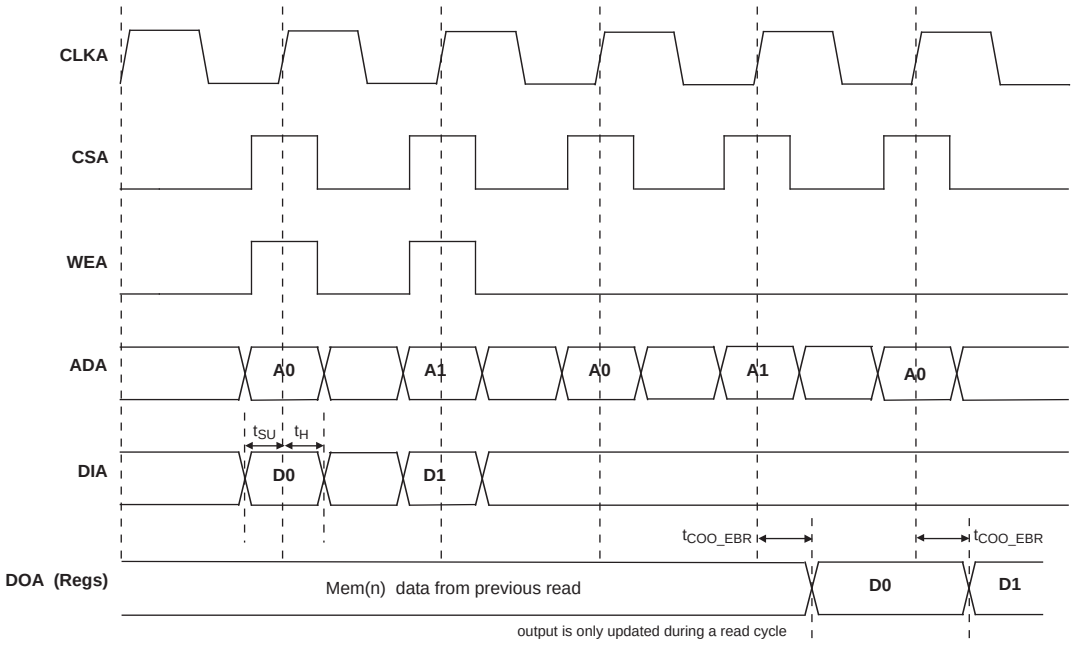
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5, 7] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	–8	–7	–6	Units
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, fast slew rate	0.21	0.25	0.29	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, fast slew rate	0.05	0.07	0.09	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, fast slew rate	0.43	0.51	0.59	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, fast slew rate	0.23	0.28	0.33	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, slow slew rate	1.44	1.58	1.72	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, slow slew rate	0.98	1.10	1.22	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, slow slew rate	0.67	0.77	0.86	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, slow slew rate	0.97	1.09	1.21	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, slow slew rate	0.67	0.76	0.85	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, slow slew rate	1.48	1.63	1.78	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, slow slew rate	1.02	1.14	1.27	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, slow slew rate	0.74	0.84	0.94	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, slow slew rate	1.02	1.14	1.26	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, slow slew rate	0.74	0.83	0.93	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, slow slew rate	1.60	1.77	1.93	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, slow slew rate	1.11	1.25	1.38	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, slow slew rate	0.87	0.98	1.09	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, slow slew rate	0.86	0.97	1.07	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, slow slew rate	1.71	1.89	2.08	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, slow slew rate	1.20	1.34	1.48	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, slow slew rate	1.37	1.56	1.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, slow slew rate	1.11	1.27	1.43	ns
PCI33	PCI, VCCIO = 3.3 V	–0.12	–0.13	–0.14	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.
5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.
6. This data does not apply to the LatticeECP3-17EA device.
7. For details on –9 speed grade devices, please contact your Lattice Sales Representative.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f_{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock[4]	2	—	420	MHz
f_{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock[4]	4	—	420	MHz
f_{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f_{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f_{VCO}	PLL VCO frequency			500	—	1000	MHz
f_{PFD}[3]	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock[4]	2	—	420	MHz
AC Characteristics							
t_{PA}	Programmable delay unit			65	130	260	ps
t_{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		$f_{OUT} \leq 250$ MHz	Primary clock	45	50	55	%
		$f_{OUT} > 250$ MHz	Primary clock	30	50	70	%
t_{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t_{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t_{OPJIT}[1]	Output clock period jitter	$f_{OUT} \geq 420$ MHz		—	—	200	ps
		420 MHz > $f_{OUT} \geq 100$ MHz		—	—	250	ps
		$f_{OUT} < 100$ MHz		—	—	0.025	UIPP
t_{SK}	Input clock to output clock skew when N/M = integer			—	—	500	ps
t_{LOCK}[2]	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t_{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t_{HI}	Input clock high time	90% to 90%		0.5	—	—	ns
t_{LO}	Input clock low time	10% to 10%		0.5	—	—	ns
t_{IPJIT}	Input clock period jitter			—	—	400	ps
t_{RST}	Reset signal pulse width high, RSTK			10	—	—	ns
	Reset signal pulse width high, RST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$ MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP		133	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS		33.3	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	Edge Clock	40		60	%
		Primary Clock	30		70	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock < 250 MHz	45		55	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250 MHz	40		60	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting		—	—	100	ps
t_{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		—	—	+/-400	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)		550	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	—	ps
t_{INSTB}	Input clock period jitter		—	—	500	ps
t_{LOCK}	DLL lock time		8	—	8200	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t_{DEL}	Delay step size		27	45	70	ps
t_{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

SERDES/PCS Block Latency

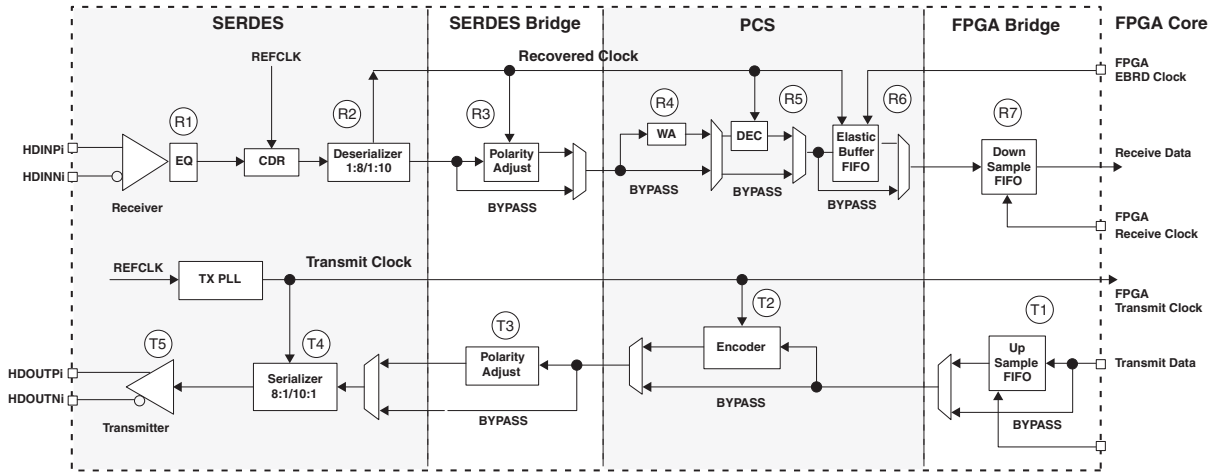
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram



SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z		–20%	50/75/HiZ	+20%	Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/– 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms

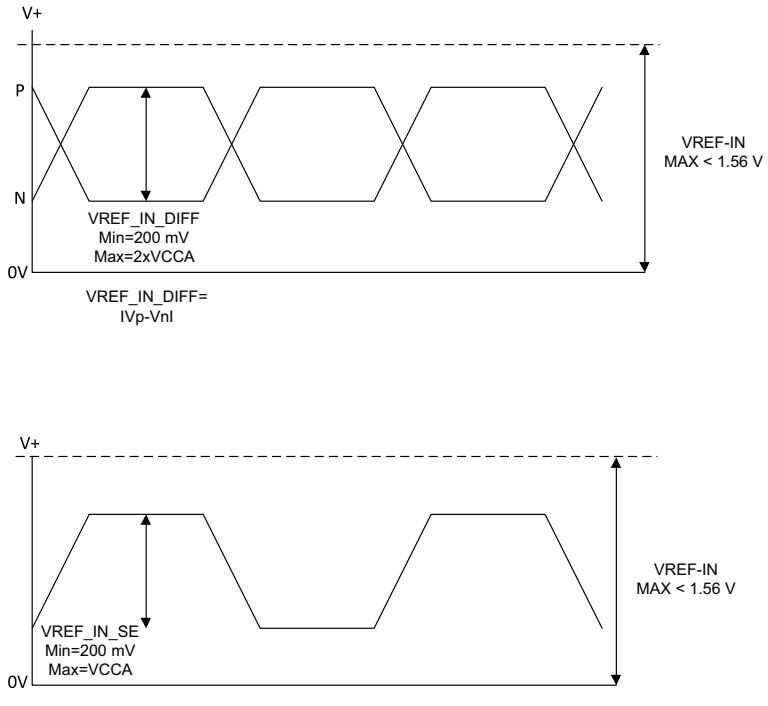


Figure 3-14. Jitter Transfer – 3.125 Gbps

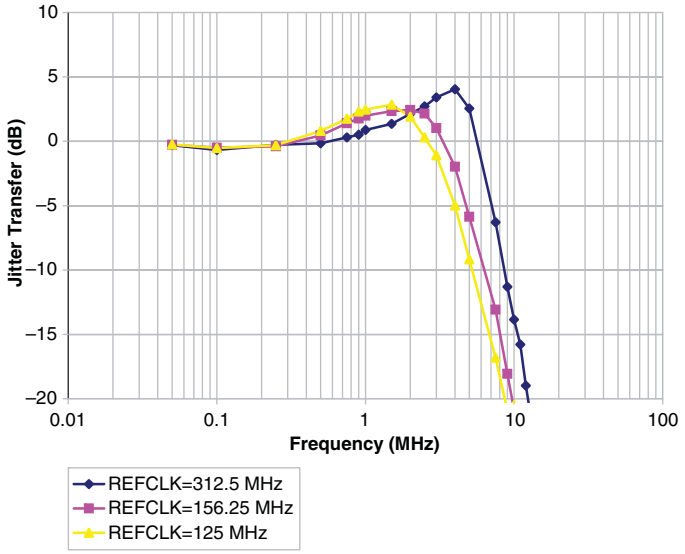


Figure 3-15. Jitter Transfer – 2.5 Gbps

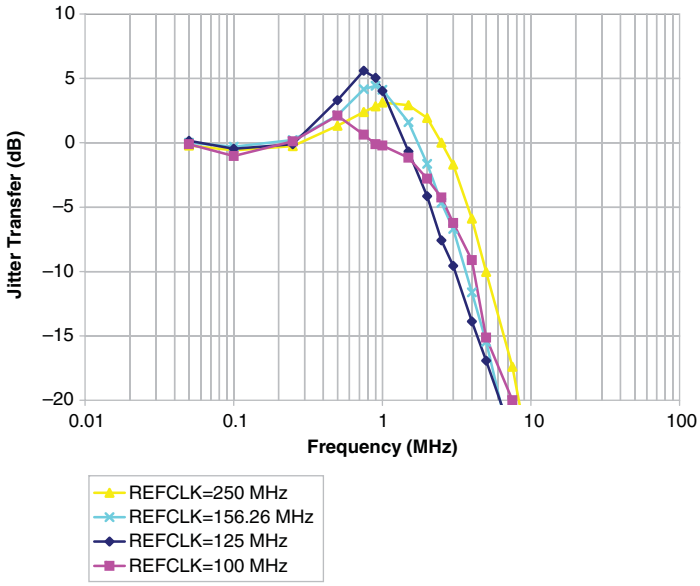
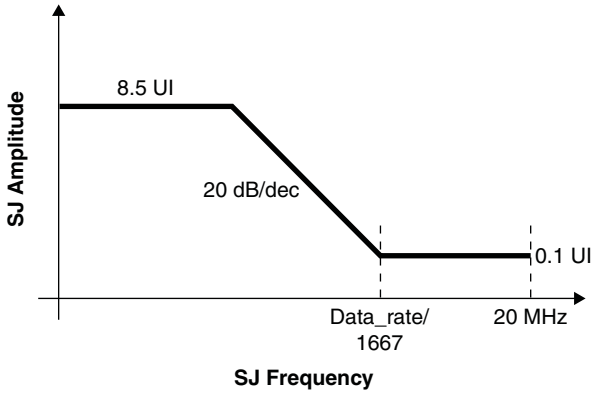


Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

LatticeECP3 Family Data Sheet Ordering Information

April 2014 Data Sheet DS1021

LatticeECP3 Part Number Description

LFE3 – XXX XX – X X XXXXXX X

Device Family
ECP3 (LatticeECP3 FPGA + SERDES)

Logic Capacity
17 = 17K LUTs
35 = 33K LUTs
70 = 67K LUTs
95 = 92K LUTs
150 = 149K LUTs

Supply Voltage
EA = 1.2 V

Speed
6 = Slowest
7
8 = Fastest for LatticeECP3-17EA

Grade
C = Commercial
I = Industrial

Package
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN1156 = 1156-ball Lead-Free fpBGA
MG328 = 328-ball Green csBGA[1]

Power
Blank = Standard Power
L = Low Power

1. Green = Halogen free and lead free.

Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:

Commercial

LATTICE
LFE3-95EA
7FN672C
Datecode

Industrial

LATTICE
LFE3-95EA
7FN672I
Datecode

Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

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Part Number	Voltage	Grade[1]	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	–6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	–7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	–8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	–6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	–7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	–8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW[1]	1.2 V	–6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW[1]	1.2 V	–7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW[1]	1.2 V	–8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.
   - The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
   - The SERDES XRES pin on the TW device passes CDM testing at 250V.

LatticeECP3 Family Data Sheet Revision History

March 2015 **Data Sheet DS1021**

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information All	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3.
			Minor style/formatting changes.
April 2014	02.7EA	DC and Switching Characteristics	Updated LatticeECP3 Supply Current (Standby) table power numbers.
			Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed I_{PW} to I_{PD} in footnote 3.
			Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching Characteristics	Updated the Wake-Up Timing Diagram
			Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms
			Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysI/O Buffer Banks text section – Updated description of “Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)” for hot socketing information.
			sysI/O Buffer Banks text section – Updated description of “Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)” for PCI clamp information.
			On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard.
			sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1.
			Added Oscillator Output Frequency table.
			LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t_{CODO} parameter.
			LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.

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Date	Version	Section	Change Summary
			LatticeECP3 Maximum I/O Buffer Speed table – Description column, references to VCCIO = 3.0V changed to 3.3V.
			Updated SERDES External Reference Clock Waveforms.
			Transmitter and Receiver Latency Block Diagram – Updated sections of the diagram to match descriptions on the SERDES/PCS Latency Break-down table.
		Pinout Information	"Logic Signal Connections" section heading renamed "Package Pinout Information". Software menu selections within this section have been updated.
			Signal Descriptions table – Updated description for V_{CCA} signal.
April 2012	02.2EA	Architecture	Updated first paragraph of Output Register Block section.
			Updated the information about sysIO buffer pairs below Figure 2-38.
			Updated the information relating to migration between devices in the Density Shifting section.
		DC and Switching Characteristics	Corrected the Definitions in the sysCLOCK PLL Timing table for t_{RST}.
		Ordering Information	Updated topside marks with new logos in the Ordering Information section.
February 2012	02.1EA	All	Updated document with new corporate logo.
November 2011	02.0EA	Introduction	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Architecture	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		DC and Switching Characteristics	Updated LatticeECP3 Supply Current table power numbers.
			Typical Building Block Function Performance table, LatticeECP3 External Switching Characteristics table, LatticeECP3 Internal Switching Characteristics table and LatticeECP3 Family Timing Adders: Added speed grade -9 and updated speed grade -8, -7 and -6 timing numbers.
		Pinout Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
		Ordering Information	Added information for LatticeECP3-17EA, 328-ball csBGA package.
			Added ordering information for low power devices and -9 speed grade devices.
July 2011	01.9EA	DC and Switching Characteristics	Removed ESD Performance table and added reference to LatticeECP3 Product Family Qualification Summary document.
			sysCLOCK PLL TIming table, added footnote 4.
			External Reference Clock Specification table – removed reference to VREF-CM-AC and removed footnote for VREF-CM-AC.
		Pinout Information	Pin Information Summary table: Corrected VCCIO Bank8 data for LatticeECP3-17EA 256-ball ftBGA package and LatticeECP-35EA 256-ball ftBGA package.
April 2011	01.8EA	Architecture	Updated Secondary Clock/Control Sources text section.
		DC and Switching Characteristics	Added data for 150 Mbps to SERDES Power Supply Requirements table.
			Updated Frequencies in Table 3-6 Serial Output Timing and Levels
			Added Data for 150 Mbps to Table 3-7 Channel Output Jitter
			Corrected External Switching Characteristics table, Description for DDR3 Clock Timing, t_{JIT}.
			Corrected Internal Switching Characteristics table, Description for EBR Timing, t_{SUWREN_EBR} and t_{HWREN_EBR}.
			Added footnote 1 to sysConfig Port Timing Specifications table.
			Updated description for RX-CIDs to 150M in Table 3-9 Serial Input Data Specifications